INTEGRATED CIRCUITS

DATA HANDBOOK

ICs for Telecom
Bipolar, MOS
Radio pagers
Mobile telephones
ISDN

BOOK IC17 1989

Philips Components

PHILIPS

ICs for Telecom

Bipolar, MOS

Radio pagers
Mobile telephones
ISDN

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type number	description	package	page
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PCF8574AP	remote 8-bit I/O expander; I²C-bus	DIL16; SOT38	369
PCF8574AT	remote 8-bit I/O expander; I²C-bus	SO16L; SOT162A	369
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PCF8577T	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	VSO40; SOT158A	415
PCF8577AP	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	DIL40; SOT129	415
PCF8577AT	LCD direct driver (32 segments) or duplex driver (64 segments); I²C-bus	VSO40; SOT158A	415
PCF8578T	LCD row/column driver for dot matrix graphic displays; 40 outputs (24 are programmable); I²C-bus	VSO56; SOT190	431
PCF8578U	LCD row/column driver for dot matrix graphic displays; 40 outputs (24 are programmable); I²C-bus	uncased chip	431
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PCF8579U	LCD row/column driver for dot matrix graphic displays; 40 column outputs; I²C-bus	uncased chip	437
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PCF8582AT	256 x 8-bit static CMOS EEPROM; I²C-bus	SO16L; SOT162A	443
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type number	description	package	page
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PCF8591P	8-bit ADC/DAC; I^2C-bus	DIL16; SOT38	471
PCF8591T	8-bit ADC/DAC; I^2C-bus	SO16L; SOT162A	471
SCC68070	16/32-bit MPU; 68000 CPU; MMU; DMA; timer; UART; I^2C-bus	PLCC84; SOT189	489
TDA1576	FM/IF amplifier and detector	DIL18; SOT102	491
TDA7050	140 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	DIL8; SOT97	503
TDA7050T	140 mW BTL or 2 x 75 mW stereo audio power amplifier; low voltage	SO8; SOT96A	507
TDA7052	1 W BTL mono audio amplifier	DIL8; SOT97	511
TDD1742T	low-power frequency synthesizer (LOPSY)	SO28; SOT136A	517
UAA2033T	digital paging receiver; low power	SO28; SOT136A	539
UMA1000T	data processor for cellular radio (DPROC)	SO28; SOT136A	547
UMA1010T	low-power universal frequency synthesizer for radio communications; I^2C-bus	SO28; SOT136A	577

FORTHCOMING NEW PRODUCTS

The types listed below are not included in this handbook. Information will be available at a later date.

PCD3348	microcontroller for telephone sets; 256 x 8-bit RAM; 8K x 8-bit ROM; I^2C-bus
PCF8584	8-bit parallel bus to I^2C-bus protocol converter

GENERAL

Product status definitions
for type numbers with
prefixes NE, SA, SE

Ordering information
for type numbers with
prefixes NE, SA, SE

Type designation
for type numbers with prefixes
PCA, PCB, PCD, PCF, TDA, TDD

Rating systems
for type numbers with prefixes
PCA, PCB, PCD, PCF, TDA, TDD

Handling MOS devices

PRODUCT STATUS DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	**Formative or in Design**	This data sheets contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	**Sampling or Pre-Production**	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	**First Production**	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains final specifications. Signetics/Philips reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Ordering Information for Prefixes ADC, AM, CA, DAC, ICM, LF, LM, MC, NE, OP, SA, SE, SG, μA, UC, ULN

Linear Products

Table 1. Part Number Description

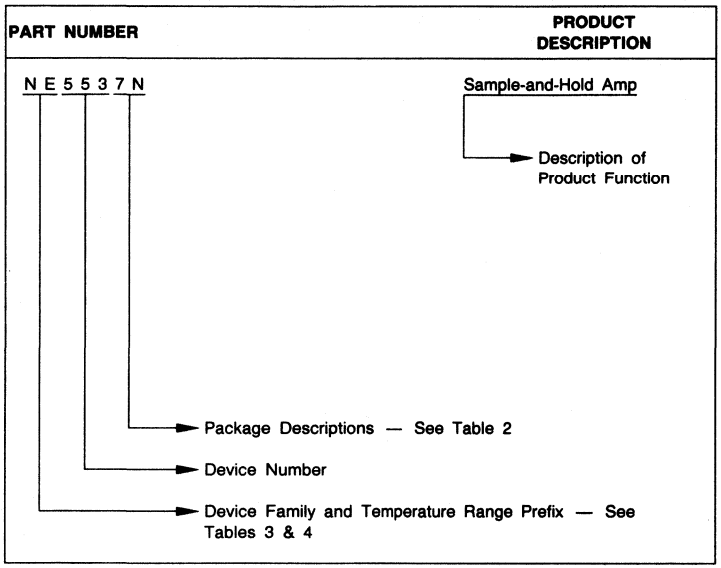

Table 2. Package Descriptions

OLD	NEW	PACKAGE DESCRIPTION
A, AA	N	14-lead plastic DIP
A	N-14	14-lead plastic DIP (selected analog products only)
B, BA	N	16-lead plastic DIP
	D	Microminiature package (SO)
F	F	14-, 16-, 18-, 22-, and 24-lead ceramic DIP (Cerdip)
I, IK	I	14-, 16-, 18-, 22-, 28-, and 4-lead ceramic DIP
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA, NX	N	24-lead plastic DIP
Q, R	Q	10-, 14-, 16-, and 24-lead ceramic flat
T, TA	H	8-lead TO-99
U	U	SIP plastic power
V	N	8-lead plastic DIP
XA	N	18-lead plastic DIP
XC	N	20-lead plastic DIP
XC	N	22-lead plastic DIP
XL, XF	N	28-lead plastic DIP
	A	PLCC
	EC	TO-46 header
	FE	8-lead ceramic DIP

Table 3. Signetics Prefix and Device Temperature

PREFIX	DEVICE TEMPERATURE RANGE
NE	0 to +70°C
SE	−55°C to +125°C
SA	−40°C to +85°C

Table 4. Industry Standard Prefix

PREFIX	DEVICE FAMILY
ADC	Linear Industry Standard
AM	Linear Industry Standard
CA	Linear Industry Standard
DAC	Linear Industry Standard
ICM	Linear Industry Standard
LF	Linear Industry Standard
LM	Linear Industry Standard
MC	Linear Industry Standard
NE	Linear Industry Standard
OP	Linear Industry Standard
SA	Linear Industry Standard
SE	Linear Industry Standard
SG	Linear Industry Standard
μA	Linear Industry Standard
UC	Linear Industry Standard
ULN	Linear Industry Standard

PRO ELECTRON TYPE DESIGNATION CODE FOR INTEGRATED CIRCUITS

This type nomenclature applies to semiconductor monolithic, semiconductor multi-chip, thin-film, thick-film and hybrid integrated circuits.

A basic type number consists of:

THREE LETTERS FOLLOWED BY A SERIAL NUMBER

FIRST AND SECOND LETTER

1. DIGITAL FAMILY CIRCUITS

   The FIRST TWO LETTERS identify the FAMILY (see note 1).

2. SOLITARY CIRCUITS

   The FIRST LETTER divides the solitary circuits into:

   S : Solitary digital circuits
   T : Analogue circuits
   U : Mixed analogue/digital circuits

   The SECOND LETTER is a serial letter without any further significance except 'H' which stands for hybrid circuits (see note 3).

3. MICROPROCESSORS

   The FIRST TWO LETTERS identify microprocessors and correlated circuits as follows:

   MA : { Microcomputer / Central processing unit
   MB : Slice processor (see note 2)
   MD : Correlated memories
   ME : Other correlated circuits (interface, clock, peripheral controller, etc.)

4. CHARGE-TRANSFER DEVICES AND SWITCHED CAPACITORS

   The FIRST TWO LETTERS identify the following:

   NH : Hybrid circuits
   NL : Logic circuits
   NM : Memories
   NS : Analogue signal processing, using switched capacitors
   NT : Analogue signal processing, using CTDs
   NX : Imaging devices
   NY : Other correlated circuits

Notes

1. A logic family is an assembly of digital circuits designed to be interconnected and defined by its basic electrical characteristics (such as: supply voltage, power consumption, propagation delay, noise immunity).
2. By 'slice processor' is meant: a functional slice of microprocessor.
3. The first letter 'S' should be used for all solitary memories, to which, in the event of hybrids, the second letter 'H' should be added (e.g. SH for Bubble-memories).

THIRD LETTER

It indicates the operating ambient temperature range.
The letters A to G give information about the temperature:

A : temperature range not specified
B : 0 to + 70 °C
C : −55 to + 125 °C
D : −25 to + 70 °C
E : −25 to + 85 °C
F : −40 to + 85 °C
G : −55 to + 85 °C

If a circuit is published for another temperature range, the letter indicating a narrower temperature range may be used or the letter 'A'.

Example: the range 0 to + 75 °C can be indicated by 'B' or 'A'.

SERIAL NUMBER

This may be either a 4-digit number assigned by Pro Electron, or the serial number (which may be a combination of figures and letters) of an existing company type designation of the manufacturer.

To the basic type number may be added:

A VERSION LETTER

Indicates a minor variant of the basic type or the package. Except for 'Z', which means customized wiring, the letter has no fixed meaning. The following letters are recommended for package variants:

C : for cylindrical
D : for ceramic DIL
F : for flat pack
L : for chip on tape
P : for plastic DIL
Q : for QIL
T : for miniature plastic (mini-pack)
U : for uncased chip

Alternatively a TWO LETTER SUFFIX may be used instead of a single package version letter, if the manufacturer (sponsor) wishes to give more information.

FIRST LETTER: General shape

C : Cylindrical
D : Dual-in-line (DIL)
E : Power DIL (with external heatsink)
F : Flat (leads on 2 sides)
G : Flat (leads on 4 sides)
K : Diamond (TO-3 family)
M : Multiple-in-line (except Dual-, Triple-, Quadruple-in-line)
Q : Quadruple-in-line (QIL)
R : Power QIL (with external heatsink)
S : Single-in-line
T : Triple-in-line
W : Lead chip-carrier (LCC)
X : Leadless chip-carrier (LLCC)
Y : Pin grid array (PGA)

SECOND LETTER: Material

C : Metal-ceramic
G : Glass-ceramic (cerdip)
M : Metal
P : Plastic

A hyphen precedes the suffix to avoid confusion with a version letter.

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

DEVICE DATA

IST BUS SPECIFICATION

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1.0 INTRODUCTION

2.0 LAYER 1 CHARACTERISTICS
- 2.1 Configuration and definitions
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- 2.3 Line characteristics
- 2.4 Isolation
- 2.5 Line signal
- 2.6 Noise immunity
- 2.7 Receiver input sensitivity
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- 2.9 Frame structure
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- 2.11 bd access protocol
- 2.12 b channel access protocol

3.0 LAYER 2 PROTOCOL FOR THE bd CHANNEL
- 3.1 Service
- 3.2 Protocol
- 3.3 Maintenance

4.0 LAYER 3 OF THE bd CHANNEL

1.0 INTRODUCTION

The Integrated Services Terminal (IST) bus offers a low cost in-house communication network. The voice service and the data service are integrated in one communication network.

As a stand alone digital communication network the IST bus provides in-house communication for up to 31 terminals within a range of 300 metres. Up to four terminals can converse simultaneously, while the exchange of data packets is allowed at the same time.

Interconnection of terminals is via a simple, easy to install, single twisted-pair cable. Terminals can be connected and disconnected at any time provided that the total number connected does not exceed 31. Only administration information should be kept on the identification number of a terminal.

If a wider communication range is required it is possible to gate data paths via a "gateway" to other networks, especially a gateway to the ISDN S reference point (note 1). The 8 kHz synchronous frame of the IST bus could be synchronized in the gateway to an 8 kHz external source.

The protocol on the IST bus is completely distributed along the members of the bus. There is no central bus controller. This ensures a reliable bus system because even if a terminal fails the communication between others will not be disturbed.

The IST bus is mainly optimized for voice communication and offers eight 64 kbit/s circuit-switched channels (b1 to b8), time multiplexed on an 8 kHz frame structure. The protocol to access one of these channels is distributed along the terminals connected on the bus. Each terminal could access arbitrarily one or more of these circuit-switched channels. A 64 kbit/s packet-switched data channel (bd) is provided next to these eight circuit-switched channels. The bd channel is the IST equivalent of the ISDN "D" channel. The b1 to b8 channels are the IST equivalent of the ISDN "B" channels.

Layers 1 and 2 of the 7-layer hierarchy of the Open Systems Interconnection (OSI) model developed by the International Standardization Organization (ISO) built on this packet-switched channel are specified. Layer 2 offers a datagram service (note 2) with error free transmission of data packets and flow control. The access mechanism to this channel is the slotted CSMA/CD protocol (note 3). With this protocol access is guaranteed even with a 100% load. This makes the IST bus also suitable for process control.

The IBI, an IST Bus Interface (PCB2310) is a VLSI circuit which offers the complete protocols for the b channels and the protocol up to layer 2 for the data channel. The coupling to the bus will be achieved with a simple transformer.

Notes to the Introduction

1. The ISDN reference point has been specified by the CCITT in recommendations I430, I440 and I450.
2. A datagram service is a connectionless service specified by ISO; see also section 3.0.
3. CSMA/CD is Carrier Sense Multiple Access with Collision Detection. If a collision occurs terminals are allowed to transmit only in specific time slots. See bd access mechanism.

2.0 LAYER 1 CHARACTERISTICS

2.1 Configuration and definitions

It is possible to connect up to 31 terminals on the IST bus. One or more terminals could have connections to other networks, these terminals are called gateways. A terminal could be any equipment with the facility to communicate digital information to other equipment, e.g.

- digital voice communication : telephone, intercom
- digital data communication : computers, printers, telex, alarm indicators, slow scan television

Physically the interface of the IST bus is a twisted-pair cable leading to all terminals. A digital transmission technique is used for the transfer of data.

Logically the IST bus defines a set of protocols. These protocols specify the distribution of the transmission capability among the connected terminals.

The connection of terminals on the IST bus is limited by the distance between connected terminals being not less than 2 metres. Connection is achieved via a cord with a maximum length of 5 metres and a transformer. Each terminal must have a unique number between 1 and 31.

Because the IST bus is a twisted-pair cable and the voltage on the line is less then 1,25 V, pick-up and emission of radiated interference is minimal.

It is possible to distribute phantom power accross the interface using the same leads that are used for the data transmission due to the fact that the Alternative Mark Inversion (AMI) line code has been used. The voltage must be less than 42,5 V in accordance IEC safety regulations.

A configuration of the IST bus is shown in Fig. 1.

2.2 Input impedance (Z_I)

Because terminals are connected as stubs along the line the input impedance must be such that when 31 terminals are connected digital transmission are not disturbed.

The real part of the impedance should be such that if 31 terminals are located close together the reflections caused by these terminals are less than 10% at 500 kHz.

DC decoupling capacitors should be larger than 1 μF.

2.3 Line characteristics

A twisted pair of cables should be used.
Characteristic impedance must be in the range:

$$Z_O = 75 \text{ to } 150\ \Omega$$

Correct matching of the line is achieved when the terminating resistance is:

$$R_T = Z_O \pm 2\%$$

The round trip propagation delay must be:

$$T_d < 3000 \text{ ns}$$

And the maximum attenuation is:

$$A = 20^{10}\log V_I/V_O < 6 \text{ dB (f = 500 kHz)}$$

2.4 Isolation

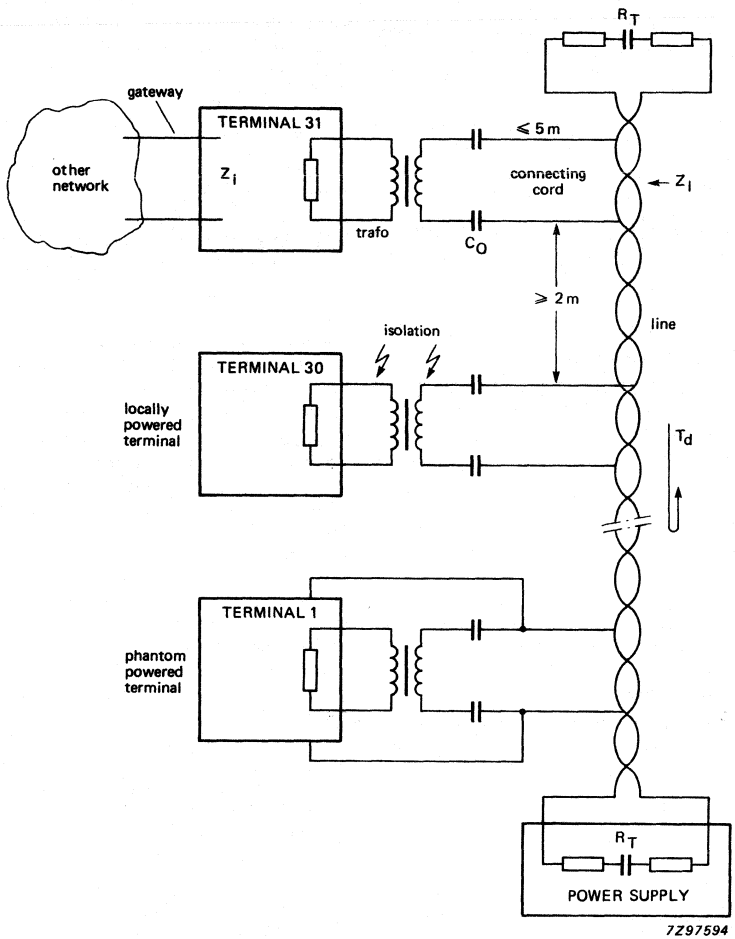
The isolation specified here is suitable for in-house systems.

A locally powered terminal must have a security isolation of more then 1500 V.

Terminals should withstand:

- Common mode voltage surge with:
  amplitude = 500 V
  rise time = 1 μs
  fall time = 1000 μs
  The source impedance is 0,015 μF
- Differential mode voltage/current surge with:
  amplitude = 50 V
  rise time = 1 μs
  fall time = 50 μs
  The source impedance has a current limit of 200 mA

DEVELOPMENT DATA



Where:

R_T = terminating resistance.
C_O = decoupling capacitance.
Z_l = input impedance as seen from the line into the cord.
isolation = isolation is defined as between the terminal and the line. The isolation defined is suitable for in-house systems.
T_d = round trip propagation delay.

Fig. 1 IST bus configuration.

2.5 Line signal

The line code is Alternative Mark Inversion. A logic 1 will result in a positive or a negative pulse on the line. A logic 0 will result in no signal on the line.

The nominal output voltage will be 1100 mV ± 150 mV into 50 Ω using the test configuration shown in Fig. 2.

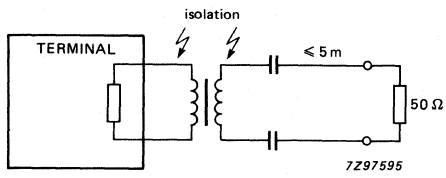


Fig. 2 Test configuration.

The bit rate is 1,024 kbits/s ± 100 ppm; based on an 8,192 kHz ± 100 ppm crystal.

The difference between the positive and the negative pulse should be less than:

$$\int \frac{\text{positive pulse}}{\text{negative pulse}} dt < 5\%$$

2.6 Noise immunity

The receiver must have a noise immunity to an input signal of 70 mV rms and below when f = 0 to 1 MHz.

2.7 Receiver input sensitivity

The receiver must handle input pulses as shown by the limits in Fig. 3. This also puts constraints on the transmitter output pulse.

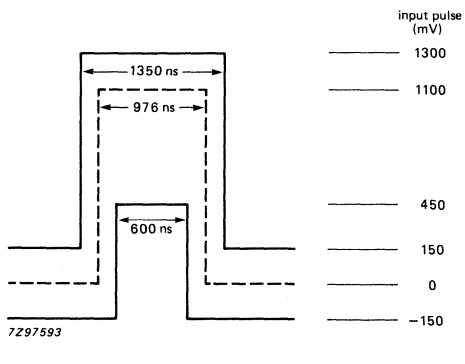


Fig. 3 Receiver input pulse mask limits.

2.8 Phantom power supply

Because the power spectrum of the AMI line code is zero for DC it is possible to distribute phantom power over the signal lines. The power supply of 42,5 V (max.) should not disturb the IST bus. The power available at the terminal is 400 to 600 mW and a maximum of 5 to 10 terminals could be powered. Connecting a terminal to the IST bus could cause the system to go down for some milli seconds.

2.9 Frame structure

A frame of 125 μs ± 122 ns contains ten time division multiplexed channels as shown in Fig. 4:

- 1 x 32 kbit/s synchronization channel ; Frame (F)
- 1 x 64 kbit/s packet-switched channel ; Data (bd)
- 8 x 64 kbit/s circuit-switched channels ; Data/voice (b1 to b8)

Each channel is preceded by an occupied bit which is logic 1 if the channel is occupied (this will result in a positive or a negative line signal). Due to line delays and synchronization a 4 μs shift in the bd and b1 to b8 channels is allowed; 0,5 μs is used as channel separation.

After power up one of the connected terminals should always transmit in the frame channel. The frame signal is coded "0011". The frame channel is used to synchronize all terminals to the 8 kHz frame. The terminal transmitting in the frame channel is the master and the others are the slaves. A fully distributed algorithm called master/slave arbitration determines which terminal will become the master. If a master fails another will automatically take over. One of the terminals connected to another network will always become the master of the IST bus. This terminal could be synchronized with that other network, but this can cause a jitter of 122 ns in the frame. The master/slave procedure is shown in Fig. 7 and Fig. 8.

If a gateway terminal connected to the IST bus is not master it will transmit a broadcast control message called "TOM". The current master will cease transmission in the frame channel as soon as all circuit-switched channels are free and the master/slave procedure restarts.

With a "TRM" primitive a terminal could request frame channel switch-off (after all circuit switched-channels are released) to enable terminal disconnection from the IST bus. A BUS_DOWN, BUS_UP primitive sequence (master) and a BUS_UP primitive (slave) indicates that another terminal is the master of the IST bus.

DEVELOPMENT DATA

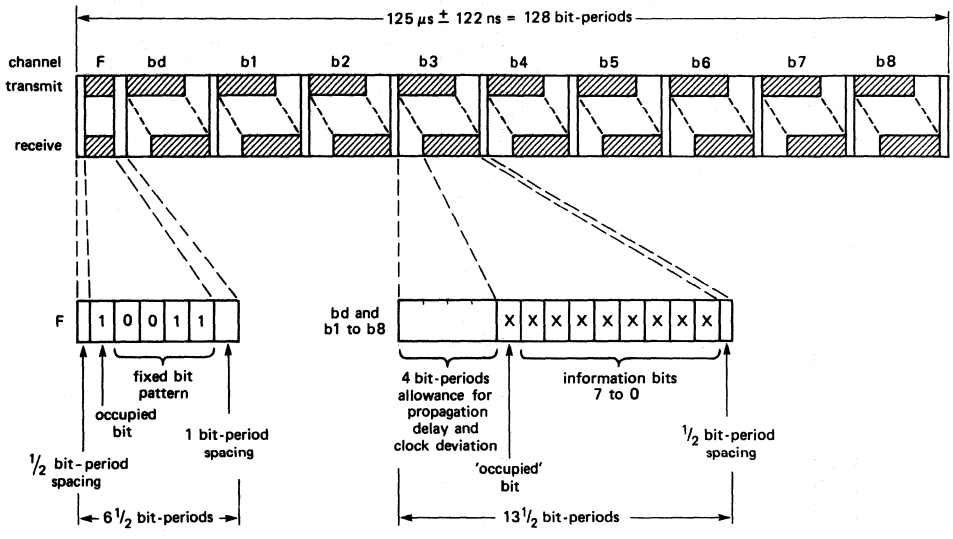
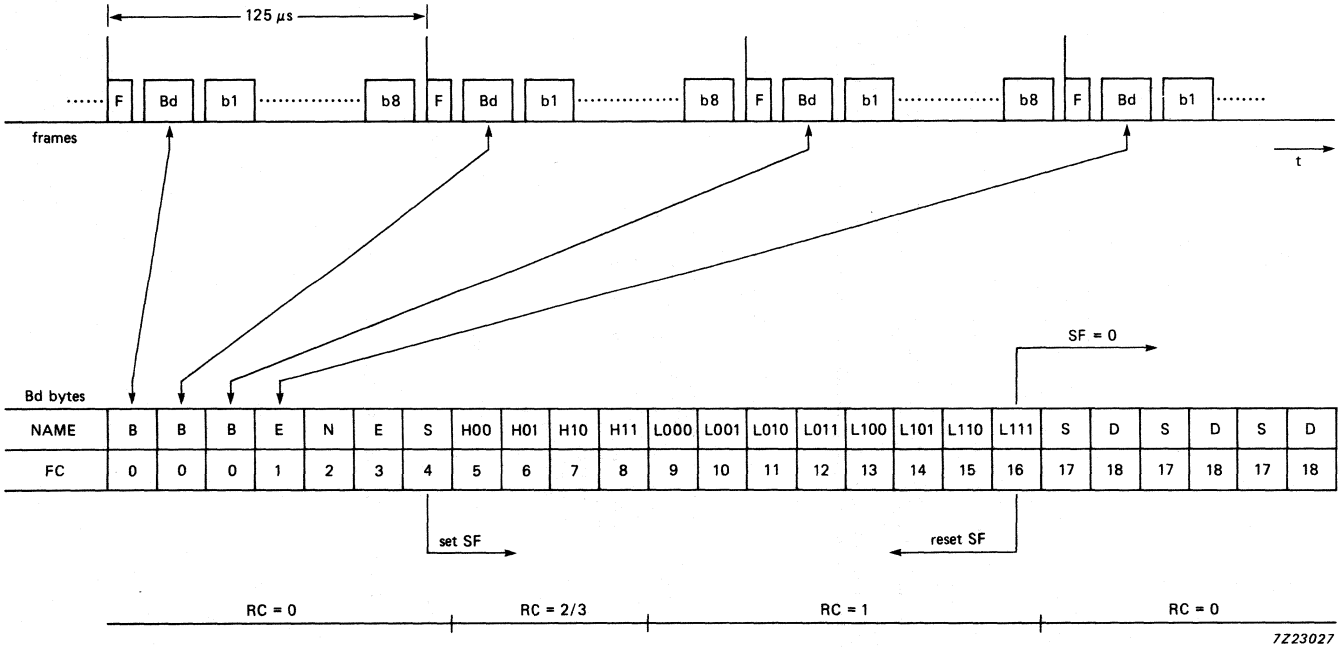


Fig. 4(a) Channel frame structure.



B = busy frame
E = empty frame
N = $\overline{ACK}$
S = frame in which an "s" message may start if SF = logic 0
D = frame in which "d" message may start

FC = frame counter
RC = retransmission counter
SF = "s" message flag
H00 to H11 = frames in which retransmissions may start if RC = 2 or RC = 3
L000 to L111 = frames in which retransmissions may start if RC = 1

Fig. 4(b) bd channel protocol principle.

2.10 Frame alignment

A terminal should recognize the frame signal three consecutive frames before they are synchronized (in-lock). When a synchronized terminal fails to recognize the frame signal for three consecutive frames the terminal is unsynchronized again (out-of-lock). A terminal is only allowed to transmit in one of the bd and/or b1 to b8 channels when synchronized.

2.11 bd access protocol

There are 3 types of message:

- "c" type; control message
- "d" type; data message
- "s" type; signalling message.

Access is determined such that terminals transmitting a "c" type or "s" type message have priority over terminals wanting to transmit "d" type messages. If a terminal has to transmit a "c" and an "s" type message the "c" type has priority. If a collision occurs between messages of the same type, the terminal number is decisive. Collided messages take priority over new messages to guarantee fair access. The terminal number is split into two parts to minimize access times. Table 1 illustrates the priority scheme.

Table 1 Access protocol priority scheme

priority	message	terminal
1	collided "c" or "s"	high number low number
2	new "c" or "s"	–
3	collided "d"	high number low number
4	new "d"	–

To access the bd channel the IST bus uses the CSMA/CD access protocol. The protocol of layer 2 for transmission of "s" and "d" messages is shown in the SDL diagrams, (Figs 9 to 12). The protocol treats "c" messages as "s" messages. In the IBI "s" and "c" messages have priority. The main part of the protocol is the bd channel access system and the frame-counter is closely related to this mechanism. Both of these mechanisms are illustrated in Fig.4(b).

Every IBI includes the frame-counter (FC) which is synchronized at the end of a packet transport in the bd channel whenever the bus is occupied. The frame indicated with B, E, N, S, H00 to H11, L000 to L111 and D have dedicated meanings as shown in Fig.4(b). The end of a packet transport is indicated by a frame in which the bd channel carries no start or information bits, i.e. an EMPTY frame (E). The frame that follows the E frame is the $\overline{\text{ACK}}$ (N) frame. In this frame stations may transmit the not acknowledge code, 11111111. This code is used if retransmission is required due to transmission errors, collisions or destination receive buffers full. If the $\overline{\text{ACK}}$ code is not needed the frame remains empty.

For circuit implementation reasons the N frame is followed by another E frame. After this first tine messages may access the bd channel in the S frame is SF = logic 0. SF is set to logic 1 if a transport is started in this frame. The 12 frames H00 to H11 and L000 to L111 are intended for retransmission purposes. In this field both signalling and data packets may start if SF = logic 0. If SF = logic 1 only signalling packets may access and data packets must wait for SF = logic 0 to occur.

If the ACK signal appears in the N frame the retransmission counters (RC) of the colliding terminals are increased. Depending on the 3 least significant bits of the 5 bit IST bus terminal address retransmissions will start in frames L000 to L111 when RC = 1. It is still possible that up to 4 stations can collide in this first retransmission period. Stations affected will start a second retransmission in the frames H00 to H11 (RC = 2) depending on the 2 most significant bits of the station's address. During the second retransmission period collisions cannot occur because the involved stations have different address bits.

Reception of $\overline{\text{ACK}}$ however is still possible during this second retransmission period, occuring due to noise or inability of the buffer to accommodate the new packet, in order to distinguish between these 2 conditions the transmission is repeated once more in frames H00 to H11 (RC = 3). If after this $\overline{\text{ACK}}$ is again received it is concluded that the receiving station was unable to store the packet. The transmitting chip will then warn its controller with a transmission overflow message. With the exception of frame control messages, (which only deal with layer 1), the transmitting chip confirms the transmission of all error free transfers with its controller.

The internal frame-counter is returned to the E position (FC = 3) in frame L111, if SF = logic 1 or access occurs during this frame, in order to give waiting data packets a retransmission chance. SF is reset at this time.

If during frame L111 SF = logic 0 and no access occurs, the internal frame-counters continue with S and D frames sequentially. First time signalling and data packets may start during these frames. This is also the normal access routine when the bd channel has been idle for some time. The S and D frames prevent collision between signalling and data packets.

2.12 b channel access protocol

The b channel access protocol is fully decentralized. All members along the IST bus have the same algorithm. Each terminal is free to occupy any number of b channels provided they are not occupied by another terminal. b channels are not in pairs. To determine which terminal is allowed to access a b channel the access mechanism of the bd channel is used. If a terminal want to access a free b channel, it transmits a unique broadcast control message in the bd channel. This control message is called "OCP". After a successful transfer the terminal is allowed to access the first free b channel. A b channel is **free** if the occupied bit of that channel is logic 0 for at least **two consecutive frames** directly after the control message has been correctly transferred.

The availability of "enquiry or call transfer" is made possible by ordering a terminal to occupy a b channel directly after that specific b channel has been released. A channel is seen **released** if its occupied bit is logic 0 for at least **one frame.**

3.0 LAYER 2 PROTOCOL FOR THE bd CHANNEL

3.1 Service

The service offered by the layer 2 protocol for the bd channel is a packet-switched datagram service. This means it is not necessary to set up a logical link before being able to transfer data packets. Layer 3 data is transferred transparantly by the layer 2 service. Two types of data packets can be transferred:

- "s" type packets for control of circuit-switched channels
- "d" type packets for data packet exchange between terminals

The average transfer delay of "s" types packets is less than that of "d" type packets due to the bd access protocol. The layer 2 message is controlled with a Cyclic Redundancy Check (CRC). If a message is received wrongly it will be retransmitted. Thus an error-free packet transmission can be guaranteed on an erroneous channel. Flow control is possible because a receiver can reject a data packet.

3.2 Protocol

Packets are separated by at least one empty byte. An occupied bit at logic 0 in the bd channel indicates an empty byte. In the packet the occupied bit is set to logic 1 to ensure transparency as shown in Fig. 5.
Each packet will be immediately rejected two frames after the transmission if:

- the calculated CRC in the receiver differs from the received CRC

or

- a receiver is not able to receive the message because of pending messages

If a packet is rejected a not acknowledge ($\overline{ACK}$) will be transferred immediately after the message.
The transmitter will then re-transmit its message in accordance with the bd access protocol. A rejection instead of an acknowledgement has been choosen because broadcast messages can be similarly rejected ("wired NOR"). However, a transmitter cannot detect whether a non-existing or a non-responding terminal has been addressed.

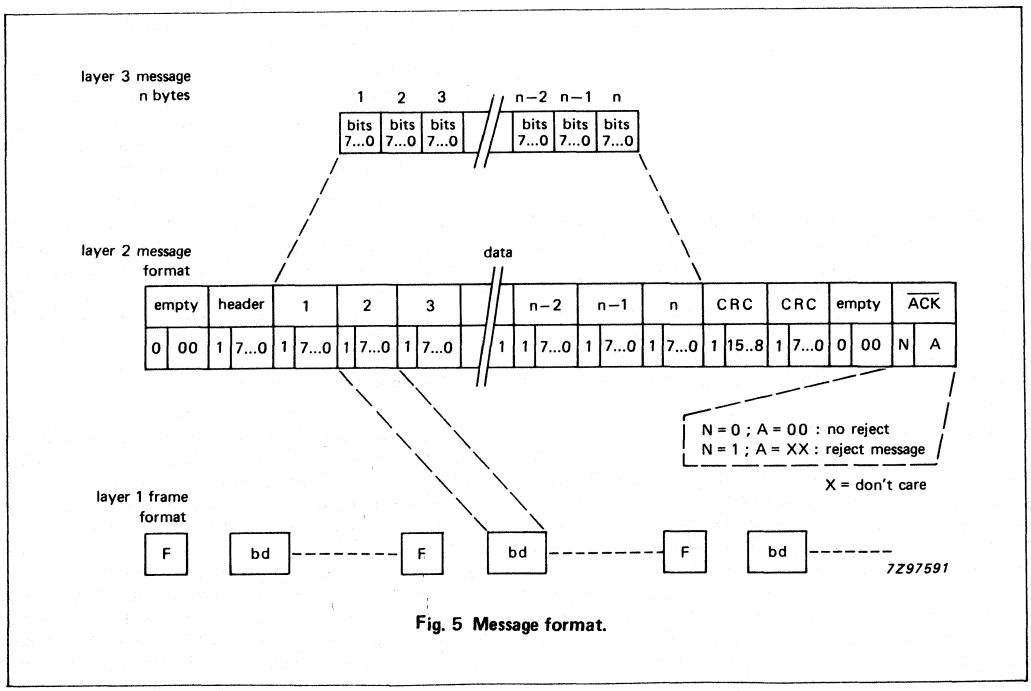


Fig. 5 Message format.

The trailer contains the 16-bit CRC. The CRC operation is a division of the complete layer 2 packet including the header. The divider is:

$$X^{16} + X^{12} + X^5 + 1$$

and the initial remainder is "00".
The final remainder of the division will be transmitted in the two CRC bytes.

The header distinguishes the three types of messages:

- "c" or control type used for control over the frame and b channels
- "d" type which can transfer any kind of data
- "s" signalling type used for routing etc.

The "s" and "d" type messages can address any specified terminal or all terminals (broadcast message). The "c" type messages address all terminals. Table 2 displays an overview of the bits in the header.

3.3 Maintenance

Five control messages are used on the IST bus:

- The "OCP" message is used to control the b channel access and is unique for each terminal because of the terminal number in the header
- The "TOM" message is used to control the frame channel (see master/slave arbitration)
- The "AFS", "SAS" and the "SCO" messages are used to control the external synchronization procedures (see Figs 12 and 13)

If a terminal wants to communicate to another network via a gateway it can ask the IST bus to synchronize with the external 8 kHz source of that network. This procedure is initiated by an EXTERNAL_SYNC_REQUEST (ESR) primitive. If the terminal is not the master on the IST bus it will transmit an "SAS" control message in the bd channel. The gateway terminal will receive an EXTERNAL_SYNC WANTED (ESW) upon receipt of an "SAS" message. If the external synchronization is established the "SCO" control message will be transferred to the bd channel and when received an EXTERNAL_SYNC_IS_ON (ESO) primitive is given.

If the gateway wants to cease the external synchronization it issues an EXTERNAL_SYNC_RELEASE_REQUEST (RES); the "AFS" control message is transferred and all terminals will receive an RELEASE_EXTERNAL_SYNC_PROCEEDS (RSP). If there is no reaction within 8 seconds from other members on the IST bus the master releases the external synchronization.

The following other maintenance services are offered to the layer 3:

- If there is no signal on the IST bus a BUS_DOWN_INDICATION (TMP) primitive is given
- When a signal reappears on the IST bus a BUS_UP_INDICATION (TMF) primitive is given
- If the transfer of an "s" or "d" type message is failed an s_FAILURE_INDICATION (FAILURE) or a d_FAILURE_INDICATION (FAILURE) is given

A transfer is failed if a reject is still received after 3 retransmissions.

- If a transfer is successful an s_SUCCESS_INDICATION (SUCCESSFUL) or a d_SUCCESS_INDICATION (SUCCESSFUL) primitive is given.

Table 2 Header format

	bit								type	
	7	6	5	4	3	2	1	0		
control messages	1	1	X	terminal number(n)					OCP	(occupation of b-channel will proceed)
zero data bits		0	0	0	0	0	0	1	TOM	(transfer of master request)
				0	0	0	1	0	AFS	(ask/give permission to finish synchronization)
				0	0	0	1	1	SAS	(slave asks for synchronization)
				0	0	1	0	0	SCO	(synchronization is ON)
signalling messages	0	1	X	destination address*					"s"	
data messages	0	0	X	destination address*					"d"	

Where:

X = don't care
* = all zeros indicate the broadcast address

DEVELOPMENT DATA

4.0 LAYER 3 OF THE bd CHANNEL

To be specified.

DEVELOPMENT DATA

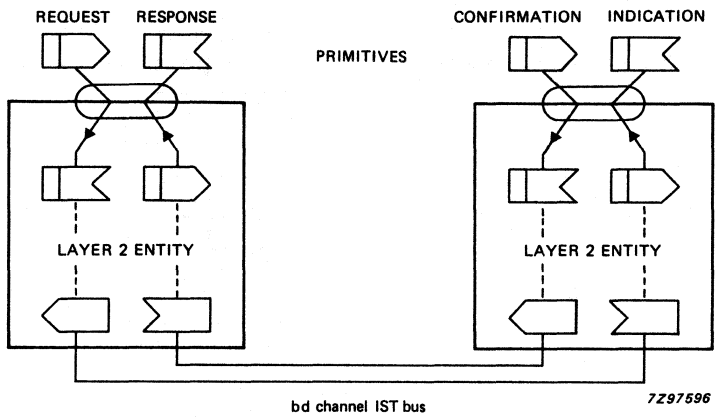
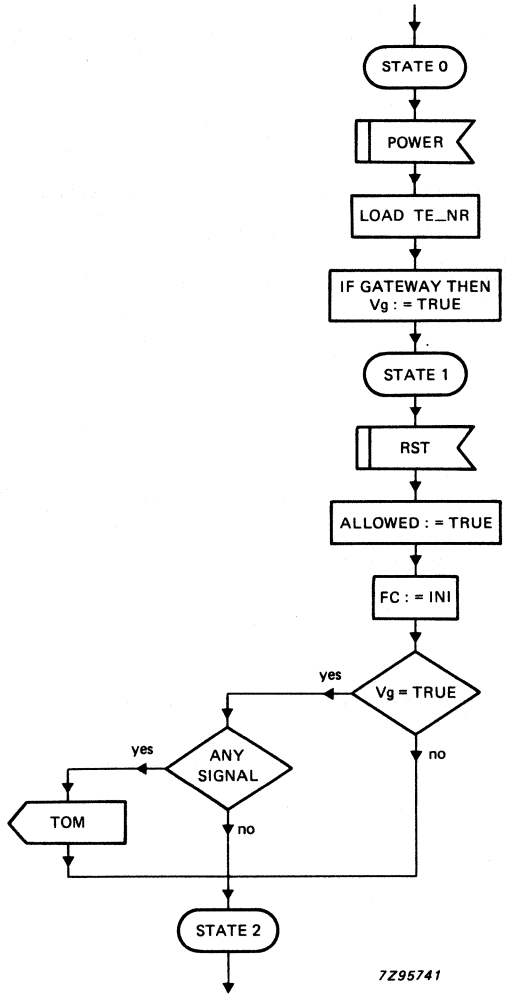


Fig. 6 SDL diagram; primitive definitions.



FC = frame counter
INI = initialization
RST = reset
TE_NR = terminal number

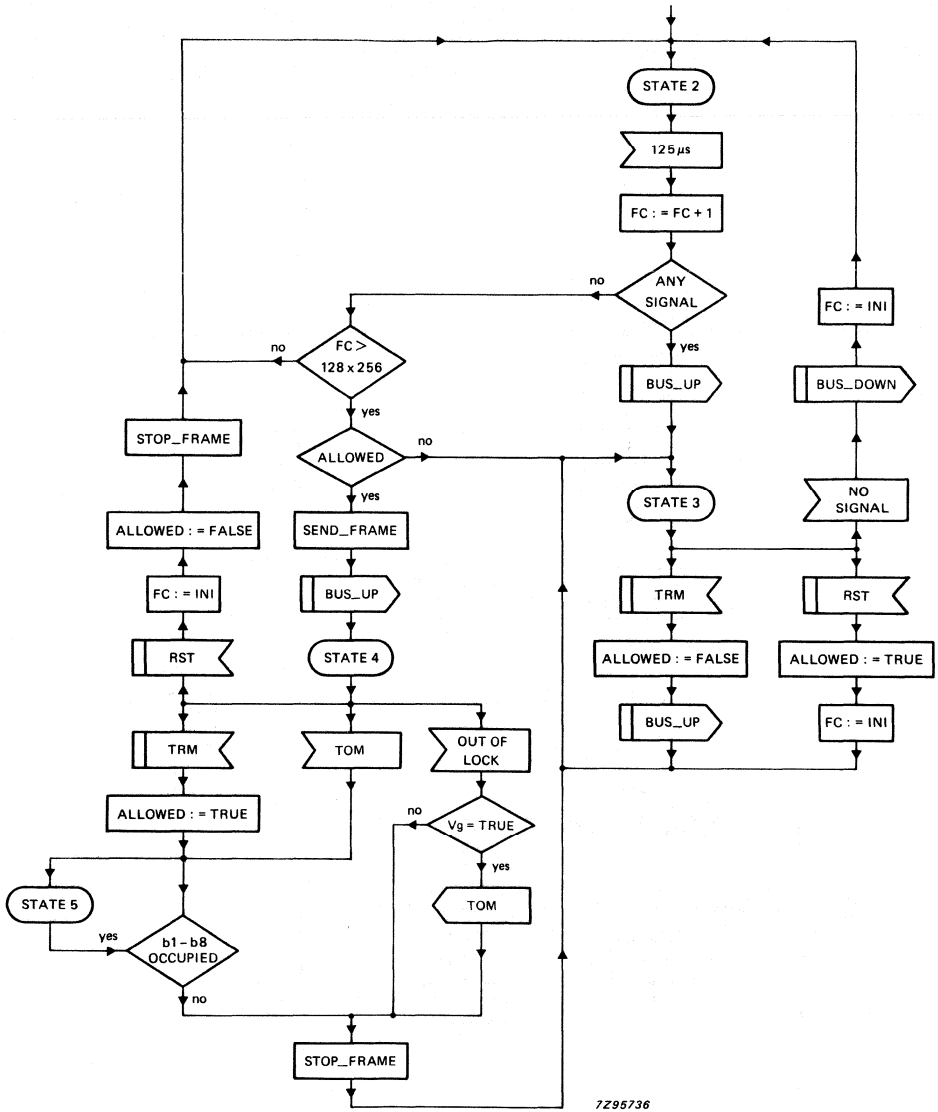
Where

At initialization the frame counter will be:

INI: = (Vg x 64 + TE_NR) x 256

Fig. 7 Master/slave arbitration; part 1.

DEVELOPMENT DATA

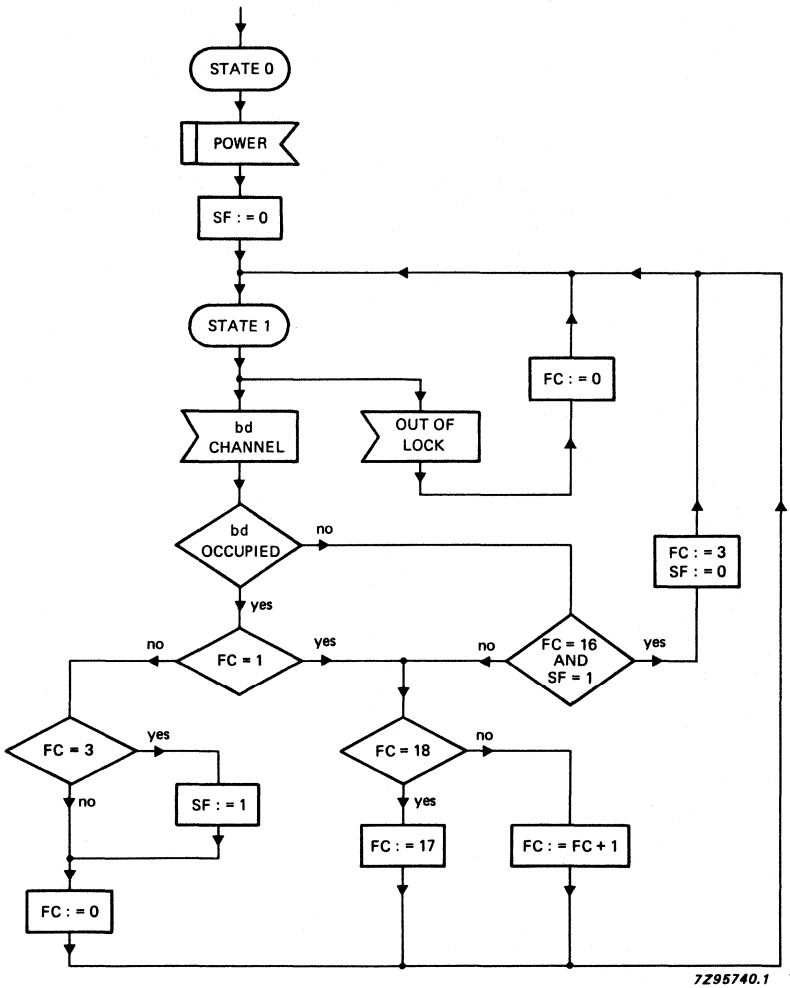


Where

SEND_FRAME: occupy frame channel and transmit "0011"
STOP_FRAME: release frame channel

FC = frame counter
INI = initialization
RST = reset

Fig. 8 Master/slave arbitration; part 2.

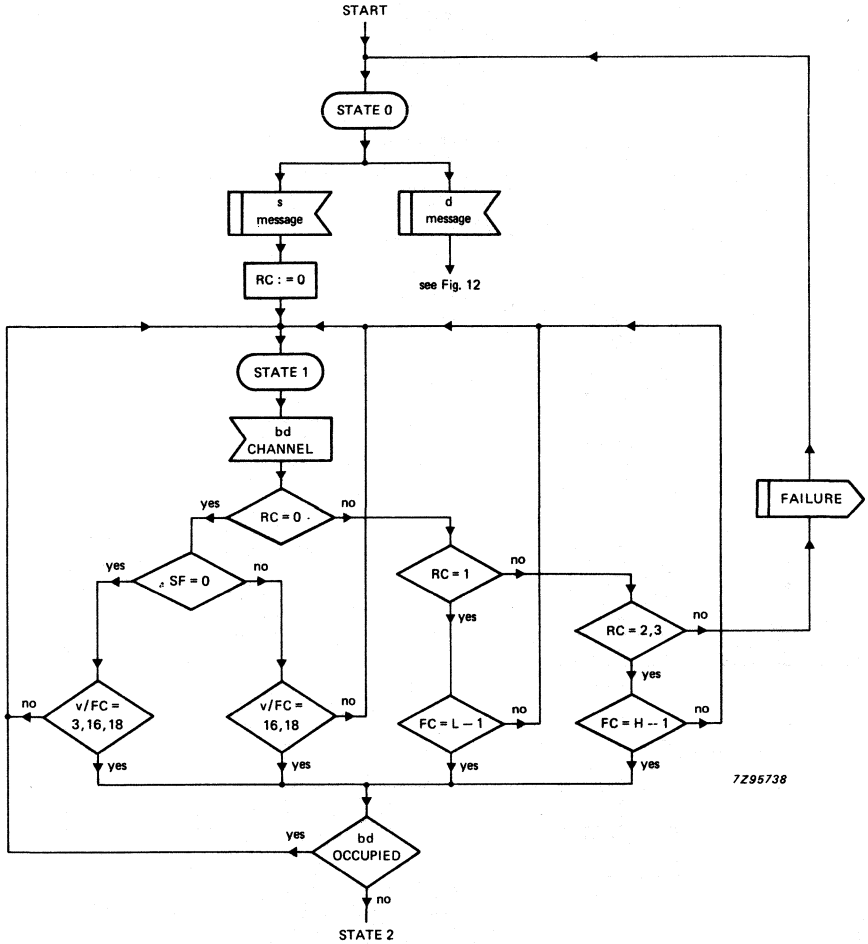


Where

FC = frame counter
SF = "s" message flag

Fig. 9 bd channel access; frame counter.

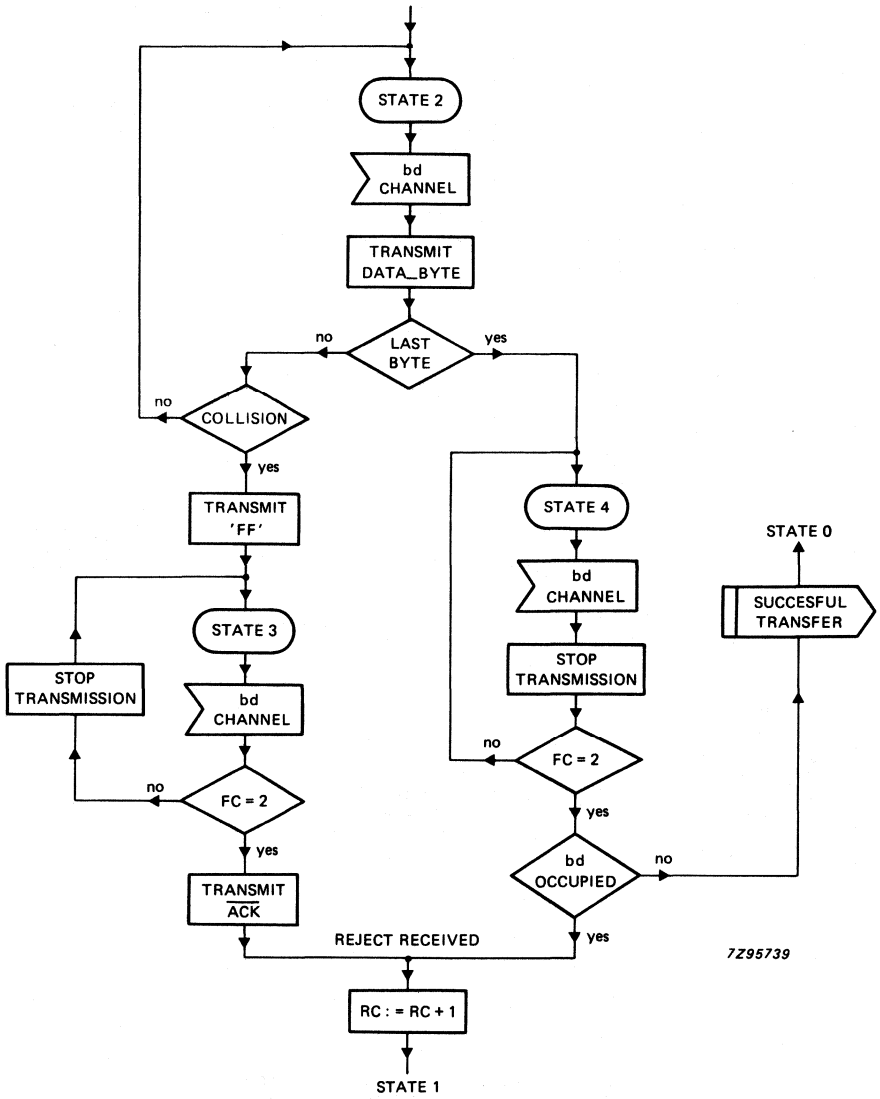
DEVELOPMENT DATA



Where

L = 9 + decimal value of low order 3 bits of TE_NR
H = 5 + decimal value of high order 2 bits of TE_NR
FC = frame counter
RC = retransmission counter
SF = "s" message flag

Fig. 10 bd channel access mechanism; part 1.

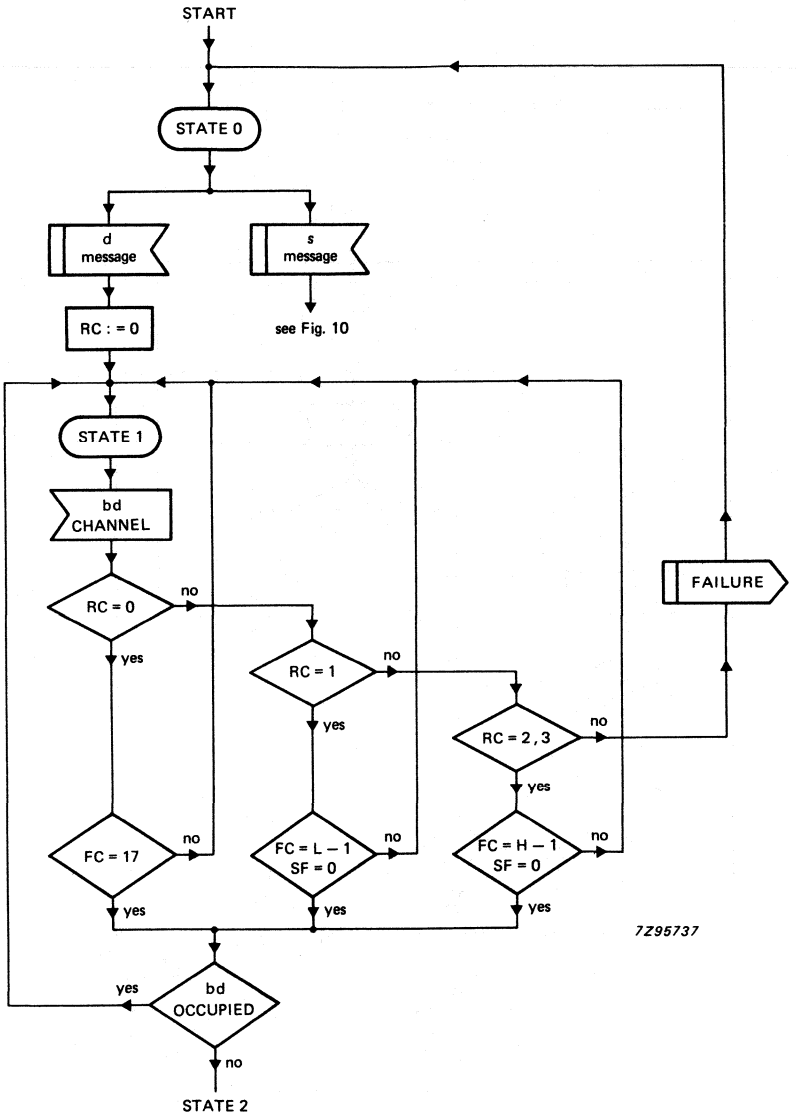


Where

FC = frame counter
RC = retransmission counter

Fig. 11 bd channel access mechanism; part 2.

DEVELOPMENT DATA



Where

L = 9 + decimal value of low order 3 bits of TE_NR
H = 5 + decimal value of high order 2 bits of TE_NR
FC = frame counter
RC = retransmission counter
SF = "s" message flag

Fig. 12 bd channel access mechanism; part 3.

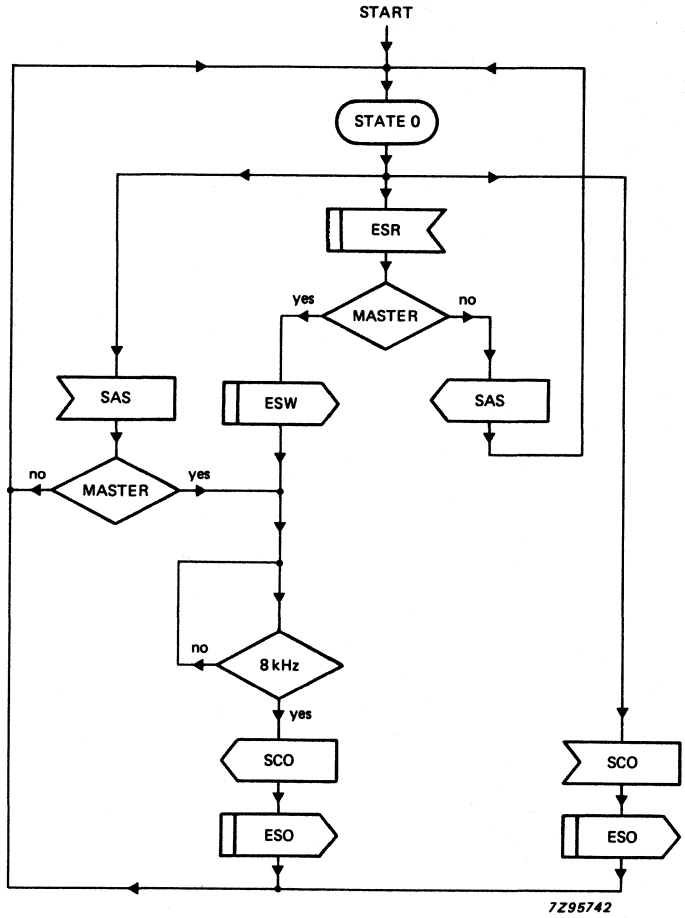


Fig. 13 External synchronization; establishment procedure.

DEVELOPMENT DATA

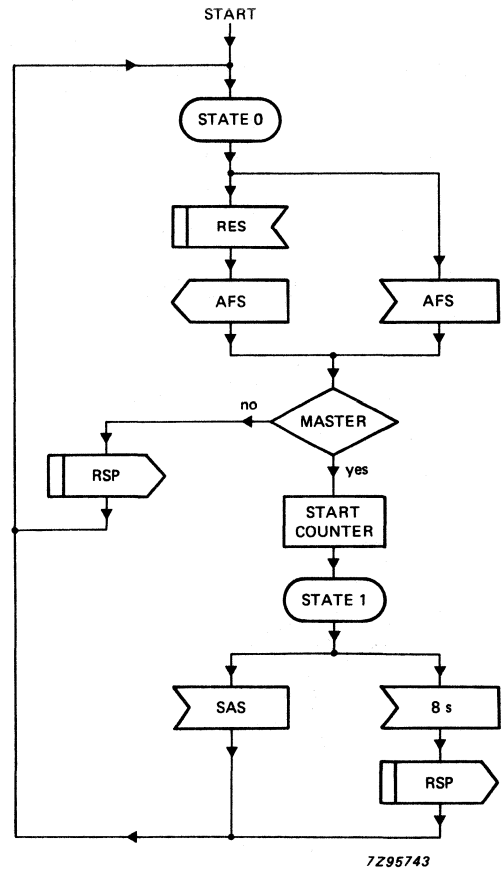


Fig. 14 External synchronization; release procedure.

NE570/571/SA571
Compandor

Product Specification

Linear Products

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full-wave rectifier to detect the average value of the signal, a linerarized temperature-compensated variable gain cell, and an operational amplifier.

The NE570/571 is well suited for use in cellular radio and radio communications systems, modems, telephone, and satellite broadcast/receive audio systems.

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full-wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full-wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively-coupled voltage inputs as shown in the following equation. Note that for capacitively-coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than 0.1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|avg}{R_1}$$

or

$$G \propto \frac{|V_{IN}|avg}{R_1}$$

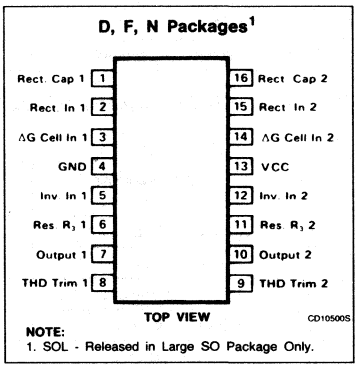
FEATURES

- **Complete compressor and expandor in one IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to $6V_{DC}$**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Cellular radio**
- **Telephone trunk compandor — 570**
- **Telephone subscriber compandor — 571**
- **High level limiter**
- **Low level expandor — noise gate**
- **Dynamic noise reduction systems**
- **Voltage-controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

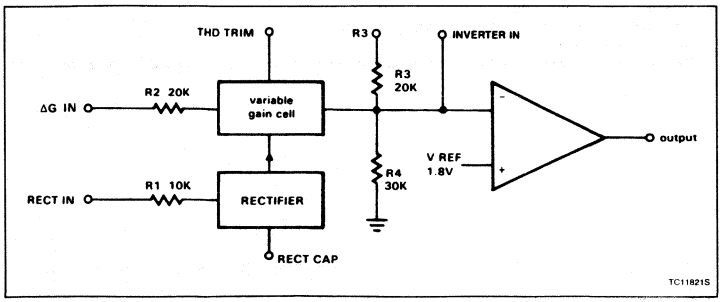


NOTE:
1. SOL - Released in Large SO Package Only.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Cerdip	0 to +70°C	NE570F
16-Pin Plastic DIP	0 to +70°C	NE570N
16-Pin Plastic SOL	0 to +70°C	NE571D
16-Pin Cerdip	0 to +70°C	NE571F
16-Pin Plastic Cerdip	0 to +70°C	NE571N
16-Pin Cerdip	-40°C to +85°C	SA571F
16-Pin Plastic DIP	-40°C to +85°C	SA571N

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Positive supply 570 571	 24 18	V_{DC}
T_A	Operating ambient temperature range NE SA	 0 to +70 −40 to +85	 °C °C
P_D	Power dissipation	400	mW

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{CC} = 15V$. Except where indicated, the 571 specifications are identical to those of the 570.

SYMBOL	PARAMETER	TEST CONDITIONS	NE570			NE/SA571[5]			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		6		24	6		18	V
I_{CC}	Supply current	No signal		3.2	4.8		3.2	4.8	mA
I_{OUT}	Output current capability		±20			±20			mA
SR	Output slew rate			±.5			±.5		V/μs
	Gain cell distortion[2]	Untrimmed Trimmed		0.3 0.05	1.0		0.5 0.1	2.0	%
	Resistor tolerance			±5	±15		±5	±15	%
	Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
	Output DC shift[3]	Untrimmed		±20	±50		±30	±100	mV
	Expandor output noise	No signal, 15Hz − 20kHz[1]		20	45		20	60	μV
	Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
	Gain change[2, 4]	−40°C < T < 70°C 0°C < T < 70°C		±0.1 ±0.1	 ±0.2		±0.1 ±0.1	 ±0.4	dB
	Reference drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+2, −25 ±5	+10, −40 ±10		+2, −25 ±5	+20, −50 ±20	mV
	Resistor drift[4]	−40°C < T < 70°C 0°C < T < 70°C		+8, −0 +1.−0					%
	Tracking error (measured relative to value at unity gain) equals $[V_O - V_O$ (unity gain)] dB − V_2dBm	Rectifier input, $V_2 = +6dBm$, $V_1 = 0dB$ $V_2 = -30dBm$, $V_1 = 0dB$		±0.2 +0.2	 −0.5, +1		 +0.2	 −1, +1.5	dB
	Channel separation			60			60		dB

NOTES:
1. Input to V_1 and V_2 grounded.
2. Measured at 0dBm, 1kHz.
3. Expandor AC input change from no signal to 0dBm.
4. Relative to value at $T_A = 25°C$.
5. Electrical characteristics for the SA571 only are specified over −40 to +85°C temperature range.

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a trade-off to be made between fast attack and decay times and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\, e^{-t/\tau} + G_{final};\ \tau = 10k \times C_{RECT}$$

The variable gain cell is a current-in, current-out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively-coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

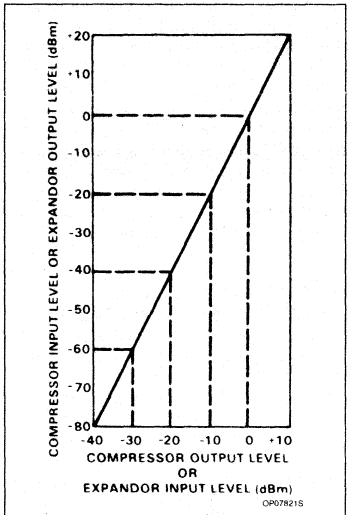
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

The output stage is capable of ± 20mA output current. This allows a +13dBm ($3.5V_{RMS}$) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

A bandgap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

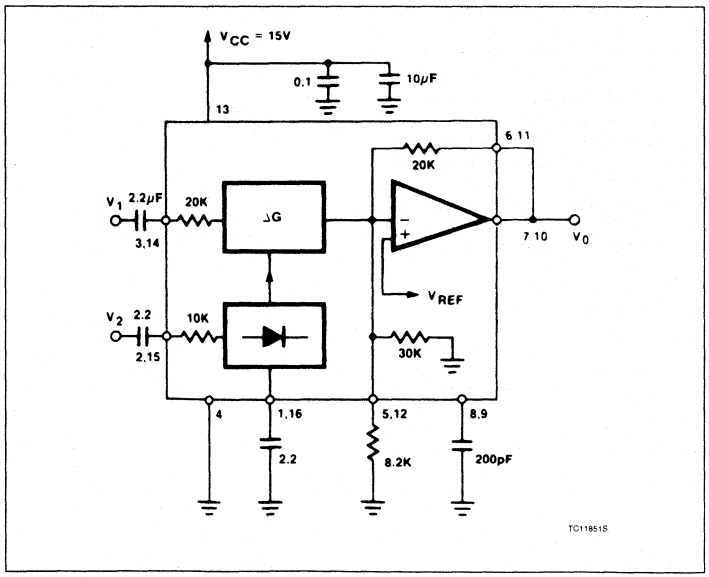
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



Basic Input-Output Transfer Curve

TYPICAL TEST CIRCUIT



INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high-performance is required, one has to resort to complex discrete circuitry with many expensive, well-matched components. This paper describes an inexpensive integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (< 0.1%), high signal-to-noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was originally designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal-to-noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal-to-noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2-to-1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full-wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. These features make the circuit useful in audio and data systems as well as in telecommunications systems.

BASIC CIRCUIT HOOK-UP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the IC). The full-wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output DC bias.

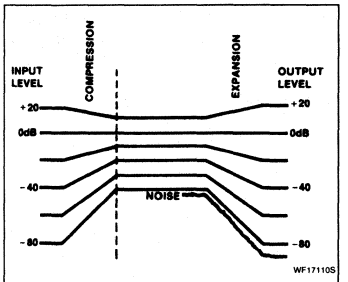


Figure 1. Restricted Dynamic Range Channel

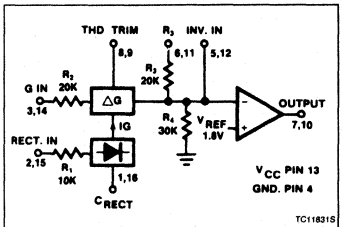


Figure 2. Chip Block Diagram (1 of 2 Channels)

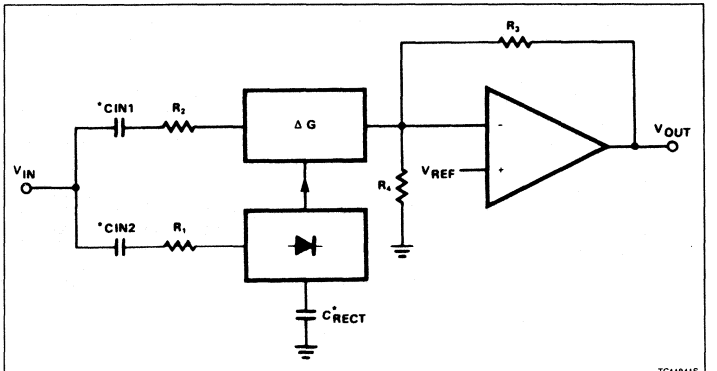
The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8V reference denoted V_{REF}. The non-inverting input of the op amp is tied to V_{REF}, and the summing nodes of the rectifier and ΔG cell (located at the right of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{REF} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{IN}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{OUT} will thus drop 12dB, giving us the desired 2-to-1 expansion.

Figure 4 shows the hook-up for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is setup to provide AC feedback only, so a separate DC feedback loop is provided by the two R_{DC} and C_{DC}. The values of R_{DC} will determine the DC bias at the output of the op amp. The output will bias to:

$$V_{OUT}\ DC = 1 + \frac{R_{DC1} + R_{DC2}}{R_4}$$

$$V_{REF} = \left(1 + \frac{R_{DC\ TOT}}{30k} \right) 1.8V$$



NOTES:

$$GAIN = \frac{2\ R_3\ V_{IN}\ (avg.)}{R_1\ R_2\ I_B}$$

$I_B = 140\mu A$

*External components

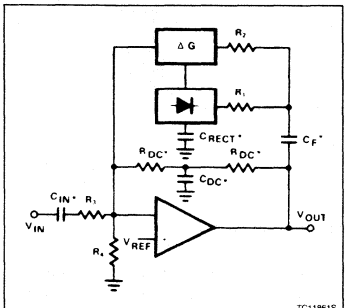
Figure 3. Basic Expandor

The output of the expandor will bias up to:

$$V_{OUT}\ DC = 1 + \frac{R_3}{R_4}\ V_{REF}$$

$$V_{REF} = \left(1 + \frac{20k}{30k} \right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the DC bias to any desired value.



NOTES:

$$GAIN = \left(\frac{R_1\ R_2\ I_B}{2\ R_3\ V_{IN}\ (avg)} \right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 4. Basic Compressor

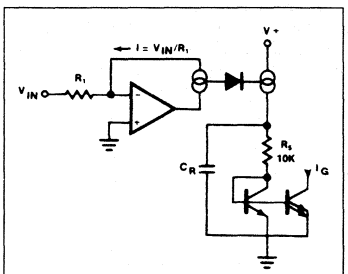
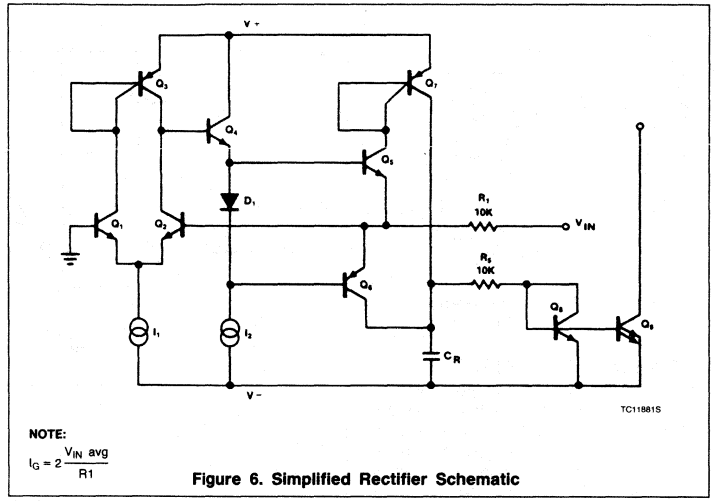


Figure 5. Rectifier Concept

CIRCUIT DETAILS — RECTIFIER

Figure 5 shows the concept behind the full-wave averaging rectifier. The input current to the summing node of the op amp, $V_{IN}R_1$, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, CR, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.



NOTE:

$$I_G = 2\frac{V_{IN}\ avg}{R1}$$

Figure 6. Simplified Rectifier Schematic

Figure 6 shows the rectifier circuit in more detail. The op amp is a one-stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{REF}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. ICs such as this have typical NPN βs of 200 and PNP βs of 40. The α's of 0.995 and 0.975 will produce errors of 0.5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere 0.13dB gain error.

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by DC coupling into the rectifier. If an offset voltage exists between the V_{IN} input pin and the base of Q_2, an error current of V_{OS}/R_1 will be generated. A mere 1mV of offset will cause an input current of 100nA which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the PNP Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μA. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

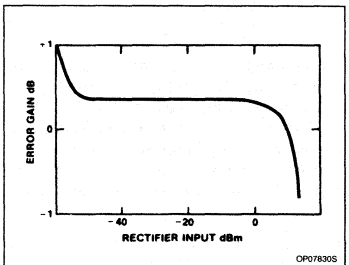


Figure 7. Rectifier Accuracy

At very high frequencies, the response of the rectifier will fall off. The roll-off will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

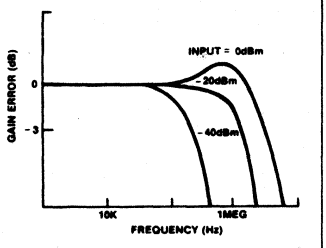


Figure 8. Rectifier Frequency Response vs Input Level

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two-quadrant transconductance multiplier. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3 and Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{REF}) by controlling the base of Q_2. The input current I_{IN} ($= V_{IN}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{IN}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is:

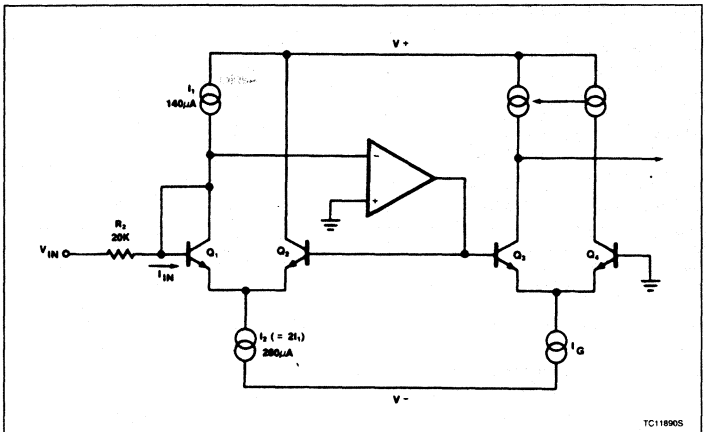
$$I_2 - (I_1 + I_{IN}) = I_1 - I_{IN} = I_{C2}.$$

The op amp has thus forced a linear current swing between Q_1 and Q_2 by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the non-linearity of the differential pair, Q_1 and Q_2, under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair, Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{IN}}{I_1 - I_{IN}}$$

plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{OUT} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,



NOTE:

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$$

Figure 9. Simplified ΔG Cell Schematic

$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{V_{IN}}{R_2} \frac{I_G}{I_1}.$$

This equation is linear and temperature-insensitive, but it assumes ideal transistors.

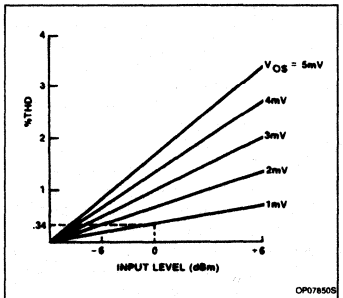


Figure 10. ΔG Cell Distortion vs Offset Voltage

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in second harmonic distortion. Figure 10 gives an indication of the magnitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mV offset will yield 0.34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about ½mV. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

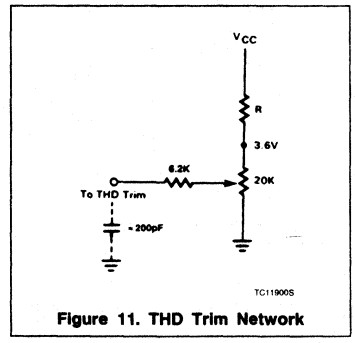


Figure 11. THD Trim Network

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feedthrough is generated in the gain cell by imperfect device matching and mismatches in the current sources, I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feedthrough, but in general, the null for minimum feedthrough will be different than the null in distortion. The control signal feedthrough can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

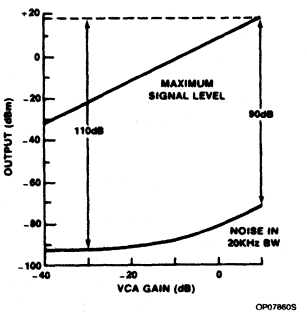


Figure 12. Dynamic Range of NE570

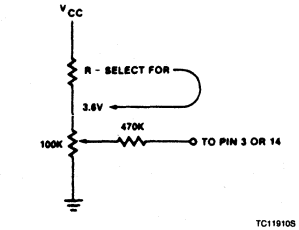


Figure 13. Control Signal Feedthrough Trim

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_M, so that a small compensation capacitor of just 10pF may be used. The output stage, although capable of output currents in excess of 20mA, is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

RESISTORS

Inspection of the gain equations in Figures 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hook-ups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion-implanted resistors which are used in this circuit. Over the critical 0°C to +70°C temperature range, there is a 10-to-1 improvement in drift from a 5% change for the diffused resistors, to a 0.5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

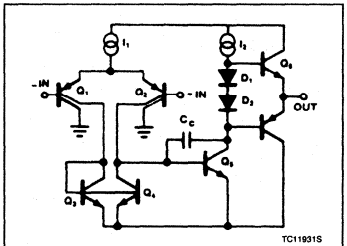


Figure 14. Operational Amplifier

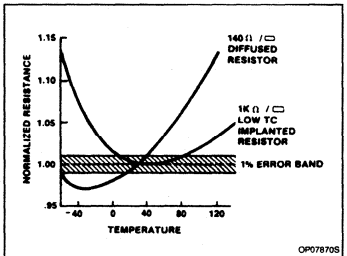


Figure 15. Resistance vs Temperature

NE575
Low Voltage Compandor

Preliminary Specification

Linear Products

DESCRIPTION

The NE575 is a dual gain-control circuit designed for low voltage applications. The NE575's channel 1 is an expandor, while channel 2 can be configured either for expandor, compressor, or automatic level controller (ALC) application.

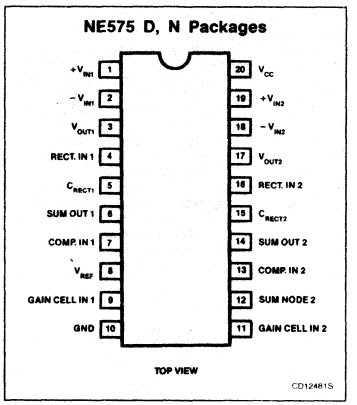
FEATURES

- **Operating voltage range from 3 to 7V**
- **Reference voltage of 100mV$_{RMS}$ = 0dB**
- **One dedicated summing op amp per channel and two extra uncommitted op amps**
- **600Ω drive capability**
- **Single or split supply operation**
- **Wide input/output swing capability.**

APPLICATIONS

- **Portable communications**
- **Cellular radio**
- **Cordless telephone**
- **Consumer audio**
- **Portable broadcast mixers**
- **Wireless microphones**
- **Modems**
- **Electric organs**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE575N
20-Pin Plastic SO	0 to +70°C	NE575D

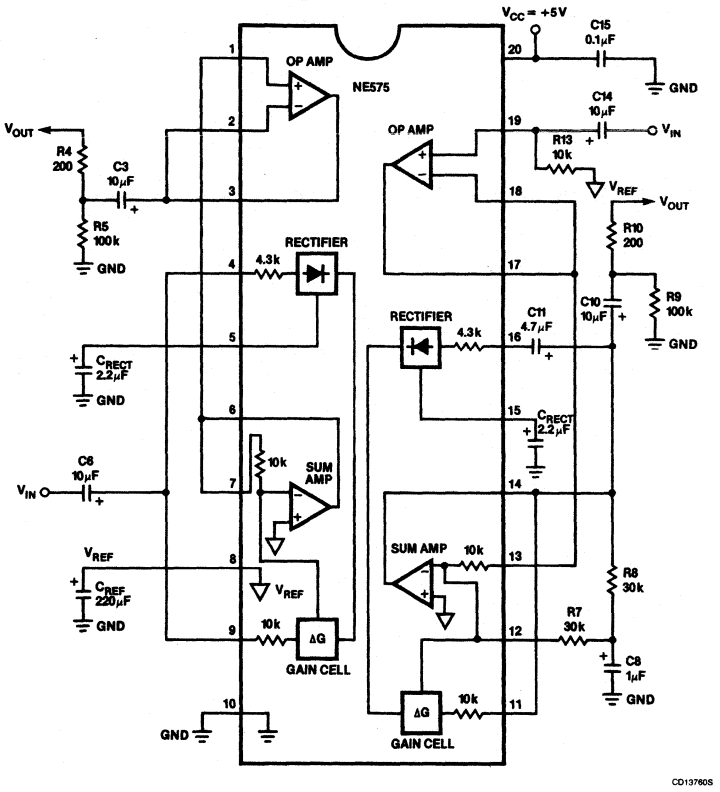
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	8	V
T_A	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, 0dB = 100mV, expander mode, V_{CC} = 5V, Figure 1, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
For compandor, including summing amplifier						
V_{CC}	Supply voltage[1]		3	5	7	V
I_{CC}	Supply current	No signal	3	4	5.5	mA
R_L	Summing amp output load		10			kΩ
THD	Total harmonic distortion	1kHz, 0dB, BW = 3.5kHz		0.13	1.0	%
eno	Output voltage noise	BW = 20kHz, R_S = 0Ω		6	20	μV
0dB	Unity gain level	1kHz	-1.0		1.0	dB
V_{OS}	Output voltage offset	no signal	-100		100	mV
	Output DC shift	no signal to 0dB	-50	10	50	mV
	Tracking error	1kHz, +6dB to -30dB	-0.5		+0.5	dB
	Crosstalk	1kHz, 0dB, C_{REF} = 220μF		-80	-65	dB
For operational amplifier						
V_O	Output swing	V_{P-P}, R_L = 10kΩ	V_{CC}-0.4	V_{CC}-0.2		V
R_L	Output load	1kHz	600			Ω
CMR	Input common-mode range		0		V_{CC}	V
CMRR	Common-mode rejection ratio		60	80		dB
I_B	Input bias current	V_{IN} = 0.5V - 4.5V	-0.3		0.3	μA
V_{OS}	Input offset voltage		-10	3	10	mV
A_{VOL}	Open-loop gain	R_L = 10kΩ	80	90		dB
SR	Slew rate	unity gain		1		V/μs
GBW	Bandwidth	unity gain		3		MHz
eni	Input voltage noise	BW = 20kHz		2.5		μV
PSRR	Power supply rejection ratio	1kHz, 250mV		60		dB

NOTE:
1. The IC remains functional down to 2V.



NOTE:
Left channel in expander mode; right channel in compressor mode.
For additional information, call the factory.

Figure 1. Typical Application

NE/SA602
Double-Balanced Mixer and Oscillator

Product Specification

Linear Products

DESCRIPTION

The SA/NE602 is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low power communication systems. The guaranteed parameters of the SA602 make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA/NE602 a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

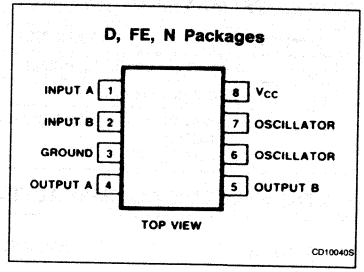
FEATURES

- **Low current consumption: 2.4mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA602 meets cellular radio specifications**

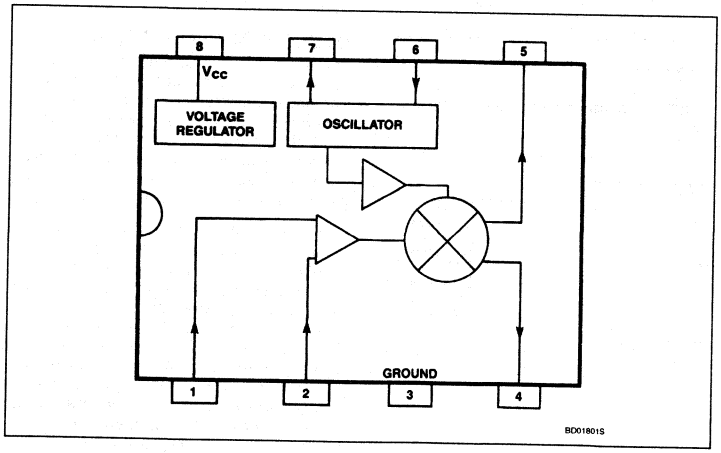
APPLICATIONS

- **Cellular radio mixer/oscillator**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE602N
8-Pin Plastic SO	0 to +70°C	NE602D
8-Pin Cerdip	0 to +70°C	NE602FE
8-Pin Plastic DIP	−40°C to +85°C	SA602N
8-Pin Plastic SO	−40°C to +85°C	SA602D
8-Pin Cerdip	−40°C to +85°C	SA602FE

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range NE602 SA602	0 to +70 −40 to +85	°C °C

AC/DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 6V$, Figure 1

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0	6.0	dB
	Third-order intercept point	RF_{IN} = −45dBm: f_1 = 45.0 f_2 = 45.06		−15	−17	dBm
	Conversion gain at 45MHz		14			dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

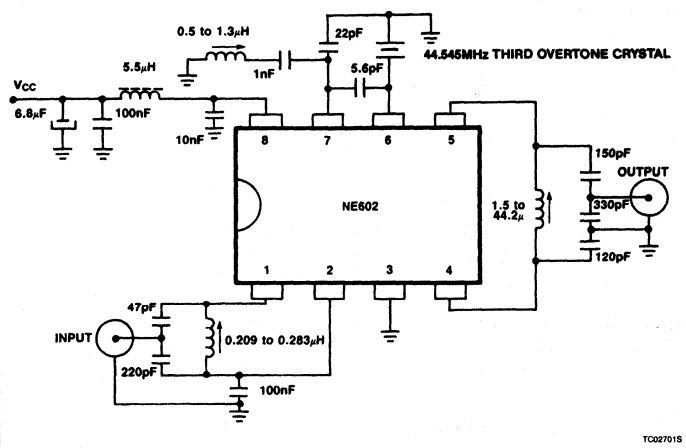


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE/SA602 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE/SA602 is designed for optimum low power performance. When used with the SA604 as a 45MHz cellular radio 2nd IF and demodulator, the SA602 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE602 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE/SA602 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedence is approximately 1.5k ‖ 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be at least $200mV_{P-P}$.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. 22kΩ will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

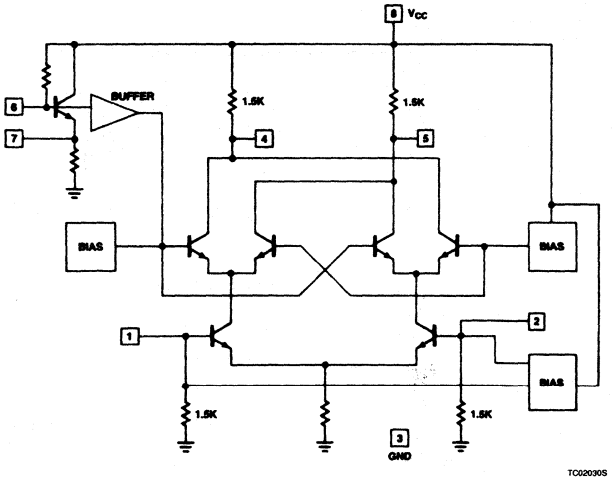
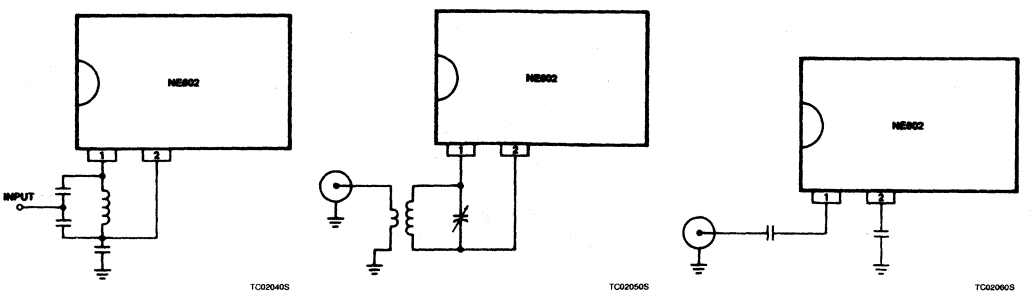


Figure 2. Equivalent Circuit

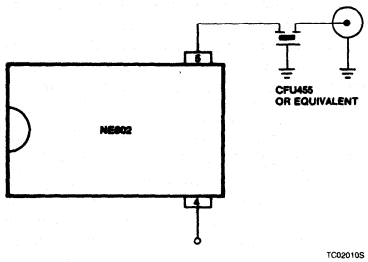


a. Single-Ended Tuned Input

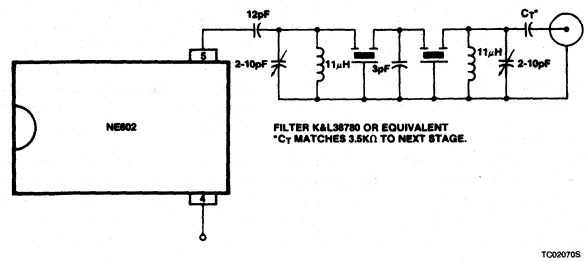
b. Balanced Input (For Attenuation of Second-Order Products)

c. Single-Ended Untuned Input

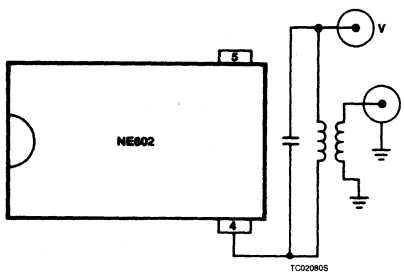
Figure 3. Input Configuration



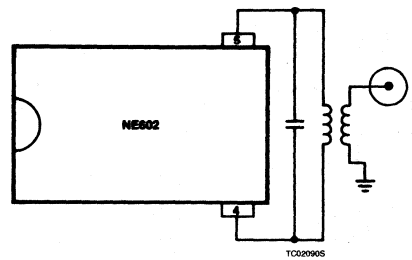
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

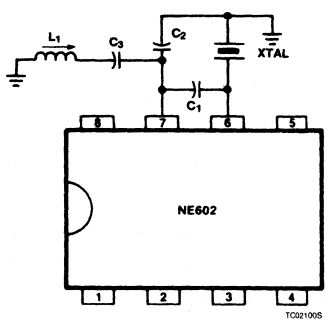


c. Single-Ended IFT

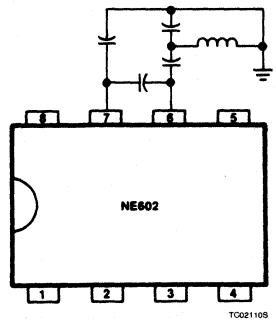


d. Balanced Output

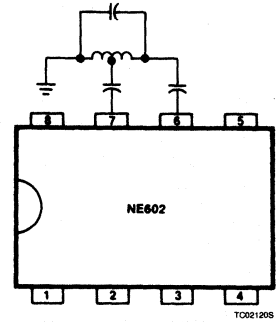
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

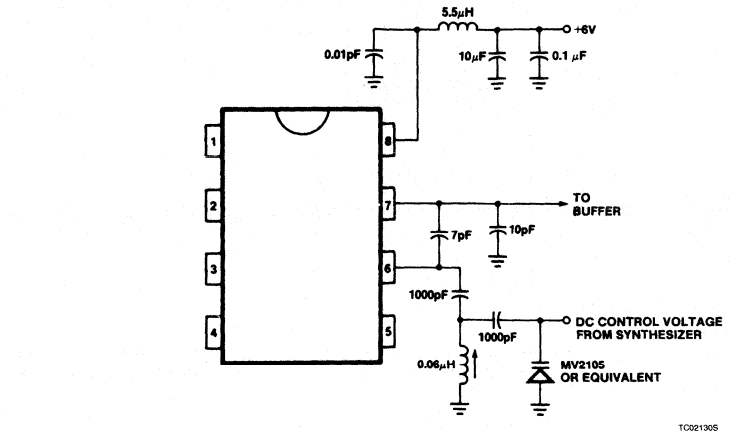


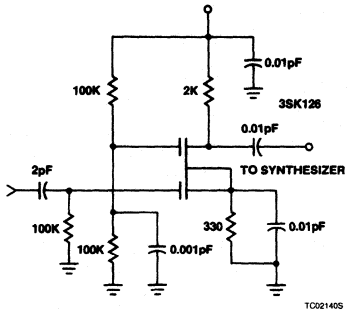
b. Colpitts L/C Tank Oscillator

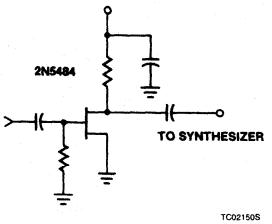


c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits







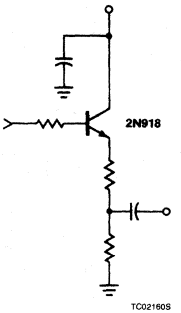


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

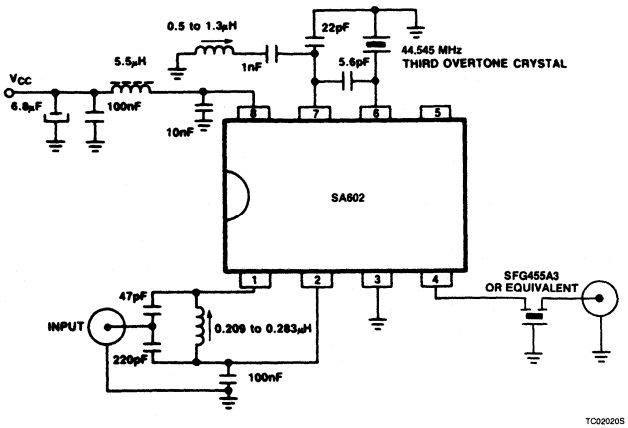


Figure 7. Typical Application for Cellular Radio

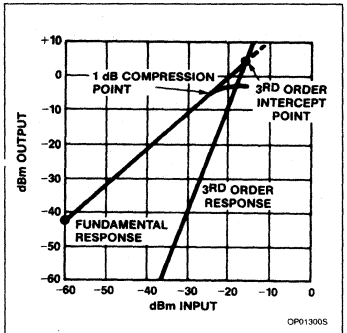


Figure 8. SA/NE602 Third-Order Intermod and 1dB Compression Point Performance

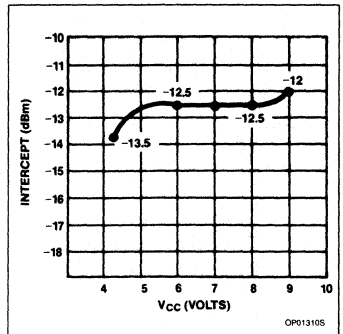


Figure 9. Input Third-Order Intercept Point vs V_{CC}

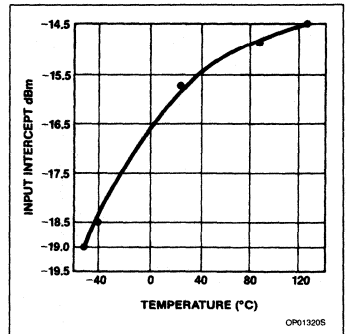


Figure 10. Third-Order Intercept Point vs Temperature

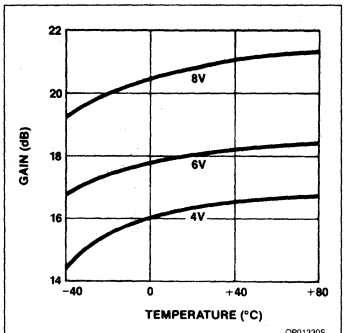


Figure 11

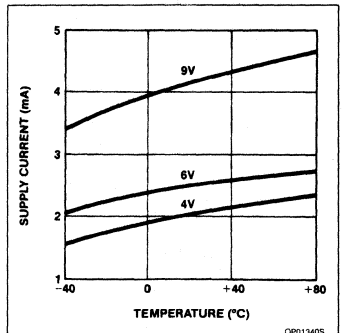


Figure 12

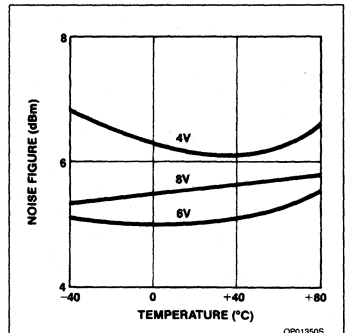


Figure 13

NE/SA604
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The NE/SA604 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE/SA604 is available in a 16-lead dual in-line plastic and Cerdip packages and 16-lead SO (surface-mounted miniature package).

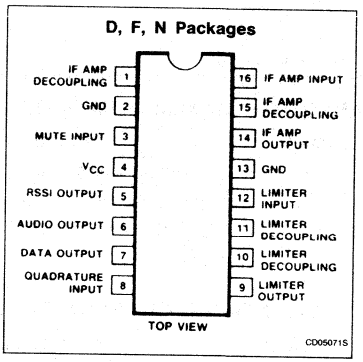
FEATURES

- **Low power consumption: 2.3mA typical**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 90dB**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity: 1.5μV across input pins (0.27μV into 50Ω matching network) for 12dB SINAD (Signal-to-Noise and Distortion ratio) at 455kHz**
- **SA604 meets cellular radio specifications**

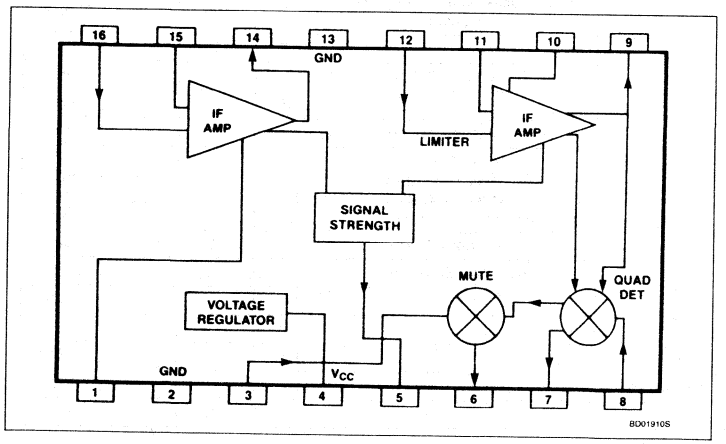
APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE604N
16-Pin Plastic SO	0 to +70°C	NE604D
16-Pin Cerdip	0 to +70°C	NE604F
16-Pin Plastic DIP	−40°C to +85°C	SA604N
16-Pin Cerdip	−40°C to +85°C	SA604F
16-Pin Plastic SO	−40°C to +85°C	SA604D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE604 SA604	 0 to +70 −40 to +85	 °C °C

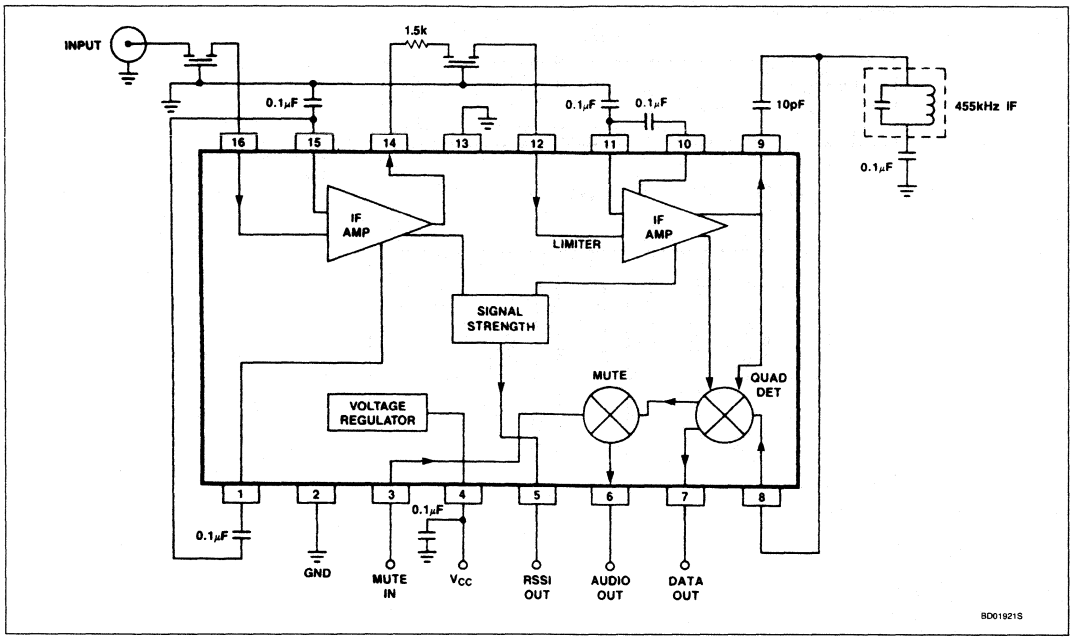
DC ELECTRICAL CHARACTERISTICS T_A = 25°C; V_{CC} = +6V, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain				2.7	mA
	Mute switch input threshold (on) (off)		 1.7		 1.0	 V V

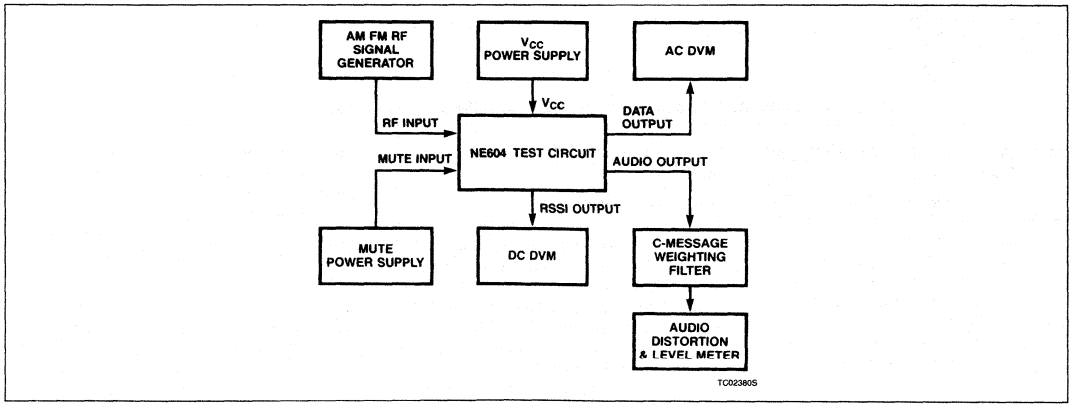
AC ELECTRICAL CHARACTERISTICS T_A = 25°C; V_{CC} = +6V, unless otherwise stated. RF frequency = 455kHz; RF level = −47dBm; FM modulation = 1kHz with+ 8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

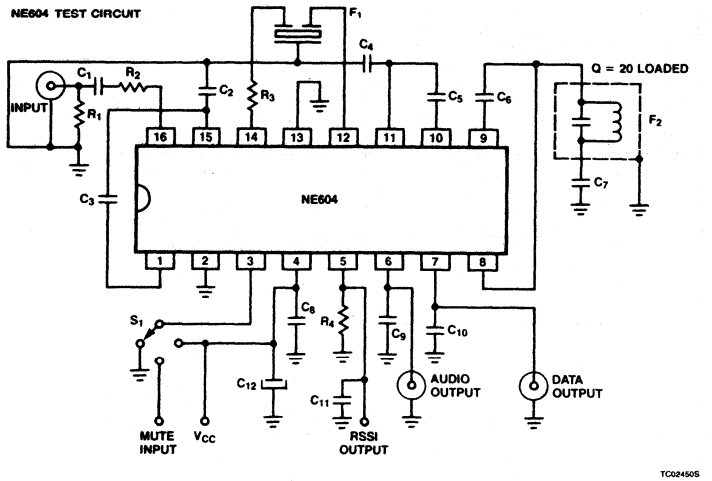
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input limiting - 3dB	Test at Pin 16			−90	dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level - 97dBm	12	15		dB
THD	Total harmonic distortion		−35			dB
S/N	Signal-to-noise ratio	No modulation for noise	70	75		dB
	RSSI output	R_4 = 100kΩ RF level = −97dBm RF level = −47dBm RF level = 3dBm	 0 2.0 4.0		 400 2.6 5.0	 mV V V
	RSSI range	R_4 = 100kΩ Pin 5		90		dB
	RSSI accuracy	R_4 = 100kΩ Pin 5		±1.5		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance		50			kΩ
	Muted audio output impedance			50		kΩ

TYPICAL 455kHz APPLICATION



NE604 TEST SETUP





NOTES:
C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V Polyester
C3 100nF ± 10% 50V Polyester
C4 100nF ± 10% 50V Polyester
C5 100nF ± 10% 50V Polyester
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V Polyester
C8 100nF ± 10% 50V Polyester
C9 15nF ± 10% 50V Polyester
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8uF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% ¼W Metal Film
R2 1500Ω ± 1% ¼W Metal Film
R3 1500Ω ± 5% ⅛W Carbon Composition
R4 100kΩ ± 1% ¼W Metal Film

Figure 1. NE604 Test Circuit and Parts List for 455kHz IF with 30kHz Bandwidth

DESCRIPTION OF OPERATION

The NE/SA604 is comprised of five subsystems for IF signal processing. These subsystems, two IF limiting amplifiers, quadrature detector, audio mute, and logarithmic signal strength, can be configured to satisfy many high-performance or low-power systems objectives. Internal temperature compensated bias regulation completes the circuitry. Taken together, the SA604 exceeds the demanding technical requirements for cellular radio.

Figure 2 shows the equivalent circuits of the NE/SA604.

Limiting Amplifiers

The NE/SA604 has two independent limiting IF amplifiers. The first has a gain of 30dB. The second has 60dB gain. Both have 1.5k nominal input impedance and 15MHz bandwidth. The output impedance of the first limiter is approximately 1kΩ. These impedances permit direct interface with popular ceramic filters such as the SFU455. On the surface, the 1k output of the first limiter would not seem correct. However, approximately 6dB insertion loss is required between limiter stages to optimize the linearity of the signal strength indicator. The impedance mismatch has little effect on passband. Use of an interstage filter reduces wide-band noise. A DC blocking capacitor or L/C filter can also be used.

As the signal frequency increases, the 90dB total gain can become a source of instability. Figure 3 shows the limiters as a closed-loop system with stray capacitance and the equivalent AC input impedance setting the loop gain.

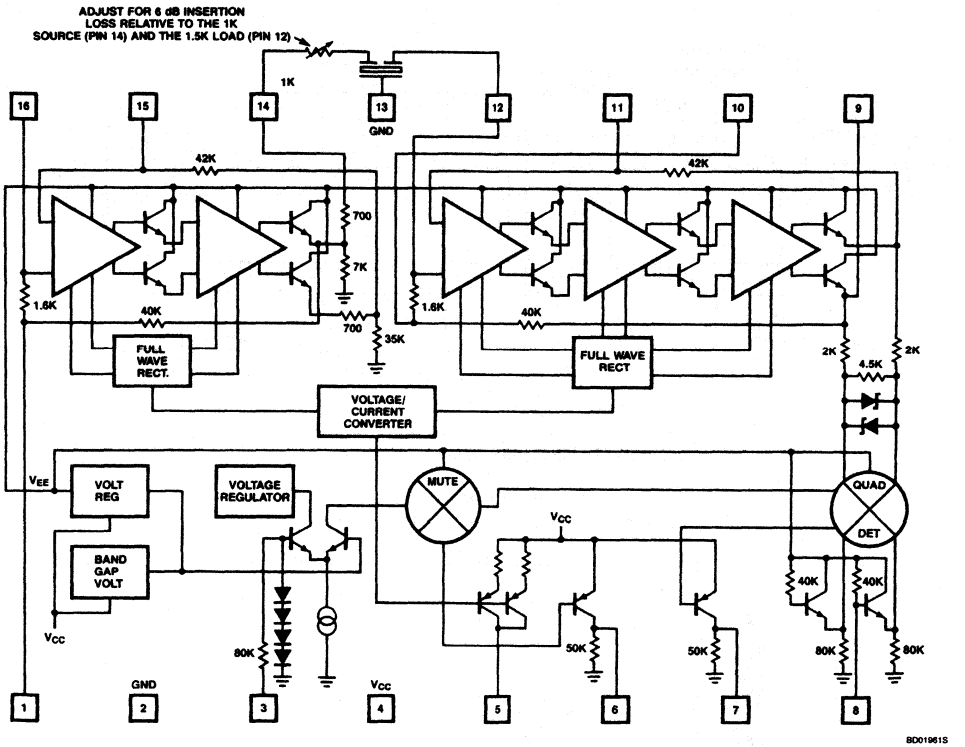


Figure 2. Equivalent Circuit

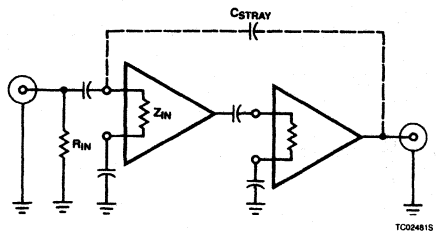
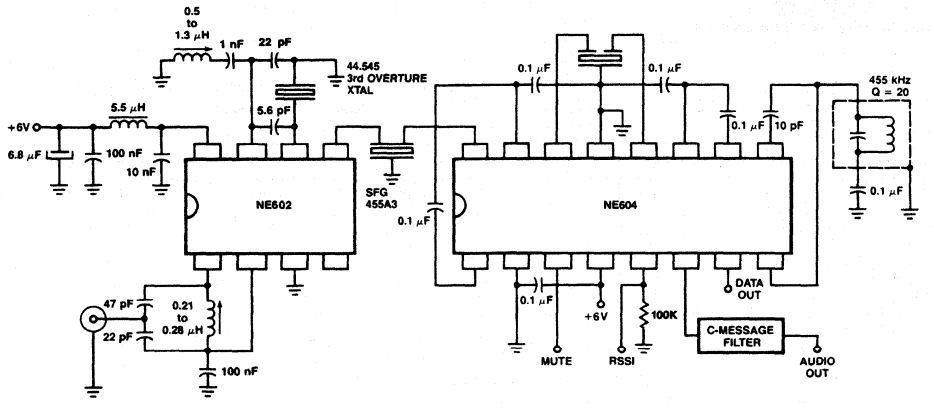


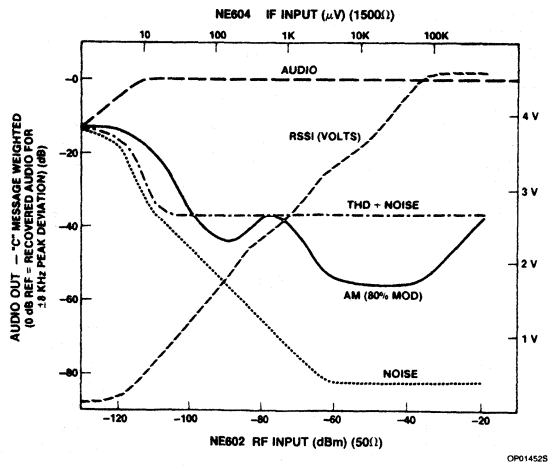
Figure 3. Considerations for Stability

The equivalent AC attenuation factor from the output to the input must be greater than 90dB or oscillation can occur. The input impedance of the device is nominally 1.5k. The stray layout capacitance is a frequency-dependent impedance so that as the frequency of operation or the value of stray capacitance increases, the output-to-input attenuation factor decreases. Keep stray capacitance low by using good RF layout technique. Sockets should be avoided above 455kHz.

Good RF layout is the proper way to avoid instability. However, if system constraints require, stability can be achieved by only using one of the limiting amplifiers, or by adding a resistance, R_{IN}, which will increase the attenuation factor.



a. Cellular Radio Configuration with 455kHz IF



b. Cellular Circuit Performance

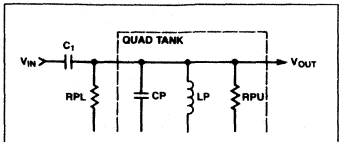
Figure 4

Adding an input resistor is an easy way to reduce the attenuation factor, but may make correct termination of interstage filters difficult or impossible. At 455kHz instability should not be a problem if reasonable RF layout is used.

Quadrature Detector

The detector of the NE604 is a four quadrant multiplier of the Gilbert cell type. It can be used for frequency or amplitude demodulation. Figure 4 indicates a typical quadrature FM configuration. Fully limited in-phase signal is applied to the multiplier internally. 90° phase shift is accomplished with the L/C tuned circuit connected directly to Pin 8 and capacitively to Pin 9. Because of the DC bias of the NE604, the phase shift network must be returned to ground through a low impedance capacitor. Recovered signal is continuously available at Pin 7 or on a switched basis at Pin 6.

The quadrature coil or crystal/ceramic discriminator affects three system parameters: bandwidth, linearity, and detected signal amplitude. Figure 6 shows three quadrature curves.



EQUATION

$$\frac{V_{OUT}}{V_{IN}} = \frac{j\omega C_1}{\frac{1}{RPL \parallel RPU}\left(1 + j2Q\frac{\Delta\omega}{\omega_0}\right) + j\omega C_1}$$

$Q = \omega_0 (RPL \parallel RPU) CP$

$\Delta\omega$ = PEAK DEVIATION

ω_0 = CENTER FREQUENCY

TC02390S

Figure 5. General Equations For Quadrature Coil

Table 1. System Parameters as Applied to Figure 4a

$\Delta\omega$	=	2π•8kHz
ω_0	=	2π•455kHz
CP	=	180pF
RPU	=	233K
RPL	=	40K
LP	=	644μH
Q	≈	20

Curve A has the most narrow bandwidth and high peak-to-peak output versus frequency deviation corresponding to a high Q network.

Curve C is very low Q with good linearity and shows how very large deviations can be processed. Curve B shows how the quadrature network can cause non-linearity in the detected output. A loaded Q for the 455kHz quadrature coil of Figure 4 is 20. Using the test circuit of Figure 4 with an input of −47dBm, the recovered audio is typically 90mV_{RMS} with −35dB distortion.

While the NE604 was designed principally for FM applications, the detector can be used for synchronous amplitude demodulation if the carrier is limited through the internal circuitry and AGC'd external to the device. The AGC'd signal is applied to Pin 8 instead of a quadrature signal. The signal strength indicator can control AGC. A low-pass filter on the output completes the demodulator. Figure 7 shows the equivalent circuit.

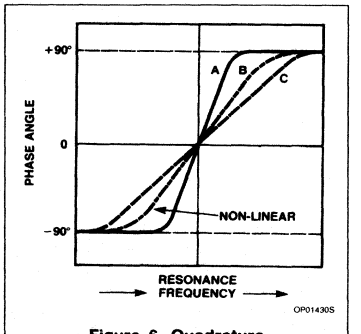


Figure 6. Quadrature

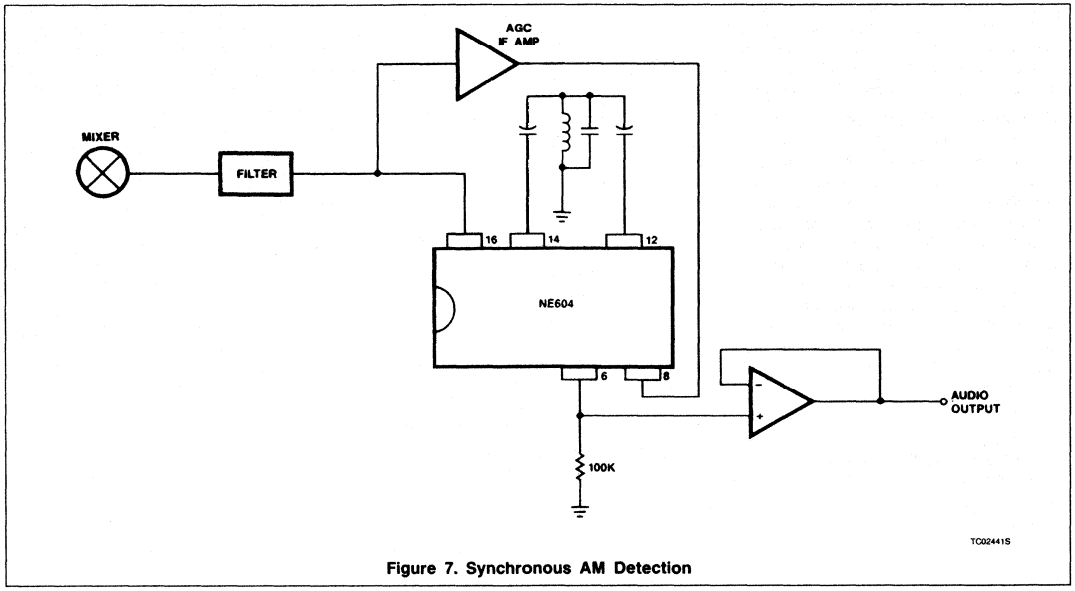


Figure 7. Synchronous AM Detection

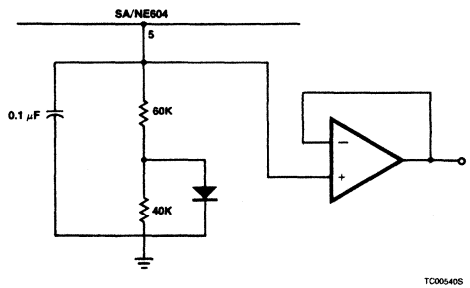
Audio Mute

An electronic switch permits muting or squelch of one of the demodulated outputs. The data (unmuted output) and audio (muted output) both have 50kΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (Pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

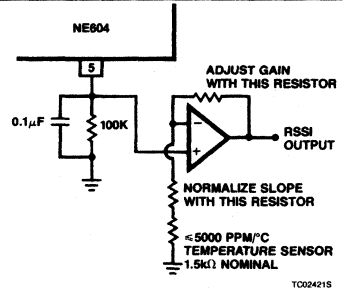
Signal Strength Indicator

The logarithmic signal strength indicator is a current source output with maximum source current of 50μA. The signal strength indicator's transfer function is approximately 10μA per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

There is some temperature dependence to the signal strength output. Figure 8 shows the characteristic. Two suggested lead circuits are shown to improve linearity in critical applications. For cellular radio applications use of either technique and the SA604 device (−40°C to +85°C) will assure compliance with RSSI criteria.



a. Temperature-Compensated RSSI Circuits



b.

Figure 8. Signal Strength

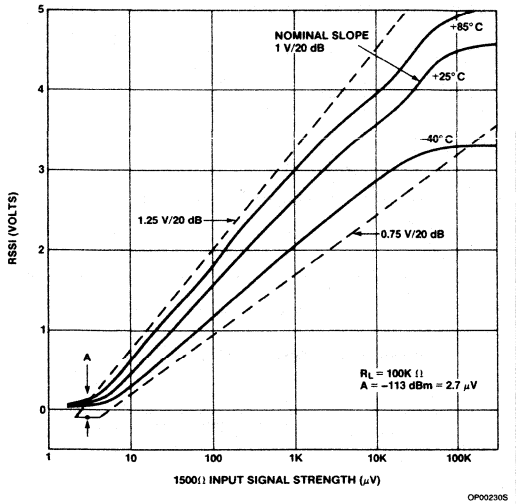


Figure 8. Signal Strength (Continued)

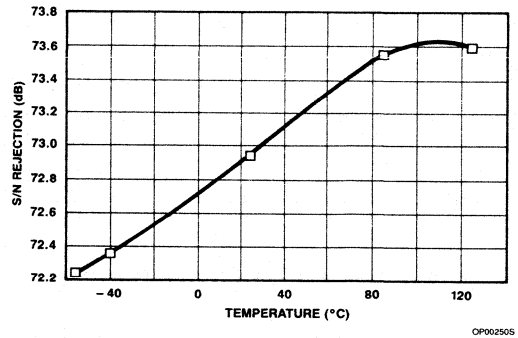


Figure 9. NE/SA604 Signal-To-Noise Ratio vs Temperature

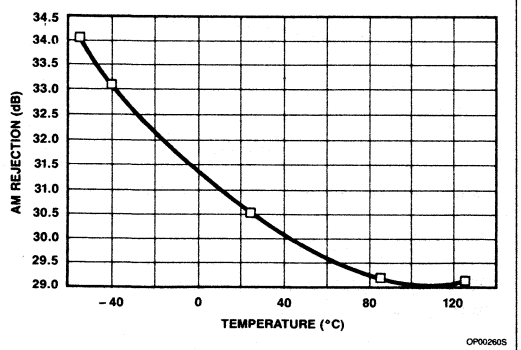


Figure 10. NE/SA604 AM Rejection vs Temperature

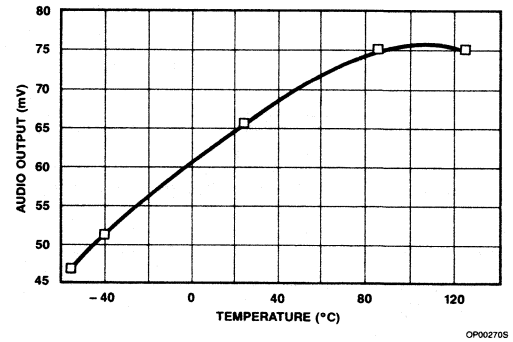


Figure 11. NE/SA604 Audio Output vs Temperature

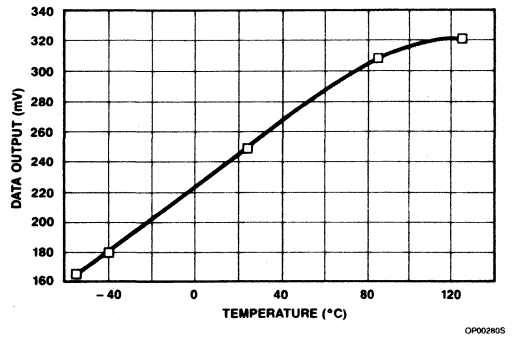


Figure 12. NE/SA604 Data Output vs Temperature

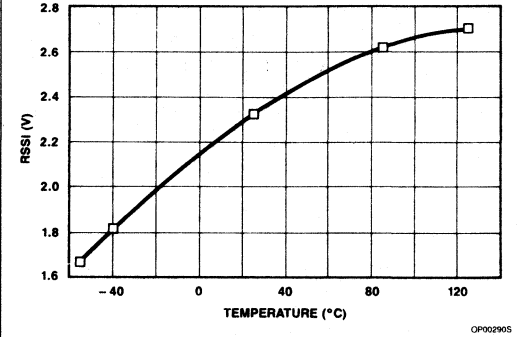


Figure 13. RSSI vs Temperature

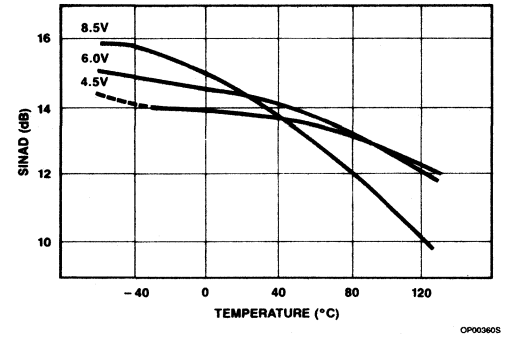


Figure 14. NE/SA604 SINAD vs Temperature and V_{CC}

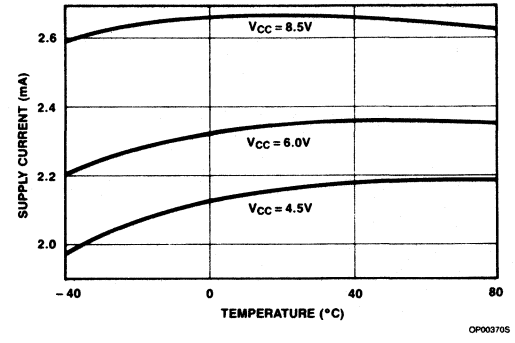


Figure 15. SA604 Supply Current vs Temperature

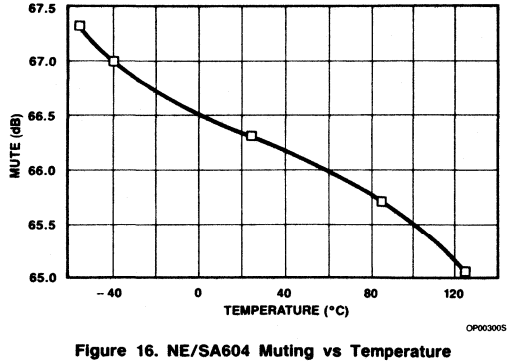


Figure 16. NE/SA604 Muting vs Temperature

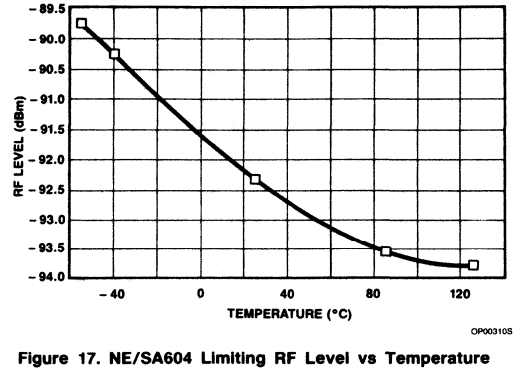


Figure 17. NE/SA604 Limiting RF Level vs Temperature

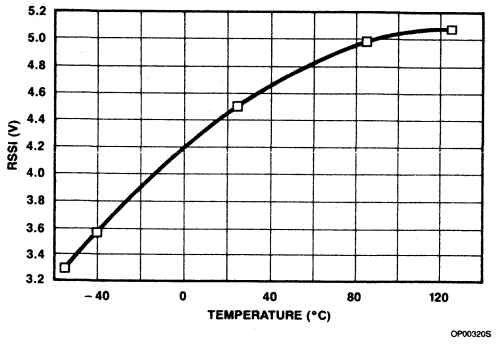


Figure 18. NE/SA604 Large-Signal Uncompensated RSSI Voltage vs Temperature

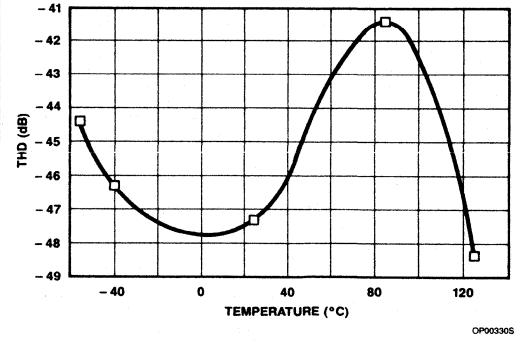


Figure 19. NE/SA604 Total Harmonic Distortion vs Temperature

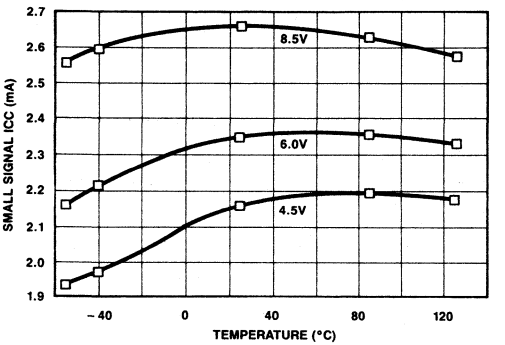


Figure 20. NE/SA604 Supply Current vs Temperature and Voltage

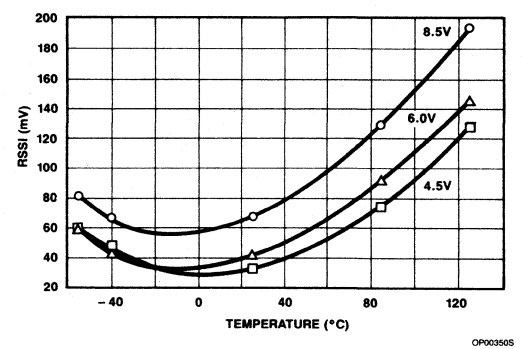


Figure 21. Small-Signal RSSI vs Temperature and Voltage

NE/SA605
Low Power FM IF System

Objective Specification

Linear Products

DESCRIPTION

The NE/SA605 is a monolithic, low power FM IF system incorporating VHF monolithic, double-balanced mixer with input amplifier, on-board oscillator, two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator.

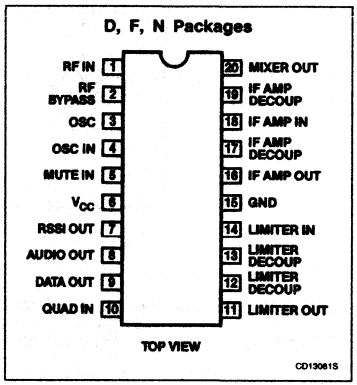
It is intended for high performance, low power communication systems. The guaranteed parameters of the SA605 make this device particularly well-suited to cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 15dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external L.O. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low power, and noise characteristics make the NE/SA605 a superior choice for high-performance battery-operated equipment.

The NE/SA605 is available in 20-lead dual in-line plastic and Cerdip packages and 20-pin SO (surface-mounted miniature) packages.

FEATURES

- **Low power consumption: 5.3mA typical**
- **Excellent noise figure: < 5.0dB typical at 45MHz**
- **High operating frequency**
- **Excellent gain, intercept, and sensitivity**
- **Low external parts count; suitable for crystal/ceramic filters**
- **SA605 meets cellular radio specifications**
- **Logarithmic Received Signal Strength Indicator (RSSI) with a dynamic range in excess of 80dB**
- **Separate data output**
- **Audio output with muting**
- **Excellent sensitivity: 1.5μV across input pins (0.27μV into 50Ω matching network) for 12dB SINAD (Signal-to-Noise and Distortion ratio) at 455kHz**

PIN CONFIGURATION



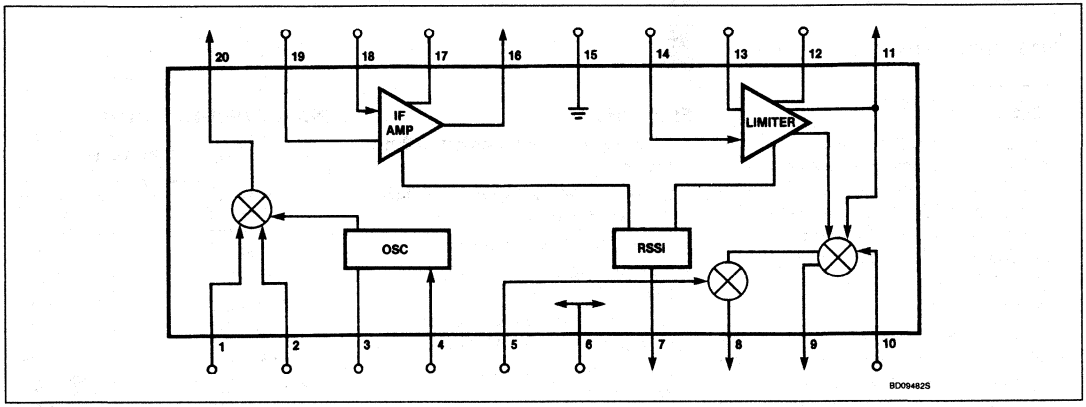
APPLICATIONS

- **Cellular radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 25MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **HF/VHF frequency conversion**
- **Instrumentation frequency conversion**
- **Broadband LANs**

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	0 to +70°C	NE605N
20-Pin Plastic SO	0 to +70°C	NE605D
20-Pin Ceramic DIP	0 to +70°C	NE605F
20-Pin Plastic DIP	-40°C to +85°C	SA605N
20-Pin Plastic SO	-40°C to +85°C	SA605D
20-Pin Ceramic DIP	-40°C to +85°C	SA605F

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating temperature range NE605 SA605	 0 to +70 −40 to +85	 °C °C

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			5.3	6.0	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	 V V

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$; $V_{CC} = +6V$, unless otherwise specified. RF frequency = 45MHz; IF frequency = 455MHz; FM modulation = 1kHz with ±8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 45MHz			5.0		dB
	Third-order intercept point	$RF_{IN} = -45dBm$: $f_1 = 45.0$ $f_2 = 45.06$		−15		dBm
	Conversion gain at 45MHz			15		dB
R_{IN}	RF input resistance	Single-ended input	1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 20)		1.5		kΩ
	Input limiting −3dB	Test at Pin 1		−117		dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level −117dBm	12	15		dB
THD	Total harmonic distortion		−35			dB
S/N	Signal-to-noise ratio	No modulation for noise	70	75		dB
	RSSI output	$R_{RSSI} = 100K$ RF level = −117dBm RF level = −67dBm RF level = −23dBm	 0 2.0 4.0		 400 2.6 5.0	 mV V V
	RSSI range	$R_{RSSI} = 100k$ Pin 7		90		dB
	RSSI accuracy	$R_{RSSI} = 100k$ Pin 7		±1.5		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance			50		kΩ
	Muted audio output impedance			50		kΩ

Circuit Description

The NE/SA605 is an RF/IF signal processing system suitable for second IF or single conversion systems with input frequency as high as 500MHz. The bandwidth of the IF amplifiers is 25MHz. However, the gain distribution is optimized for 455kHz. The overall system is well-suited to battery operation as well as high-performance and high quality products of all types.

The input stage is a Gilbert cell mixer with oscillator. Typical mixer characteristics include a noise figure of 5dB, conversion gain of 15dB, and input third order intercept of −15dBm. The oscillator will operate well in excess of 200MHz in L/C tank configurations, either Hartley or Colpitts. For crystal oscillators, the Colpitts configuration is used.

The output of the mixer is internally loaded with a 1.5kΩ resistor permitting direct connection to a 455kHz ceramic filter. The equivalent input impedance of the limiting IF amplifiers is also 1.5kΩ. With most 455kHz ceramic filters and many crystal filters, no impedance matching network is necessary. To achieve optimum linearity of the log signal strength indicator, there must be a 6dB insertion loss between the first and second IF stages. If the IF filter or interstage network does not cause 6dB insertion loss, a fixed or variable resistor can be added between the first IF output (Pin 16) and the interstage network..

The signal from the second limiting amplifier goes to a Gilbert cell quadrature detector. One port of the Gilbert cell is internally driven by the IF. The other output of the IF is AC-coupled to a tuned quadrature network. This signal, which now has a 90° phase relationship to the internal signal, drives the other port of the multiplier cell.

Overall, the IF section has a gain of 92dB. For operation at intermediate frequencies greater than 455kHz, special care must be given to layout, termination, and interstage loss to avoid instability. Alternatively, if gain distribution permits, only the second limiting IF stage can be used. This stage has 57dB of gain.

The demodulated output of the quadrature detector is available at two pins, one continuous and one with a mute switch. Signal attenuation with the mute activated is greater than 60dB. The mute input is very high impedance and is compatible with CMOS or TTL levels.

A log signal strength indicator completes the circuitry. The output range is greater than 80dB and is temperature compensated. This log signal strength indicator exceeds the criteria for AMPs or TACs cellular telephone.

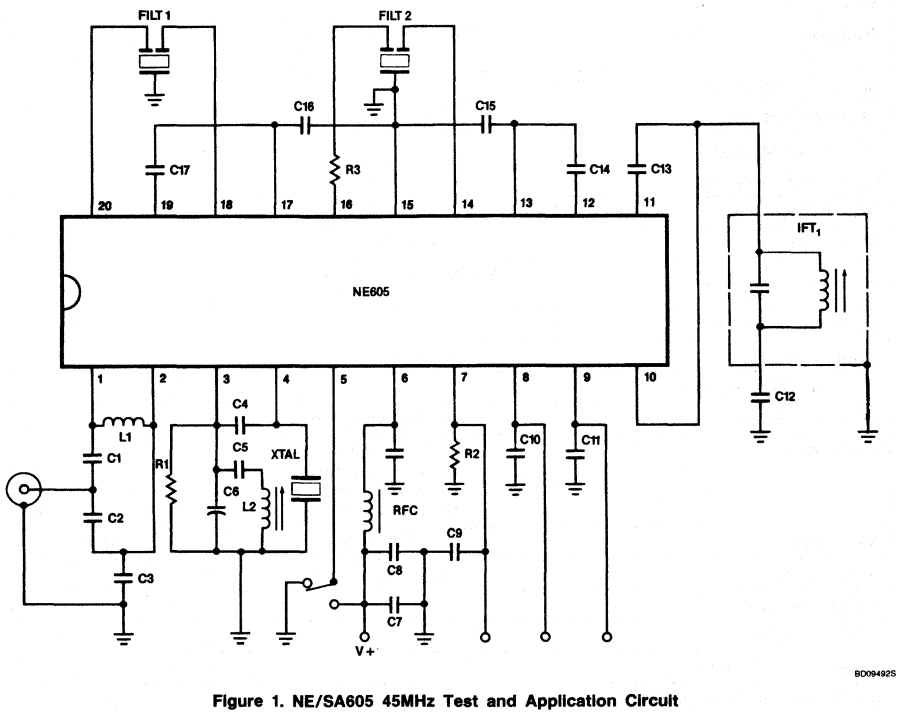


Figure 1. NE/SA605 45MHz Test and Application Circuit

NE612
Double-Balanced Mixer and Oscillator

Product Specification

Linear Products

DESCRIPTION

The NE612 is a low-power VHF monolithic double-balanced mixer with on-board oscillator and voltage regulator. It is intended for low cost, low power communication systems with signal frequencies to 500MHz and local oscillator frequencies as high as 200MHz. The mixer is a "Gilbert cell" multiplier configuration which provides gain of 14dB or more at 49MHz.

The oscillator can be configured for a crystal, a tuned tank operation, or as a buffer for an external L.O. Noise figure at 49MHz is typically below 6dB and makes the device well suited for high performance cordless telephone. The low power consumption makes the NE612 excellent for battery operated equipment. Networking and other communications products can benefit from very low radiated energy levels within systems. The NE612 is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface mounted miniature package).

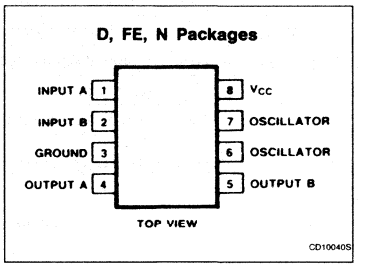
FEATURES

- **Low current consumption**
- **Low cost**
- **Operation to 500MHz**
- **Low radiated energy**
- **Low external parts count; suitable for crystal/ceramic filter**
- **Excellent sensitivity, gain, and noise figure**

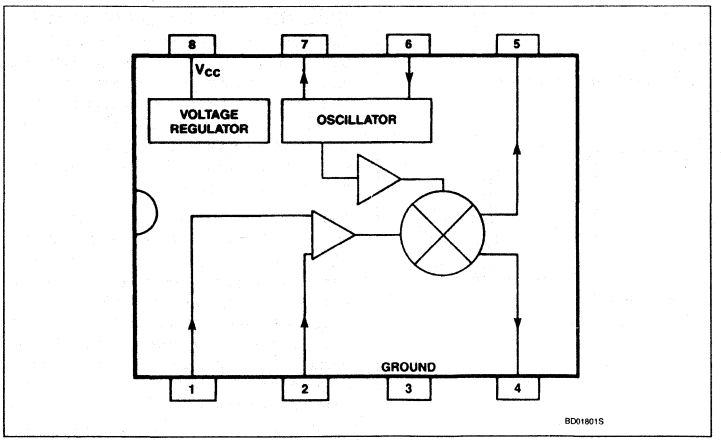
APPLICATIONS

- **Cordless telephone**
- **Portable radio**
- **VHF transceivers**
- **RF data links**
- **Sonabuoys**
- **Communications receivers**
- **Broadband LANs**
- **HF and VHF frequency conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic DIP	0 to +70°C	NE612N
8-Pin Plastic SO	0 to +70°C	NE612D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature	−65 to +150	°C
T_A	Operating ambient temperature range	0 to +70	°C

AC/DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 6V, Figure 1

SYMBOL	PARAMETER	TEST CONDITION	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figured at 49MHz			5.0		dB
	Third-order intercept point at 49MHz	RF_{IN} = −45dBm		−15		dBm
	Conversion gain at 49MHz		14			dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3		pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

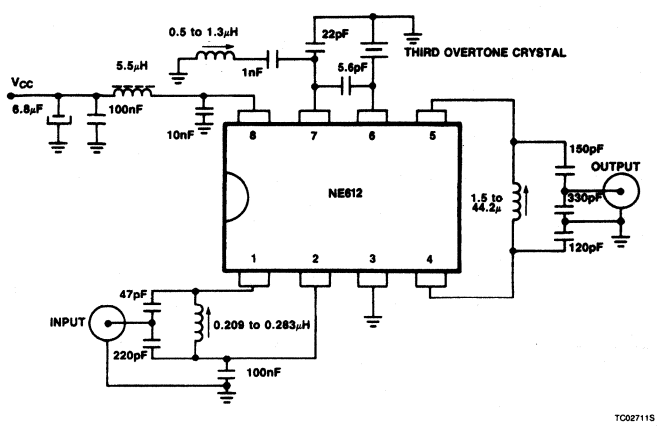


Figure 1. Test Configuration

DESCRIPTION OF OPERATION

The NE612 is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The NE612 is designed for optimum low power performance. When used with the NE614 as a 49MHz cordless telephone system, the NE612 is capable of receiving −119dBm signals with a 12dB S/N ratio. Third-order intercept is typically −15dBm (that's approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues not critical, the input to the NE612 should be appropriately scaled.

Besides excellent low power performance well into VHF, the NE612 is designed to be flexible. The input, output, and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 3 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 4 shows three single-ended output configurations and a balanced output.

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the Q of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required L.O. is beyond oscillation limits, or the system calls for an external L.O., the external signal can be injected at Pin 6 through a DC blocking capacitor. External L.O. should be $200mV_{P-P}$ minimum to $300mV_{P-P}$ maximum.

Figure 5 shows several proven oscillator circuits. Figure 5a is appropriate for cordless telephones. In this circuit a third overtone parallel-mode crystal with approximately 5pF load capacitance should be specified. Capacitor C3 and inductor L1 act as a fundamental trap. In fundamental mode oscillation the trap is omitted.

Figure 6 shows a Colpitts varacter tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar circuits provide the simple solution for non-critical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assume correct system operation.

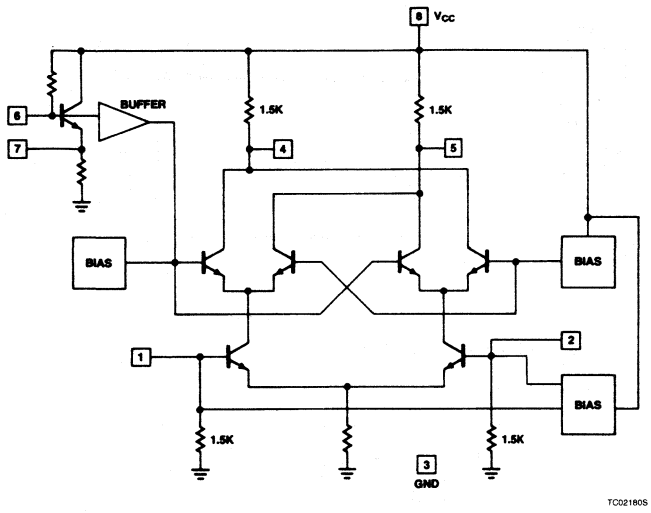
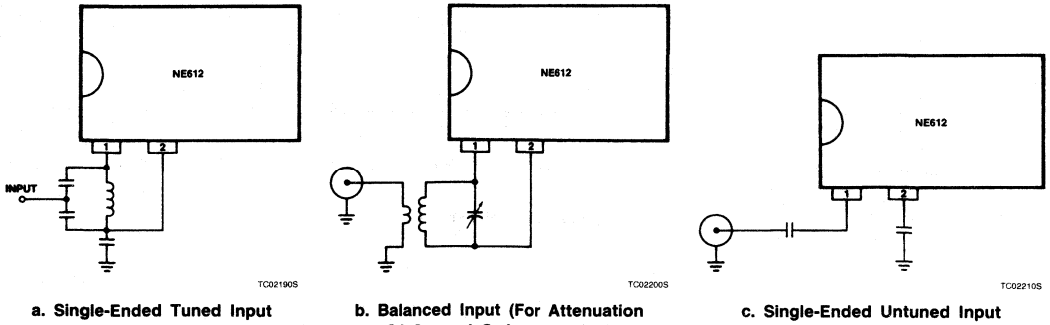


Figure 2. Equivalent Circuit

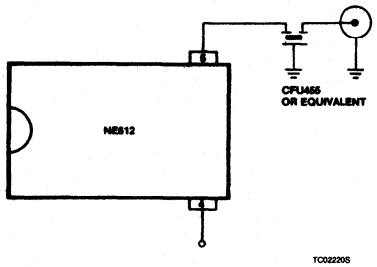


a. Single-Ended Tuned Input

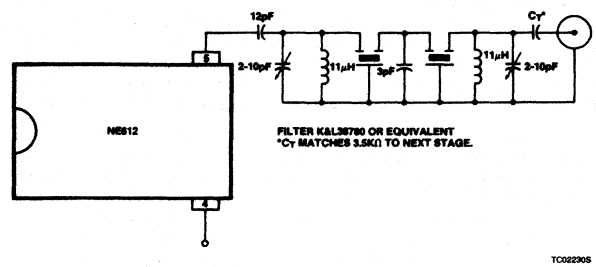
b. Balanced Input (For Attenuation Of Second Order Products)

c. Single-Ended Untuned Input

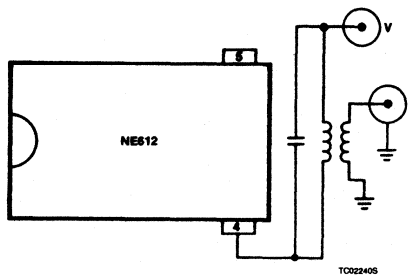
Figure 3. Input Configuration



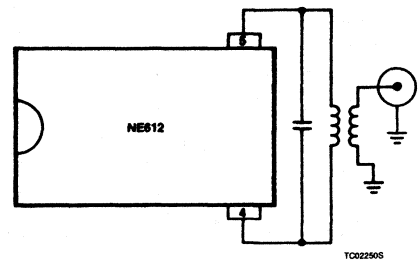
a. Single-Ended Ceramic Filter



b. Single-Ended Crystal Filter

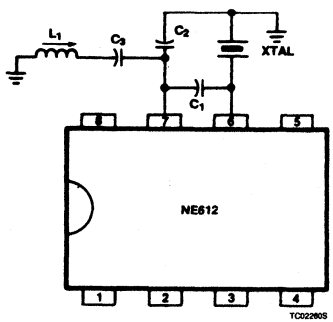


c. Single-Ended IFT

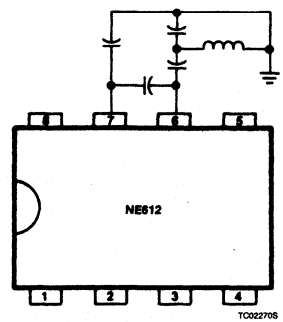


d. Balanced Output

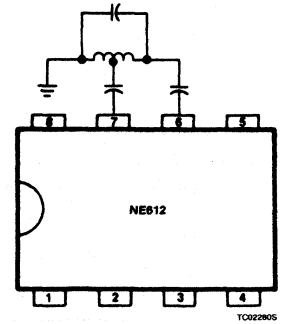
Figure 4. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)



b. Colpitts L/C Tank Oscillator



c. Hartley L/C Tank Oscillator

Figure 5. Oscillator Circuits

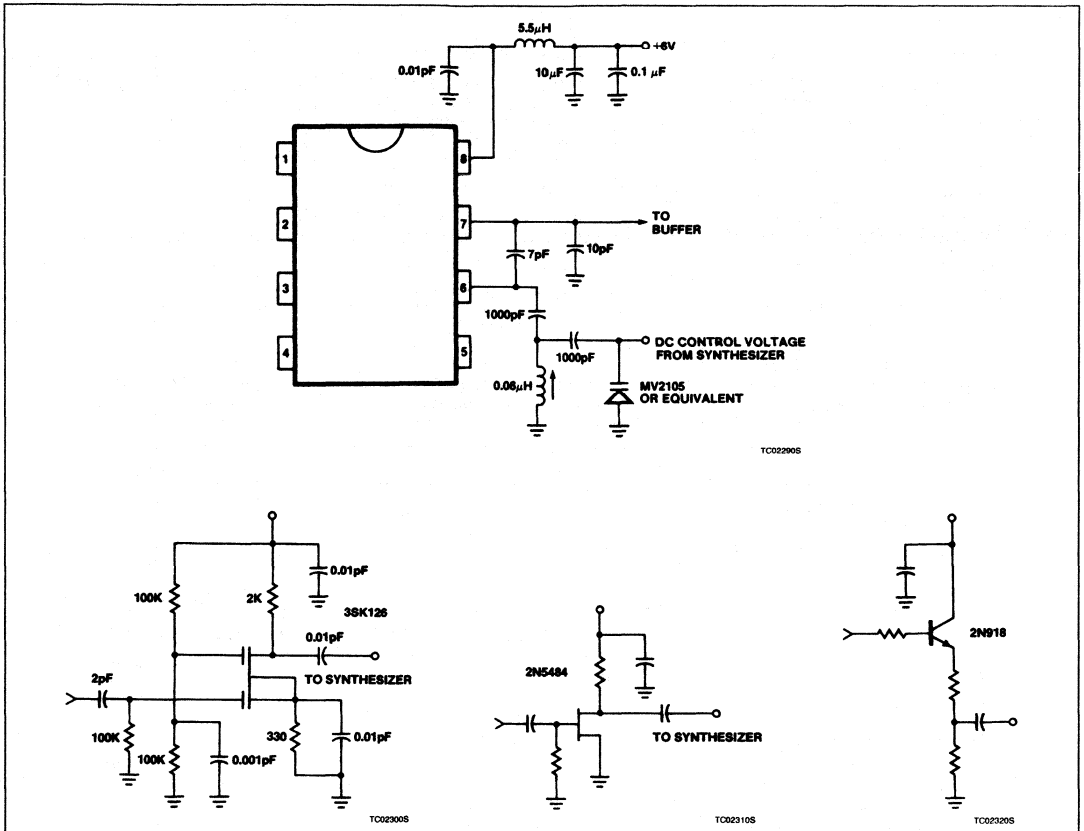


Figure 6. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

TEST CONFIGURATION

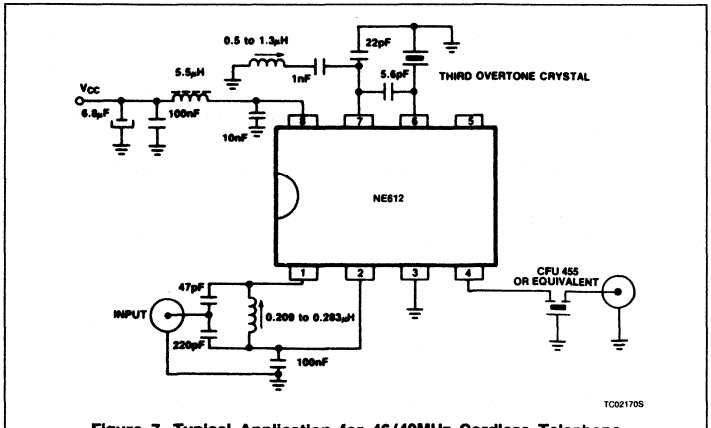


Figure 7. Typical Application for 46/49MHz Cordless Telephone

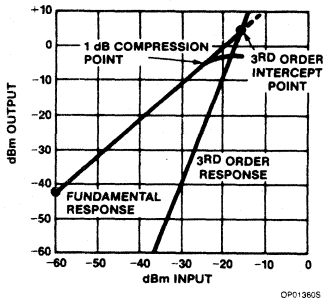


Figure 8. NE612 Third-Order Intermod And 1dB Compression Point Performance

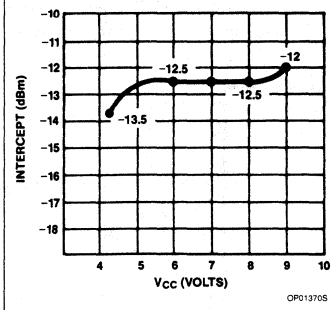


Figure 9. Input Third-Order Intercept Point vs V_{CC}

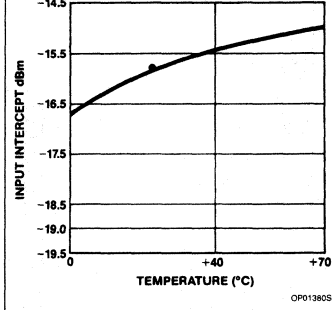


Figure 10. Third-Order Intercept Point vs Temperature

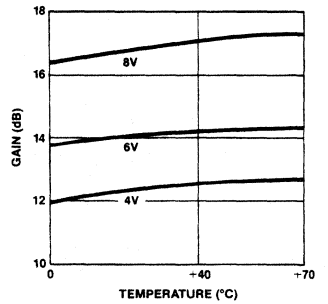


Figure 11

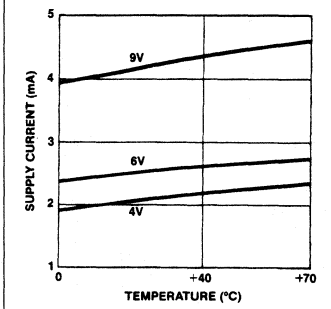


Figure 12

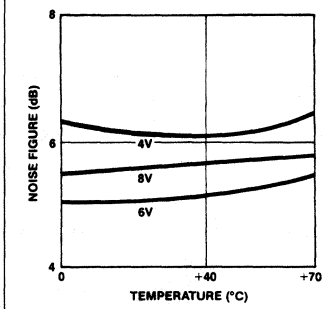


Figure 13

NE614
Low Power FM IF System

Product Specification

Linear Products

DESCRIPTION

The NE614 is a monolithic low power FM IF system incorporating two limiting intermediate frequency amplifiers, quadrature detector, muting, logarithmic signal strength indicator, and voltage regulator. The NE614 is available in a 16-lead dual in-line plastic package and 16-lead SO (surface-mounted miniature package).

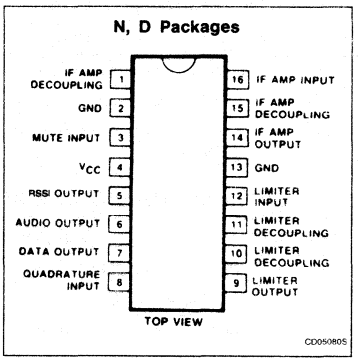
FEATURES

- **Low power consumption**
- **Logarithmic signal strength indicator**
- **Separate data output**
- **Audio output with muting**
- **Low external count; suitable for crystal/ceramic filters**
- **Excellent sensitivity**

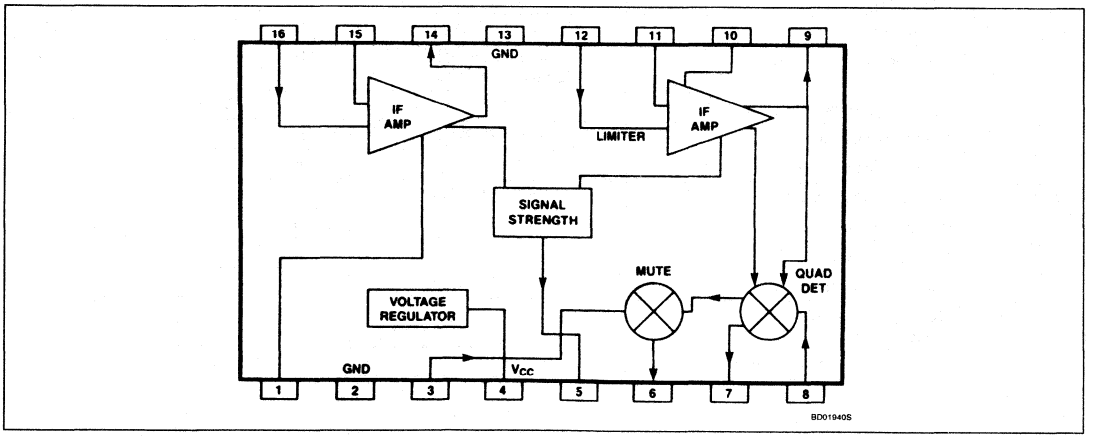
APPLICATIONS

- **Cellular Radio FM IF**
- **Communications receivers**
- **Intermediate frequency amplification and detection up to 15MHz**
- **RF level meter**
- **Spectrum analyzer**
- **Instrumentation**
- **Cordless telephone**
- **Remote control**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0 to +70°C	NE614N
16-Pin Plastic SO	0 to +70°C	NE614D

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	−65 to +150	°C
T_A	Operating ambient temperature range NE614	0 to +70	°C

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C; V_{CC} = +6V, unless otherwise specified.

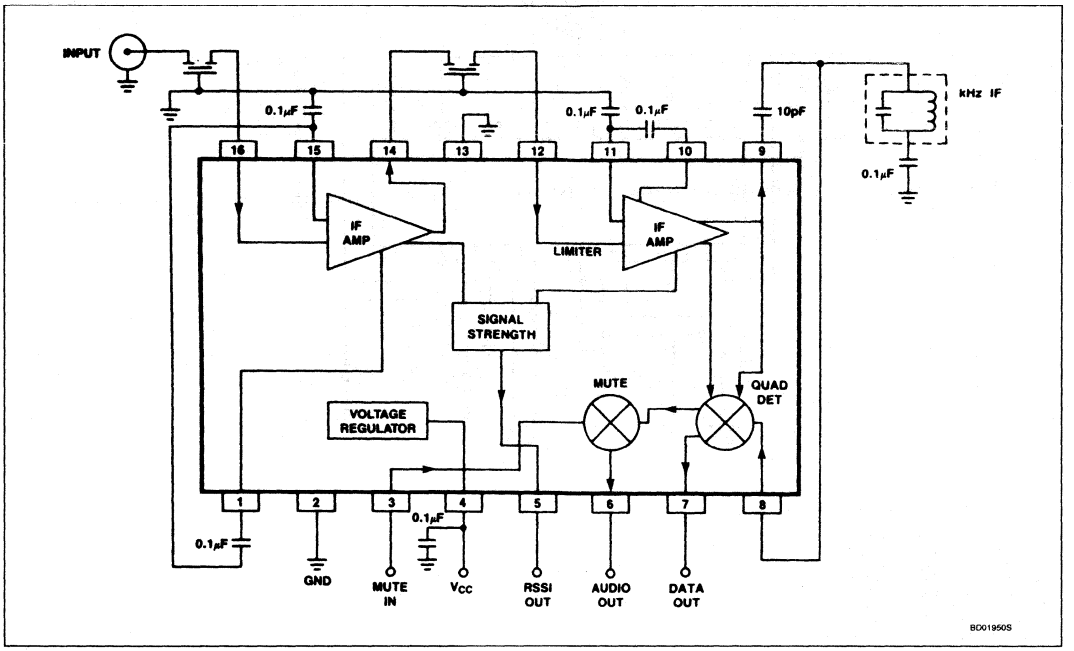
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain				3.0	mA
	Mute switch input threshold (on) (off)		1.7		 1.0	 V V

AC ELECTRICAL CHARACTERISTICS

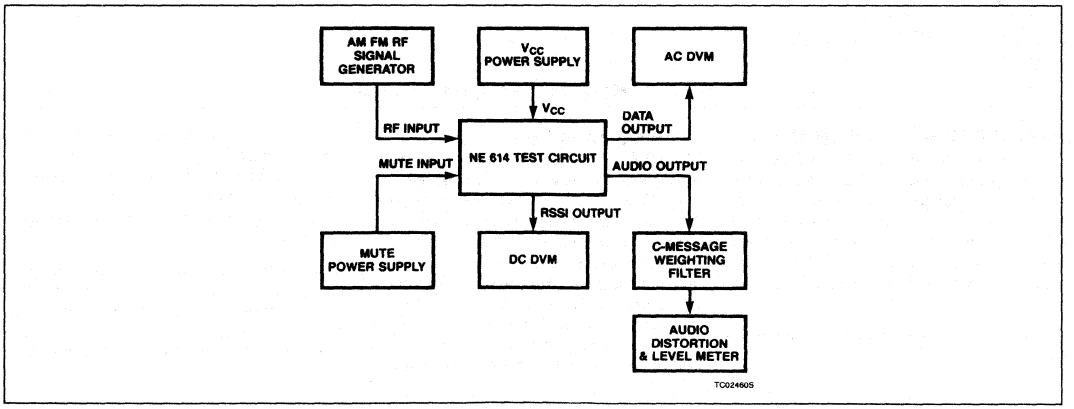
T_A = 25°C; V_{CC} = +6V, unless otherwise specified. RF frequency = 455kHz; RF level = −47dBm; FM modulation = 1kHz with +8kHz peak deviation. Audio output with C-message weighted filter and de-emphasis capacitor.

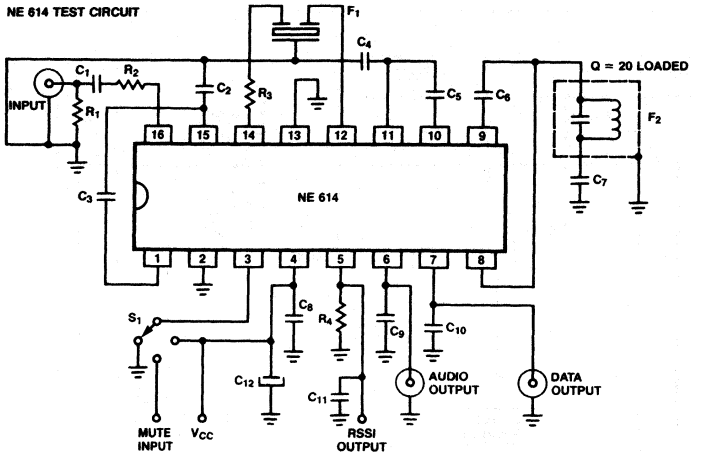
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input limiting − 3dB	Test at pin 16		−90	−80	dBm
	AM rejection	80% AM 1kHz	30			dB
	Recovered audio level	After C filter and de-emphasis capacitor	80	100		mV_{RMS}
	Recovered data level		250	350		mV_{RMS}
	SINAD sensitivity	RF level − 97dBm	8	12		dB
THD	Total harmonic distortion		−35			dB
S/N	Signal-to-noise ratio	No modulation		75		dB
	IF input impedance		1.5			kΩ
	IF output impedance		1.0			kΩ
	Limiter input impedance		1.5			kΩ
	Quadrature detector data output impedance		50			kΩ
	Muted audio output impedance			50		kΩ

TYPICAL APPLICATION



TEST SETUP





NOTES:
C1 10nF +80 – 20% 63V K10000-Z5V Ceramic
C2 100nF ± 10% 50V Polyester
C3 100nF ± 10% 50V Polyester
C4 100nF ± 10% 50V Polyester
C5 100nF ± 10% 50V Polyester
C6 10pF ± 2% 100V NPO Ceramic
C7 100nF ± 10% 50V Polyester
C8 100nF ± 10% 50V Polyester
C9 15nF ± 10% 50V Polyester
C10 150pF ± 2% 100V N1500 Ceramic
C11 1nF ± 10% 100V K2000-Y5P Ceramic
C12 6.8μF ± 20% 25V Tantalum
F1 455kHz Ceramic Filter Murata SFG455A3
F2 455kHz IF Filter A2549
R1 51Ω ± 1% 1/4W Metal Film
R2 1500Ω ± 1% 1/4W Metal Film
R3 1500Ω ± 5% 1/8W Carbon Composition
R4 100kΩ ± 1% 1/4W Metal Film

Figure 1. NE614 Test Circuit and Parts List

DESCRIPTION OF OPERATION

The NE614 is comprised of five subsystems for IF signal processing. These subsystems, two IF limiting amplifiers, quadrature detector, audio mute, and logarithmic signal strength, can be configured to satisfy many high-performance or low power systems objectives. Internal temperature compensated bias regulation completes the circuitry.

Figure 2 shows the equivalent circuits of the NE614.

Limiting Amplifiers

The NE614 has two independent limiting IF amplifiers. The first has a typical gain of 30dB. The second typically has 60dB gain. Both have 1.5k nominal input impedance and 15MHz bandwidth. The output impedance of the first limiter is approximately 1kΩ. These impedances permit direct interface with popular ceramic filters such as the SFU455. On the surface, the 1k output of the first limiter would not seem correct. However, approximately 6dB insertion loss is required between limiter stages to optimize the linearity of the signal strength indicator. The impedance mismatch has little effect on passband. Use of an interstage filter reduces wide-band noise. A DC blocking capacitor or L/C filter can also be used.

As the signal frequency increases, the 90dB total gain can become a source of instability. Figure 3 shows the limiters as a closed-loop system with stray capacitance and the equivalent AC input impedance setting the loop gain.

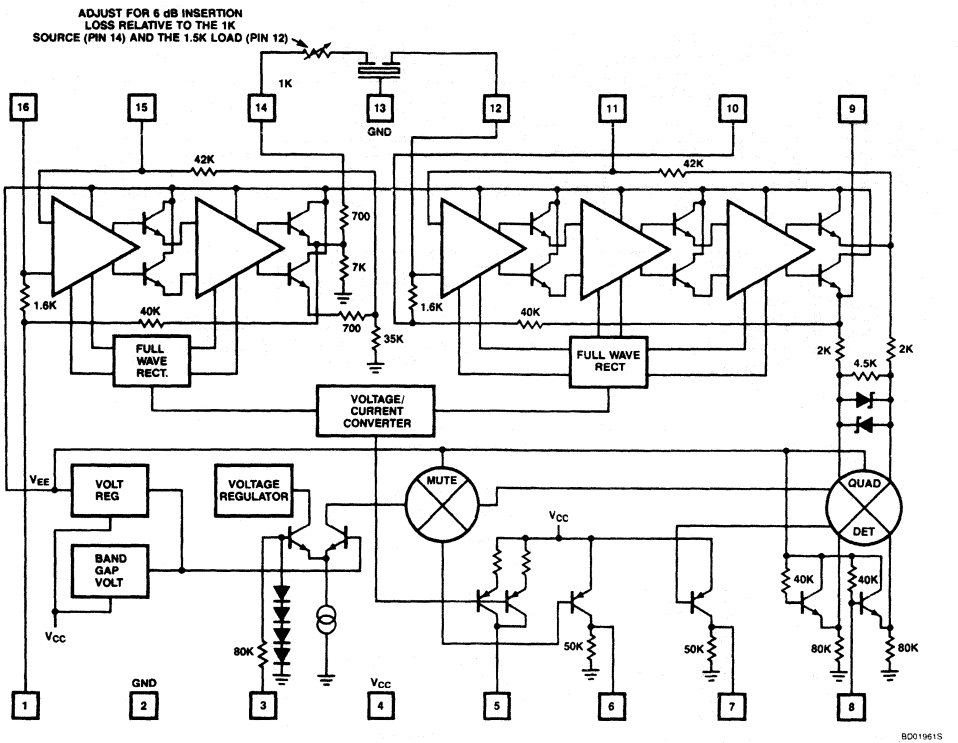


Figure 2. Equivalent Circuit

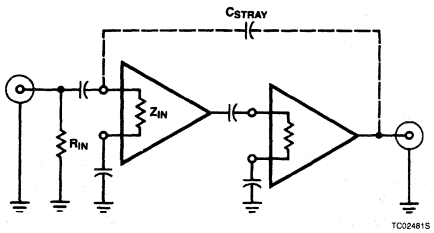
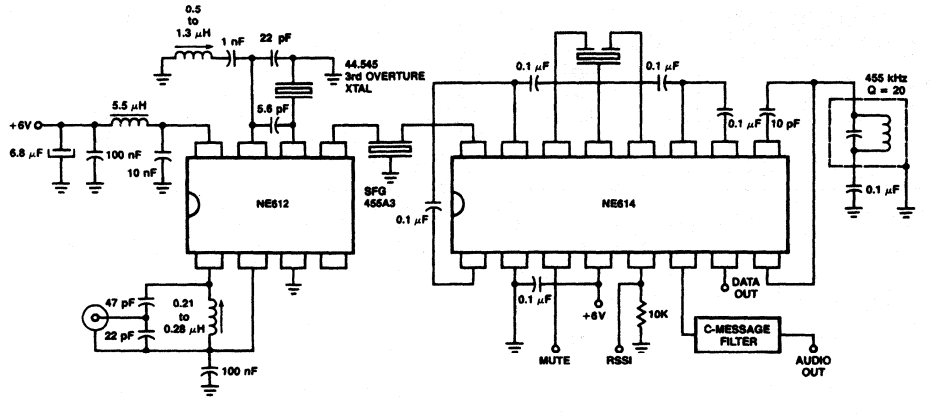


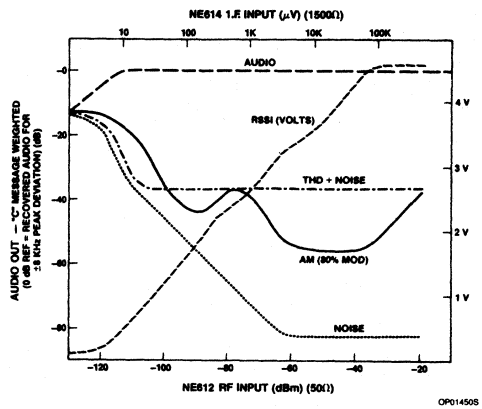
Figure 3. Considerations for Stability

The equivalent AC attenuation factor from the output to the input must be greater than 90dB or oscillation can occur. The input impedance of the device is nominally 1.5k. The stray layout capacitance is a frequency-dependent impedance so that as the frequency of operation or the value of stray capacitance increases, the output-to-input attenuation factor decreases. Keep stray capacitance low by using good RF layout technique. Sockets should be avoided above 455kHz.

Good RF layout is the proper way to avoid instability. However, if system constraints require, stability can be achieved by only using one of the limiting amplifiers, or by adding a resistance, R_{IN}, which will increase the attenuation factor.



a. NE614 Application Circuit



b. Typical Application Circuit Performance

Figure 4

Adding an input resistor is an easy way to reduce the attenuation factor, but may make correct termination of interstage filters difficult or impossible. At 455kHz instability should not be a problem if reasonable RF layout is used. Figure 4a indicates a 455kHz circuit configuration which should serve as a reasonable starting point for many applications. This circuit is configured for 46/49MHz cordless telephone.

Quadrature Detector

The detector of the NE614 is a four quadrant multiplier of the Gilbert cell type. It can be used for frequency or amplitude demodulation. Figure 4b indicates a typical quadrature FM configuration. Fully limited in-phase signal is applied to the multiplier internally. 90° phase phase shift is accomplished with the L/C tuned circuit connected directly to Pin 8 and and capacitively to Pin 9. Because of the DC bias of the NE614, the phase shift network must be returned to ground through a low impedance capacitor. Recovered signal is continuously available at Pin 7 or on a switched basis at Pin 6.

Table 1. System Parameters as Applied to Figure 4a

$\Delta\omega$	=	2π*8kHz
ω_0	=	2π*455kHz
CP	=	180pF
RPU	=	233K
RPL	=	40K
LP	=	644μH
Q	≈	20

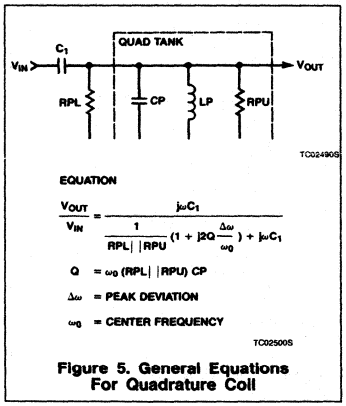


Figure 5. General Equations For Quadrature Coil

The quadrature coil or crystal/ceramic discriminator affects three system parameters: Bandwidth, linearity, and detected signal amplitude. Figure 6 shows three quadrature curves.

Curve A has the most narrow bandwidth and high peak-to-peak output versus frequency deviation corresponding to a high Q network. Curve C is very low Q with good linearity and shows how very large deviations can be processed. Curve B shows how the quadrature network can cause non-linearity in the detected output. A typical loaded Q for the 455kHz quadrature coil of Figure 4 is 20. Using the test circuit of Figure 4 with an input of −47dBm, the recovered audio is typically $90mV_{RMS}$ with −35dB distortion.

While the NE614 was designed principally for FM applications, the detector can be used for synchronous amplitude demodulation if the carrier is limited through the internal circuitry and AGC'd external to the device. The AGC'd signal is applied to Pin 8 instead of a quadrature signal. The signal strength indicator can control AGC. A low-pass filter on the output completes the demodulator. Figure 7 shows the equivalent circuit.

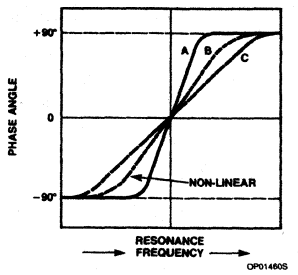


Figure 6. Quadrature

Audio Mute

An electronic switch permits muting or squelch of one of the demodulated outputs. The data (unmuted output) and audio (muted output) both have 50kΩ output impedance and their detected signals are 180 degrees out of phase with each other. The mute input (Pin 3) has a very high impedance and is compatible with three and five volt CMOS and TTL levels. Little or no DC level shift occurs after muting when the quadrature detector is adjusted to the IF center frequency. Muting will attenuate the audio signal by more than 60dB and no voltage spikes will be generated by muting.

Signal Strength Indicator

The logarithmic signal strength indicator is a current source output with maximum source current of 50μA. The signal strength indicator's transfer function is approximately 10μA per 20dB and is independent of IF frequency. The interstage filter must have a 6dB insertion loss to optimize slope linearity.

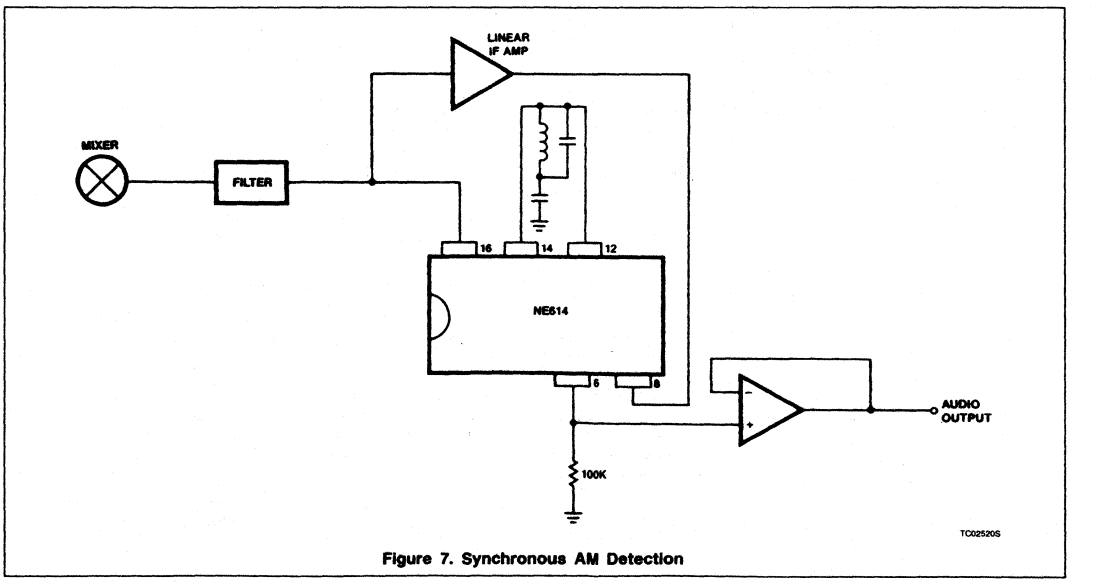


Figure 7. Synchronous AM Detection

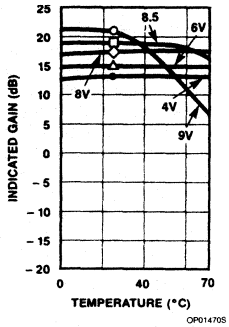


Figure 8. NE614 Indicated Gain vs Temperature and Voltage

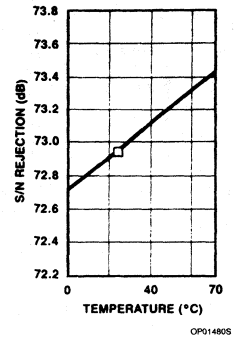


Figure 9. NE614 Signal-To-Noise Ratio vs Temperature

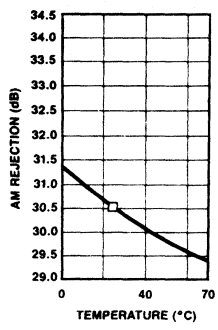


Figure 10. NE614 AM Rejection vs Temperature

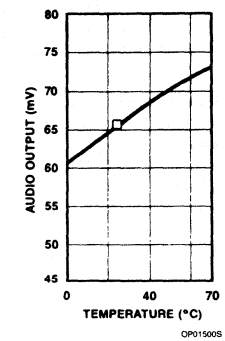


Figure 11. NE614 Audio Output vs Temperature

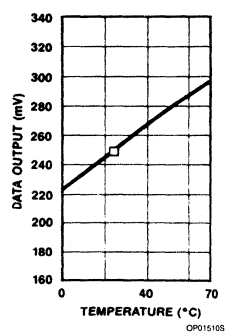


Figure 12. NE614 Data Output vs Temperature

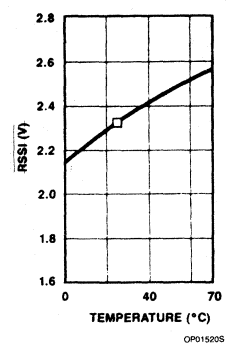


Figure 13. RSSI vs Temperature

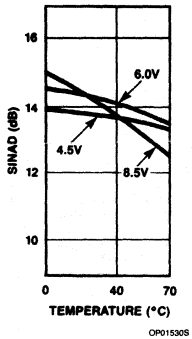


Figure 14. NE614 SINAD vs Temperature and V_{CC}

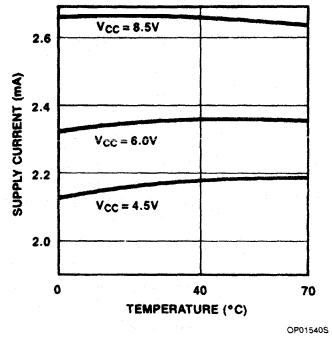


Figure 15. NE614 Supply Current vs Temperature

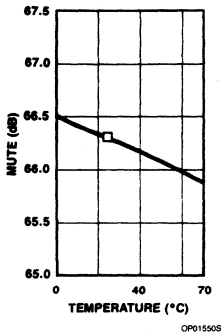


Figure 16. NE614 Muting vs Temperature

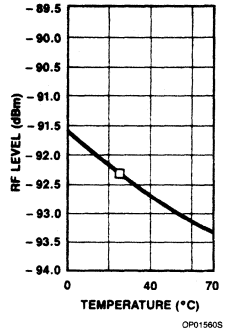


Figure 17. NE614 Limiting RF Level vs Temperature

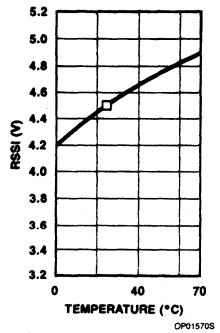


Figure 18. NE614 Large Signal Uncompensated RSSI Voltage vs Temperature

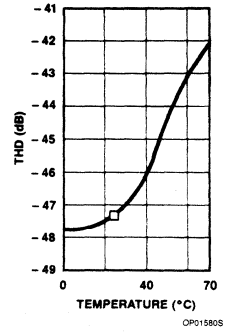


Figure 19. NE614 Total Harmonic Distortion vs Temperature

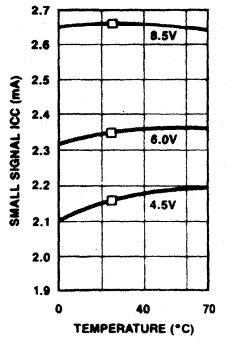


Figure 20. NE614 Supply Current vs Temperature and Voltage

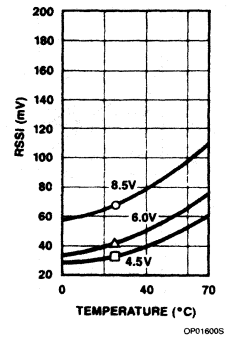


Figure 21. Small-Signal RSSI vs Temperature and Voltage

NE/SA5230
Low Voltage Operational Amplifier

Product Specification

Linear Products

DESCRIPTION

The NE5230 is a very low voltage operational amplifier that can perform with a voltage supply as low as 1.8V or as high as 15V. In addition, split or single supplies can be used, and the output will swing to ground when applying the latter. There is a bias adjusting pin which controls the supply current required by the device and thereby controls its power consumption. If the part is operated at ±0.9V supply voltages, the current required is only 110μA when the current control pin is left open. Even with this low power consumption, the device obtains a typical unity gain bandwidth of 180kHz. When the bias adjusting pin is connected to the negative supply, the unity gain bandwidth is typically 600kHz while the supply current is increased to 600μA. In this mode, the part will supply full power output beyond the audio range.

The NE5230 also has a unique input stage that allows the common-mode input range to go above the positive and below the negative supply voltages by 250mV. This provides for the largest possible input voltages for low voltage applications. The part is also internally-compensated to reduce external component count.

The NE5230 has a low input bias current of typically ±40nA, and a large open-loop gain of 125dB. These two specifications are beneficial when using the device in transducer applications. The large open-loop gain gives very accurate signal processing because of the large "excess" loop gain in a closed-loop system.

The output stage is a class AB type that can swing to within 100mV of the supply voltages for the largest dynamic range that is needed in many applications. The NE5230 is ideal for portable audio equipment and remote transducers because of its low power consumption, unity gain bandwidth, and 30nV/$\sqrt{Hz}$ noise specification.

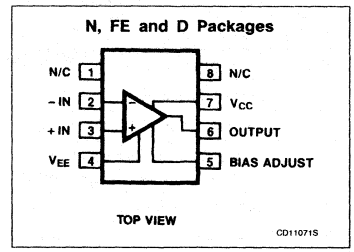
FEATURES

- **Works down to 1.8V supply voltages**
- **Adjustable supply current**
- **Low noise**
- **Common-mode includes both rails**
- **V_{OUT} within 100mV of both rails**

APPLICATIONS

- **Portable precision instruments**
- **Remote transducer amplifier**
- **Portable audio equipment**
- **Rail-to-rail comparators**
- **Half-wave rectification without diodes**
- **Remote temperature transducer with 4 to 20mA output transmission**

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO	0 to +70°C	NE5230D
8-Pin Ceramic DIP	0 to +70°C	NE5230FE
8-Pin Plastic DIP	0 to +70°C	NE5230N
8-Pin Plastic SO	−40°C to +85°C	SA5230D
8-Pin Ceramic DIP	−40°C to +85°C	SA5230FE
8-Pin Plastic DIP	−40°C to +85°C	SA5230N

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Single supply voltage	18	V
V_S	Dual supply voltage	±9	V
V_{IN}	Input voltage[1]	±9 (18)	V
	Differential input voltage[1]	$\pm V_S$	V
V_{CM}	Common-mode voltage (positive)	V_{CC} + 0.5	V
V_{CM}	Common-mode voltage (negative)	V_{EE} − 0.5	V
P_D	Power dissipation[2]	500	mW
T_J	Operating junction temperature[2]	150	°C
	Output short-circuit duration to either power supply pin[2, 3]	Indefinite	s
T_{STG}	Storage temperature	−65 to 150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	300	°C

NOTES:
1. Can exceed the supply voltages when $V_S \leqslant \pm 7.5V$ (15V).
2. The maximum operating junction temperature is 150°C. At elevated temperatures, devices must be derated according to the package thermal resistance and device mounting conditions.
   Derate above 25°C at the following rates:
   FE package at 6.7mW/°C
   N package at 9.5mW/°C
   D package at 6.25mW/°C
3. Momentary shorts to either supply are permitted in accordance to transient thermal impedance limitations determined by the package and device mounting conditions.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Single supply voltage	1.8 to 15	V
Dual supply voltage	±0.9 to ±7.5	V
Common-mode voltage (positive)	V_{CC} + 0.25	V
Common-mode voltage (negative)	V_{EE} − 0.25	V
Temperature		
NE grade	0 to 70	°C
SA grade	−40 to 85	°C

DC AND AC ELECTRICAL CHARACTERISTICS Unless otherwise specified, $\pm 0.9V \leqslant V_S \leqslant \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER		TEST CONDITIONS		BIAS	NE/SA5230			UNIT
						Min	Typ	Max	
V_{OS}	Offset voltage		$T_A = 25°C$		Any		0.4	3	mV
					Any		3	4	mV
V_{OS}	Drift				Any		2	5	µV/°C
I_{OS}	Offset current		$T_A = 25°C$		High		3	50	nA
			$T_A = 25°C$		Low		3	30	nA
					High			100	nA
					Low			60	nA
I_{OS}	Drift				High		0.5	1.4	nA/°C
					Low		0.3	1.4	nA/°C
I_B	Bias current		$T_A = 25°C$		High		40	150	nA
			$T_A = 25°C$		Low		20	60	nA
					High			200	nA
					Low			150	nA
I_B	Drift				High		2	4	nA/°C
					Low		2	4	nA/°C
I_S	Supply current		$V_S = \pm 0.9V$	$T_A = 25°C$	Low		110	160	µA
				$T_A = 25°C$	High		600	750	µA
					Low			250	µA
					High			800	µA
			$V_S = \pm 7.5V$	$T_A = 25°C$	Low		320	550	µA
				$T_A = 25°C$	High		1.1	1.6	mA
					Low			600	µA
					High			1.7	mA
V_{CM}	Common-mode input range		$V_{OS} \leqslant 6mV$, $T_A = 25°C$		Any	$V^- - 0.25$		$V^+ + 0.25$	V
					Any	V^-		V^+	V
CMRR	Common-mode rejection ratio		$V_S = \pm 7.5V$	$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$, $T_A = 25°C$	Any	85	95		dB
				$R_S = 10k\Omega$, $V_{CM} = \pm 7.5V$	Any	80			dB
PSRR	Power supply rejection ratio		$T_A = 25°C$		High	90	105		dB
			$T_A = 25°C$		Low	85	95		dB
					High	75			dB
					Low	80			dB
I_L	Load current	source	$V_S = \pm 7.5V$		Any	4	10		mA
		sink	$V_S = \pm 7.5V$		Any	5	15		mA
		source	$V_S = \pm 0.9V$		Any	1	5		mA
		sink	$V_S = \pm 0.9V$		Any	2	6		mA
		source	$V_S = \pm 0.9V$, $T_A = 25°C$		High	4	6		mA
		sink	$V_S = \pm 0.9V$, $T_A = 25°C$		High	5	7		mA
		source	$V_S = \pm 7.5V$, $T_A = 25°C$		High		16		mA
		sink	$V_S = \pm 7.5V$, $T_A = 25°C$		High		32		mA

DC AND AC ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise specified, $\pm 0.9V \leq V_S \leq \pm 7.5V$ or equivalent single supply, $R_L = 10k\Omega$, full input common-mode range, over full operating temperature range.

SYMBOL	PARAMETER	TEST CONDITIONS		BIAS	NE/SA5230			UNIT
					Min	Typ	Max	
A_{VOL}	Large-signal open-loop gain	$V_S = \pm 7.5V$	$R_L = 10k\Omega$, $T_A = 25°C$	High	120	2000		V/mV
			$R_L = 10k\Omega$, $T_A = 25°C$	Low	60	750		V/mV
				High	100			V/mV
				Low	50			V/mV
V_{OUT}	Output voltage swing	$V_S = \pm 0.9V$	$T_A = 25°C$, +SW	Any	750	800		mV
			$T_A = 25°C$, -SW	Any	750	800		mV
			+SW	Any	700			mV
			-SW	Any	700			mV
		$V_S = \pm 7.5V$	$T_A = 25°C$, +SW	Any	7.30	7.35		V
			$T_A = 25°C$, -SW	Any	-7.32	-7.35		V
			+SW	Any	7.25	7.30		V
			-SW	Any	-7.30	-7.35		V
SR	Slew rate	$T_A = 25°C$		High		0.25		V/μs
		$T_A = 25°C$		Low		0.09		V/μs
BW	Inverting unity gain bandwidth	$C_L = 100pF$, $T_A = 25°C$		High		0.6		MHz
		$C_L = 100pF$, $T_A = 25°C$		Low		0.25		MHz
θ_M	Phase margin	$C_L = 100pF$, $T_A = 25°C$		Any		70		Deg.
t_S	Settling time	$C_L = 100pF$, 0.1%		High		2		μs
		$C_L = 100pF$, 0.1%		Low		5		μs
V_{INN}	Input noise	$R_S = 0\Omega$, f = 1kHz		High		30		$nV/\sqrt{Hz}$
		$R_S = 0\Omega$, f = 1kHz		Low		60		$nV/\sqrt{Hz}$
THD	Total Harmonic Distortion	$V_S = \pm 7.5V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.003		%
		$V_S = \pm 0.9V$ $A_V = 1$, $V_{IN} = 500mV$, f = 1kHz		High		0.002		%

THEORY OF OPERATION

Input Stage

Operational amplifiers which are able to function at minimum supply voltages should have input and output stage swings capable of reaching both supply voltages within a few millivolts in order to achieve ease of quiescent biasing and to have maximum input/output signal handling capability. The input stage of the NE5230 has a common-mode voltage range that not only includes the entire supply voltage range, but also allows either supply to be exceeded by 250mV without increasing the input offset voltage by more than 6mV. This is unequalled by any other operational amplifier today.

In order to accomplish the feat of rail-to-rail input common-mode range, two emitter-coupled differential pairs are placed in parallel so that the common-mode voltage of one can reach the positive supply rail and the other can reach the negative supply rail. The simplified schematic of Figure 1 shows how the complementary emitter-coupler transistors are configured to form the basic input stage cell. Common-mode input signal voltages in the range from 0.8V above V_{EE} to V_{CC} are handled completely by the NPN pair, Q3 and Q4, while common-mode input signal voltages in the range of V_{EE} to 0.8V above V_{EE} are processed only by the PNP pair, Q1 and Q2. The intermediate range of input voltages requires that both the NPN and PNP pairs are operating. The collector currents of the input transistors are summed by the current combiner circuit composed of transistors Q8 through Q11 into one output current. Transistor Q8 is connected as a diode to ensure that the outputs of Q2 and Q4 are properly subtracted from those of Q1 and Q3.

The input stage was designed to overcome two important problems for rail-to-rail capability. As the common-mode voltage moves from the range where only the NPN pair was operating to where both of the input pairs were operating, the effective transconductance would change by a factor of two. Frequency compensation for the ranges where one input pair was operating would, of course, not be optimal for the range where both pairs were operating. Secondly, fast changes in the common-mode voltage would abruptly saturate and restore the emitter current sources, causing transient distortion. These problems were overcome by assuring that only the input transistor pair which is able to function properly is active. The NPN pair is normally activated by the current source I_{B1} through Q5 and the current mirror Q6 and Q7, assuming the PNP pair is non-conducting. When the common-mode input voltage passes below the reference voltage, $V_{B1} = 0.8V$ at the base of Q5, the emitter current is gradually steered toward the PNP pair, away from the NPN pair. The transfer of the emitter currents between the complementary input pairs occurs in a voltage range of about 120mV around the reference voltage V_{B1}. In this way the sum of the emitter currents for each of the NPN and PNP transistor pairs is kept constant; this ensures that the transconductance of the parallel combination will be constant, since the transconductance of bipolar transistors is proportional to their emitter currents.

An essential requirement of this kind of input stage is to minimize the changes in input offset voltage between that of the NPN and PNP transistor pair which occurs when the input common-mode voltage crosses the internal reference voltage, V_{B1}. Careful circuit layout with a cross-coupled quad for each input pair has yielded a typical input offset voltage of less than 0.3mV and a change in the input offset voltage of less than 0.1mV.

Output Stage

Processing output voltage swings that nominally reach to less than 100mV of either supply voltage can only be achieved by a pair of complementary common-emitter connected transistors. Normally, such a configuration causes complex feed-forward signal paths that develop by combining biasing and driving which can be found in previous low supply voltage designs. The unique output stage of the NE5230 separates the functions of driving and biasing, as shown in the simplified schematic of Figure 2, and has the advantage of a shorter signal path which leads to increasing the effective bandwidth.

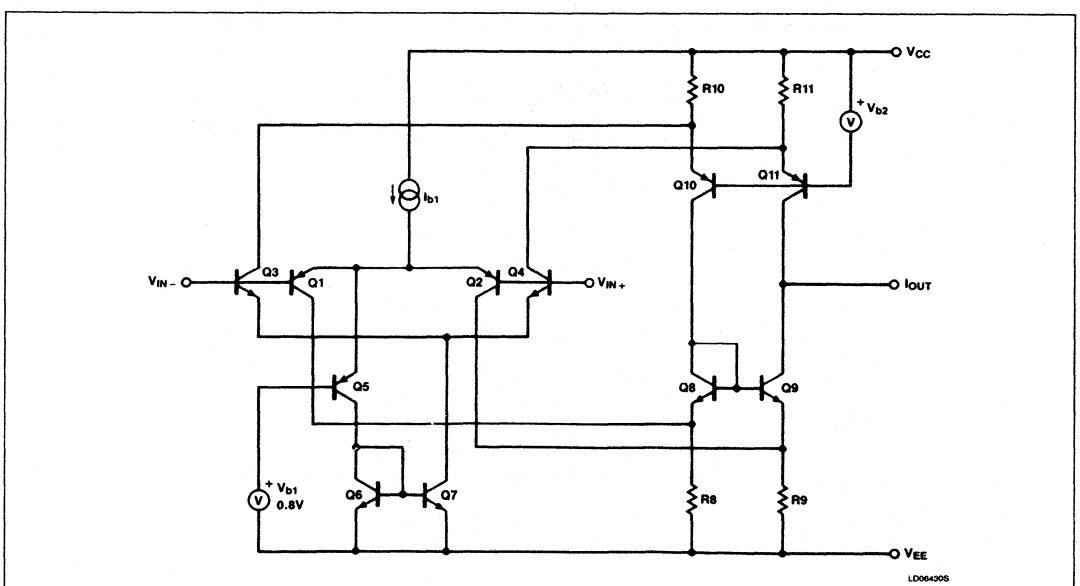


Figure 1. Input Stage

This output stage consists of two parts: the Darlington output transistors and the class AB control regulator. The output transistor Q3 connected with the Darlington transistors Q4 and Q5 can source up to 10mA to an output load. The output of NPN Darlington connected transistors Q1 and Q2 together are able to sink an output current of 10mA. Accurate and efficient class AB control is necessary to insure that none of the output transistors are ever completely cut off. This is accomplished by the differential amplifier (formed by Q8 and Q9) which controls the biasing of the output transistors. The differential amplifier compares the summed voltages across two diodes, D1 and D2, at the base of Q8 with the summed voltages across the base-emitter diodes of the output transistors Q1 and Q3. The base-emitter voltage of Q3 is converted into a current by Q6 and R6 and reconverted into a voltage across the base-emitter diode of Q7 and R7. The summed voltage across the base-emitter diodes of the output transistors Q3 and Q1 is proportional to the logarithm of the product of the push and pull currents I_{OP} and I_{ON}, respectively. The combined voltages across diodes D1 and D2 are proportional to the logarithm of the square of the reference current I_{B1}. When the diode characteristics and temperatures of the pairs Q1, D1 and Q3, Q2 are equal, the relation $I_{OP} \times I_{ON} = I_{B1} \times I_{B1}$ is satisfied.

Separating the functions of biasing and driving prevents the driving signals from becoming delayed by the biasing circuit. The output Darlington transistors are directly accessible for in-phase driving signals on the bases of Q5 and Q2. This is very important for simple high-frequency compensation. The output transistors can be high-frequency compensated by Miller capacitors CM1A and CM1B connected from the collectors to the bases of the output Darlington transistors.

A general-purpose op amp of this type must have enough open-loop gain for applications when the output is driving a low resistance load. The NE5230 accomplishes this by inserting an intermediate common-emitter stage between the input and output stages. The three stages provide a very large gain, but the op amp now has three natural dominant poles — one at the output of each common-emitter stage. Frequency compensation is implemented with a simple scheme of nested, pole-splitting Miller integrators. The Miller capacitors CM1A and CM1B are the first part of the nested structure, and provide compensation for the output and intermediate stages. A second pair of Miller integrators provide pole-splitting compensation for the pole from the input stage and the pole resulting from the compensated combination of poles from the intermediate and output stages. The result is a stable, internally-compensated op amp with a phase margin of 70 degrees.

THERMAL CONSIDERATIONS

When using the NE5230, the internal power dissipation capabilities of each package should be considered. Philips does not recommend operation at die temperatures above 110°C in the SO package because of its inherently smaller package mass. Die temperatures of 150°C can be tolerated in all the other packages. With this in mind, the following equation can be used to estimate the die temperature:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

Where $T_A \equiv$ Ambient Temperature
T_J = Die Temperature
$P_D \equiv$ Power Dissipation
$= (I_{CC} \times V_{CC})$
$\theta_{JA} \equiv$ Package thermal resistance
= 270°C/W for SO-8 in PC board mounting

See the packaging section for information regarding other methods of mounting.

θ_{JA} = 100°C/W for the plastic DIP;
θ_{JA} = 110°C/W for the ceramic DIP.

The maximum supply voltage for the part is 15V and the typical supply current is 1.1mA (1.6mA max). For operation at supply voltages other than the maximum, see the data

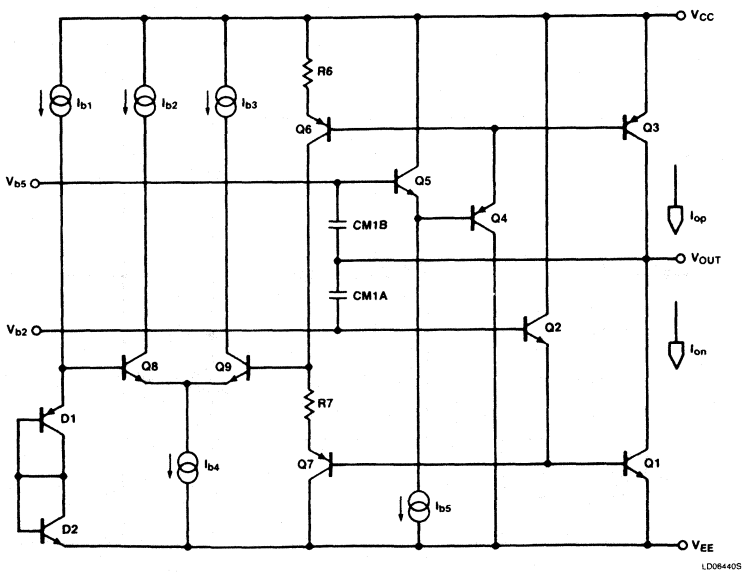


Figure 2. Output Stage

sheet for I_{CC} versus V_{CC} curves. The supply current is somewhat proportional to temperature and varies no more than 100μA between 25°C and either temperature extreme.

Operation at higher junction temperatures than that recommended is possible but will result in lower MTBF (Mean Time Between Failures). This should be considered before operating beyond recommended die temperature because of the overall reliability degradation.

DESIGN TECHNIQUES AND APPLICATIONS

The NE5230 is a very user-friendly amplifier for an engineer to design into any type of system. The supply current adjust pin (Pin 5) can be left open or tied through a pot or fixed resistor to the most negative supply (i.e., ground for single supply or to the negative supply for split supplies). The minimum supply current is achieved by leaving this pin open. In this state it will also decrease the bandwidth and slew rate. When tied directly to the most negative supply, the device has full bandwidth, slew rate and I_{CC}. The programming of the current-control pin depends on the trade-offs which can be made in the designer's application. The graph in Figure 3 will help by showing bandwidth versus I_{CC}. As can be seen, the supply current can be varied anywhere over the range of 100μA to 600μA for a supply voltage of 1.8V. An external resistor can be inserted between the current control pin and the most negative supply. The resistor can be selected between 1Ω to 100kΩ to provide any required supply current over the indicated range. In addition, a small varying voltage on the bias current control pin could be used for such exotic things as changing the gain-bandwidth for voltage controlled low pass filters or amplitude modulation. Furthermore, control over the slew rate and the rise time of the amplifier can be obtained in the same manner. This control over the slew rate also changes the settling time and overshoot in pulse response applications. The settling time to 0.1% changes from 5μs at low bias to 2μs at high bias. The supply current control can also be utilized for wave-shaping applications such as for pulse or triangular waveforms. The gain-bandwidth can be varied from between 250kHz at low bias to 600kHz at high bias current. The slew rate range is 0.08V/μs at low bias and 0.25V/μs at high bias.

The full output power bandwidth range for V_{CC} equals 2V, is above 40kHz for the maximum bias current setting and greater than 10kHz at the minimum bias current setting.

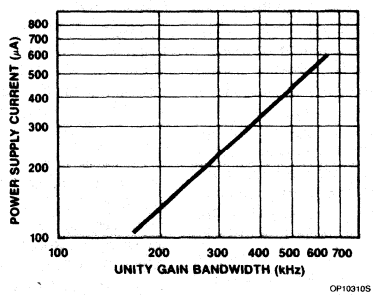
If extremely low signal distortion (< 0.05%) is required at low supply voltages, exclude the common-mode crossover point (V_{B1}) from the common-mode signal range. This can be accomplished by proper bias selection or by using an inverting amplifier configuration.

Most single supply designs necessitate that the inputs to the op amp be biased between V_{CC} and ground. This is to assure that the input signal swing is within the working common-mode range of the amplifier. This leads to another helpful and unique property of the NE5230 that other CMOS and bipolar low voltage parts cannot achieve. It is the simple fact that the input common-mode voltage can go beyond either the positive or negative supply voltages. This benefit is made very clear in a non-inverting voltage-follower configuration. This is shown in Figure 4 where the input sine wave allows an undistorted output sine wave which will swing less than 100mV of either supply voltage. Many competitive parts will show severe clipping caused by input common-mode limitations. The NE5230 in this configuration offers more freedom for quiescent biasing of the inputs close to the positive supply rail where similar op amps would not allow signal processing.

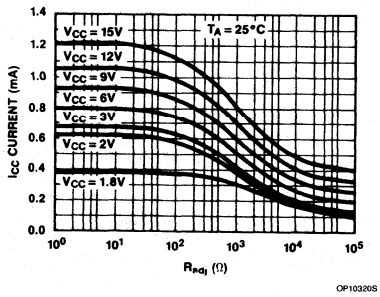
There are not as many considerations when designing with the NE5230 as with other devices. Since the NE5230 is internally-compensated and has a unity gain-bandwidth of 600kHz, board layout is not so stringent as for very high frequency devices such as the NE5205. The output capability of the NE5230 allows it to drive relatively high capacitive loads and small resistive loads. The power supply pins should be decoupled with a low-pass RC network as close to the supply pins as possible to eliminate 60Hz and other external power line noise, although the power supply rejection ratio (PSRR) for the part is very high. The pinout for the NE5230 is the same as the standard single op amp pinout with the exception of the bias current adjusting pin.

REMOTE TRANSDUCER WITH CURRENT TRANSMISSION

There are many ways to transmit information along two wires, but current transmission is



a. Unity Gain Bandwidth vs Power Supply Current for $V_{CC} = \pm 0.9V$



b. I_{CC} Current vs Bias Current Adjusting Resistor for Several Supply Voltages

Figure 3

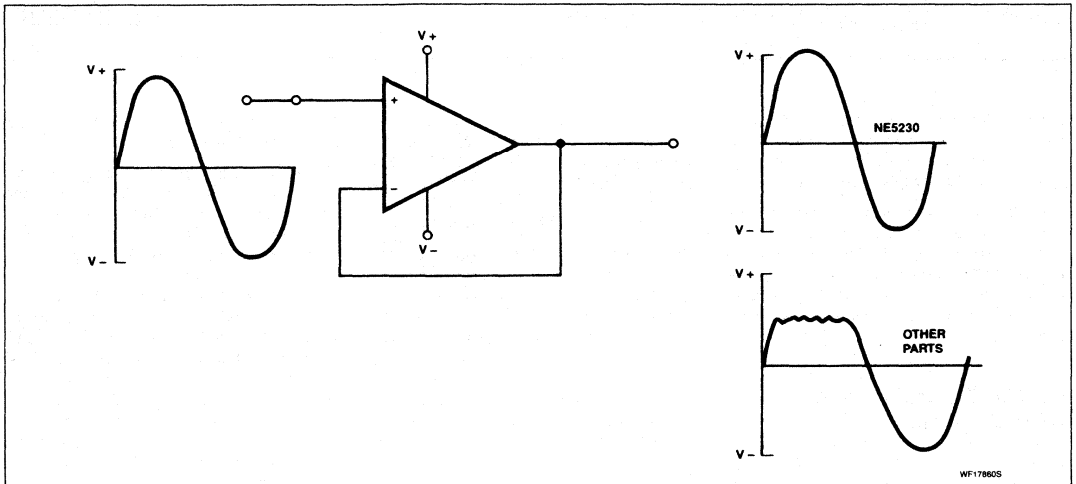


Figure 4. In a Non-Inverting Voltage-Follower Configuration, the NE5230 will Give Full Rail-to-Rail Swing. Other Low Voltage Amplifiers will not Because they are Limited by their Input Common-Mode Range and Output Swing Capability

the most beneficial when the sensing of remote signals is the aim. It is further enhanced in the form of 4 to 20mA information which is used in many control-type systems. This method of transmission provides immunity from line voltage drops, large load resistance variations, and voltage noise pickup. The zero reference of 4mA not only can show if there is a break in the line when no current is flowing, but also can power the transducer at the remote location. Usually the transducer itself is not equipped to provide for the current transmission. The unique features of the NE5230 can provide high output current capability coupled with low power consumption. It can be remotely connected to the transducer to create a current loop with minimal external components. The circuit for this is shown in Figure 5. Here, the part is configured as a voltage-to-current, or transconductance amplifier. This is a novel circuit that takes advantage of the NE5230's large open-loop gain. In AC applications, the load current will decrease as the open-loop gain rolls off in magnitude. The low offset voltage and current sinking capabilities of the NE5230 must also be considered in this application.

The NE5230 circuit shown in Figure 5 is a pseudo transistor configuration. The inverting input is equivalent to the "base," the point where V_{EE} and the non-inverting input meet is the "emitter," and the connection after the output diode meets the V_{CC} pin is the collector. The output diode is essential to keep the output from saturating in this configuration. From here it can be seen that the base and emitter form a voltage-follower and the voltage present at R_C must equal the input voltage present at the inverting input. Also, the emitter and collector form a current-follower and the current flowing through R_C is equivalent to the current through R_L and the amplifier. This sets up the current loop. Therefore, the following equation can be formulated for the working current transmission line. The load current is:

$$I_L = V_{IN}/R_C \quad (2)$$

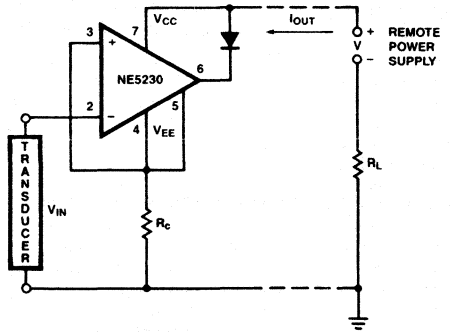
and proportional to the input voltage for a set R_C. Also, the current is constant no matter what load resistance is used while within the operating bandwidth range of the op amp. When the NE5230's supply voltage falls past a certain point, the current cannot remain constant. This is the "voltage compliance" and is very good for this application because of the near rail output voltage. The equation that determines the voltage compliance as well as the largest possible load resistor for the NE5230 is as follows:

$$R_{L\ max} = [V_{remote\ supply}) - V_{CC\ min} - V_{IN\ max}]/I_L \quad (3)$$

Where $V_{CC\ min}$ is the worst-case power supply voltage (approximately 1.8V) that will still keep the part operational. As an example, when using a 15V remote power supply, a current sensing resistor of 1Ω, and an input voltage (V_{IN}) of 20mV, the output current (I_L) is 20mA. Furthermore, a load resistance of zero to approximately 650Ω can be inserted in the loop without any change in current when the bias current-control pin is tied to the negative supply pin. The voltage drop across the load and line resistance will not affect the NE5230 because it will operate down to 1.8V. With a 15V remote supply, the voltage available at the amplifier is still enough to power it with the maximum 20mA output into the 650Ω load.

What this means is that several instruments, such as a chart recorder, a meter, or a controller, as well as a long cable, can be connected in series on the loop and still obtain accurate readings if the total resistance does not exceed 650Ω. Furthermore, any variation of resistance in this range will not change the output current.

Any voltage output type transducer can be used, but one that does not need external DC voltage or current excitation to limit the maximum possible load resistance is preferable. Even this problem can be surmounted if the supply power needed by the transducer is compatible with the NE5230. The power goes up the line to the transducer and amplifier while the transducer signal is sent back via the current output of the NE5230 transconductance configuration. The voltage range on the input can be changed for transducers that produce a large output by simply increasing the current sense resistor to get the corresponding 4 to 20mA output current. If a very long line is used which causes high line resistance, a current repeater could be inserted into the line. The same configuration of Figure 5 can be used

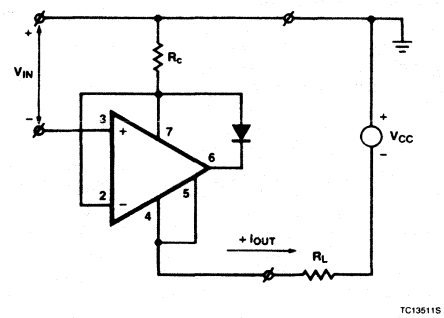


NOTES:
1. $I_{OUT} = V_{IN/RC}$
2. $R_{L\ max} \simeq \frac{V_{REMOTE} - 1.8V - V_{IN\ max}}{I_{OUT}}$

For $R_C = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

a. The NE5230 as a Remote Transducer Transconductance Amp With 4 – 20mA Current Transmission Output Capability



b. The Same Type of Circuit as Figure 5a, but for Sourcing Current to the Load

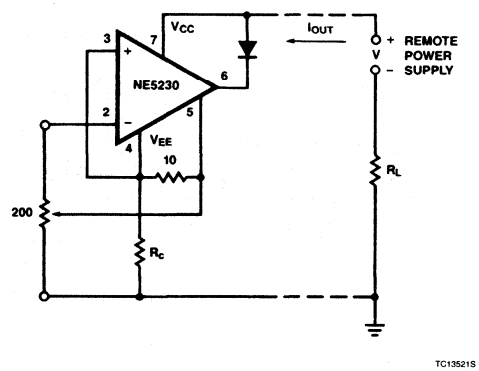
Figure 5

with exception of a resistor across the input and line ground to convert the current back to voltage. Again, the current sensing resistor will set up the transconductance and the part will receive power from the line.

TEMPERATURE TRANSDUCER

A variation on the previous circuit makes use of the supply current control pin. The voltage present at this pin is proportional to absolute temperature (PTAT) because it is produced by the amplifier bias current through an internal resistor divider in a PTAT cell. If the control pin is connected to the input pin, the NE5230 itself can be used as a temperature transducer. If the center tap of a resistive pot is connected to the control pin with one side to ground and the other to the inverting input, the voltage can be changed to give different temperature versus output current conditions (see Figure 6). For additional control, the output current is still proportional to the input voltage differential divided by the current sense resistor.

When using the NE5230 as a temperature transducer, the thermal considerations in the previous section must be kept in mind.



NOTES:
1. $I_{OUT} = V_{IN/RC}$
2. $R_L Max \simeq \frac{V_{REMOTE} - 1.8V - V_{IN}Max}{I_{OUT}}$

For $RC = 1\Omega$

I_{OUT}	V_{IN}
4mA	4mV
20mA	20mV

Figure 6. NE5230 Remote Temperature Transducer Utilizing 4 – 20mA Current Transmission. This Application Shows the use of the Accessibility of the PTAT Cell in the Device to Make the Part, Itself, a Transducer

HALF-WAVE RECTIFIER WITH RAIL-TO-GROUND OUTPUT SWING

Since the NE5230 input common-mode range includes both positive and negative supply rails and the output can also swing to either supply, achieving half-wave rectifier functions in either direction becomes a simple task. All that is needed are two external resistors; there is no need for diodes or matched resistors. Moreover, it can have either positive- or negative-going outputs, depending on the way the bias is arranged. This can be seen in Figure 7. Circuit (a) is biased to ground, while circuit (b) is biased to the positive supply. This rather unusual biasing does not cause any problems with the NE5230 because of the unique internal saturation detectors incorporated into the part to keep the PNP and NPN output transistors out of "hard" saturation. It is therefore relatively quick to recover from a saturated output condition. Furthermore, the device does not have parasitic current draw when the output is biased to either rail. This makes it possible to bias the NE5230 into "saturation" and obtain half-wave rectification with good recovery. The simplicity of biasing and the rail-to-ground half-sine wave swing are unique to this device. The circuit gain can be changed by the standard op amp gain equations for an inverting configuration.

It can be seen in these configurations that the op amp cannot respond to one-half of the incoming waveform. It cannot respond because the waveform forces the amplifier to swing the output beyond either ground or the positive supply rail, depending on the biasing, and, also, the output cannot disengage during this half cycle. During the other half cycle, however, the amplifier achieves a half-wave that can have a peak equal to the total supply voltage. The photographs in Figure 8 show the effect of the different biasing schemes, as well as the wide bandwidth (it works over the full audio range), that the NE5230 can achieve in this configuration.

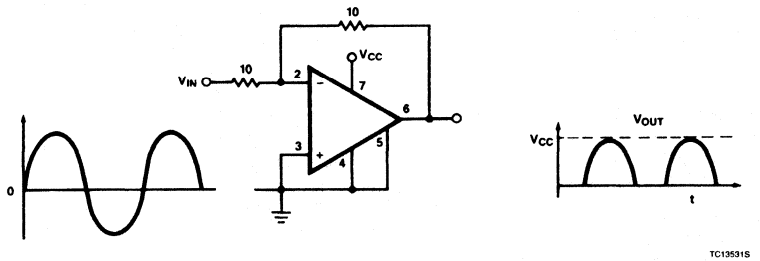
By adding another NE5230 in an inverting summer configuration at the output of the half-wave rectifier, a full-wave can be realized. The values for the input and feedback resistors must be chosen so that each peak will have equal amplitudes. A table for calculating values is included in Figure 9. The summing network combines the input signal at the half-wave and adds it to double the half-wave's output, resulting in the full-wave. The output waveform can be referenced to the supply or ground, depending on the half-wave configuration. Again, no diodes are needed to achieve the rectification.

This circuit could be used in conjunction with the remote transducer to convert a received AC output signal into a DC level at the full-wave output for meters or chart recorders that need DC levels.

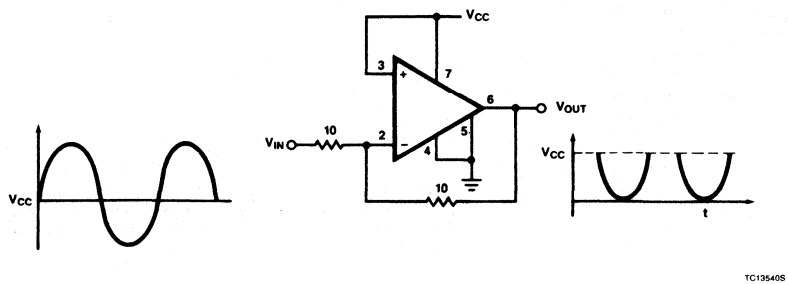
CONCLUSION

The NE5230 is a versatile op amp in its own right. The part was designed to give low voltage and low power operation without the limitations of previously available amplifiers that had a multitude of problems. The previous application examples are unique to this amplifier and save the user money by excluding various passive components that would have been needed if not for the NE5230's special input and output stages.

The NE5230 has a combination of novel specifications which allows the designer to implement it easily into existing low-supply voltage designs and to enhance their performance. It also offers the engineer the freedom to achieve greater amplifier system design goals. The low input referenced noise voltage eases the restrictions on designs



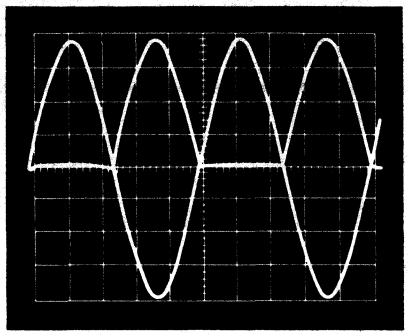
a. Rail-to-Ground Output Swing Referenced to Ground



b. Negative-Going Output Referenced to V_{CC}

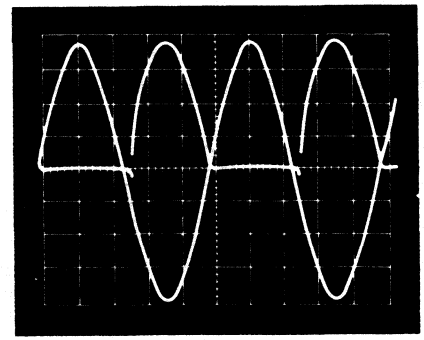
Figure 7. Half-Wave Rectifier With Positive-Going Output Swings

where S/N ratios are important. The wide full-power bandwidth and output load handling capability allow it to fit into portable audio applications. The truly ample open-loop gain and low power consumption easily lend themselves to the requirements of remote transducer applications. The low, untrimmed typical offset voltage and low offset currents help to reduce errors in signal processing designs. The amplifier is well isolated from changes on the supply lines by its typical power supply rejection ratio of 105dB.



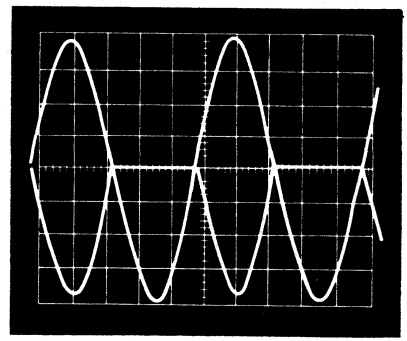
WF17870S

500mV/DIV 200μS/DIV
Biased to Ground



WF17880S

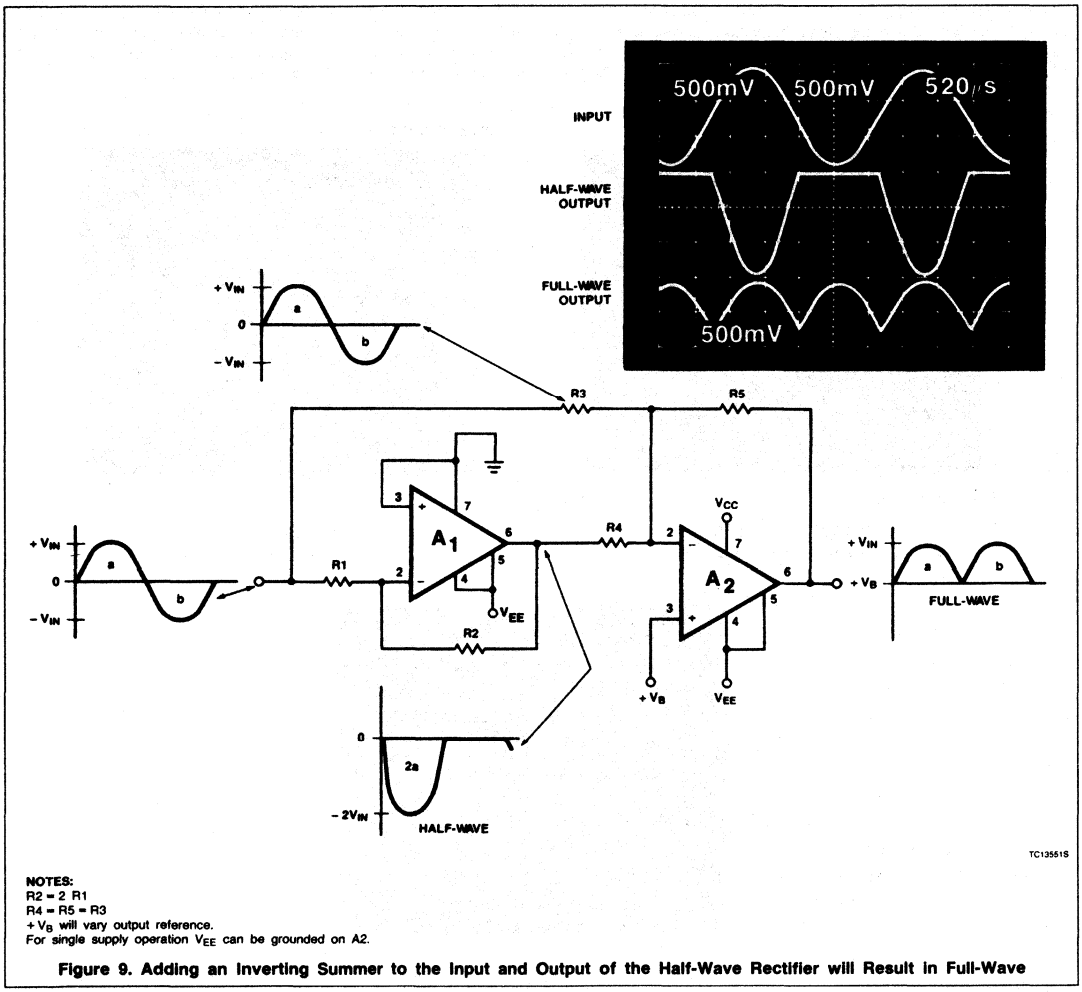
500mV/DIV 20μS/DIV
Biased to Ground



WF17890S

500mV/DIV 20μS/DIV
Biased to Positive Rail

Figure 8. Performance Waveforms for the Circuits in Figure 7. Good Response is Shown at 1 and 10kHz for Both Circuits Under Full Swing With a 2V Supply



NOTES:
R2 = 2 R1
R4 = R5 = R3
+V_B will vary output reference.
For single supply operation V_{EE} can be grounded on A2.

Figure 9. Adding an Inverting Summer to the Input and Output of the Half-Wave Rectifier will Result in Full-Wave

REFERENCES

Johan H. Huijsing, "Multi-stage Amplifier with Capacitive Nesting for Frequency Compensation," U.S. Patent Application Serial No. 602.234, filed April 19, 1984.

Bob Blauschild, "Differential Amplifier with Rail-to-Rail Capability," U.S. Patent Application Serial No. 525.181, filed August 23, 1983.

Operational Amplifiers — Characteristics and Applications, Robert G. Irvine, Prentice-Hall, Inc., Englewood Cliffs, NJ 07632, 1981.

Transducer Interface Handbook — A Guide to Analog Signal Conditioning, Edited by Daniel H. Sheingold, Analog Devices, Inc., Norwood, MA 02062, 1981.

LOW COST SPEECH DEMONSTRATION BOARD

GENERAL DESCRIPTION

The low cost speech demonstration board is designed to add voice output to existing card based electronic equipment with the minimum of additional effort and components. The majority of components used are of the CMOS type with low power consumption making the board suitable for battery operation.

Applications include speech evaluation and speech demonstration.

FEATURES

- PCF8200 speech synthesizer
  - Male and female speech of very high quality
  - CMOS technology
  - Extended operating temperature range
  - Programmable speaking speed
- Low current consumption
  - All major components use CMOS technology (PCF8200, 80C39 and 27C64)
- Very large vocabulary up to 12 minutes
  - 4 EPROM sockets
  - EPROM selection for 27C16 to 27C256
  - Low data rates for synthesizer (average 1500 bits per second)
- Easy interfacing
  - 8-bit parallel data bus/key switch input
  - Volume control, speaker connection
  - Control signals (e.g. RESET, BUSY etc etc)
- Simple operating modes
  - ROM selection
  - Word sequence within a ROM
  - Repeat last utterence
  - Control software is readily customizeable
  - To implement parameter download from external source
- Single Eurocard size PC board
- Single +5 V supply
- Low cost

APPLICATIONS

- OEM design-in
- May be simply used with many card systems for speech evaluation
- Speech demonstration
  - Particularly simple when used with the OM8201 (Speech Demonstration Box)

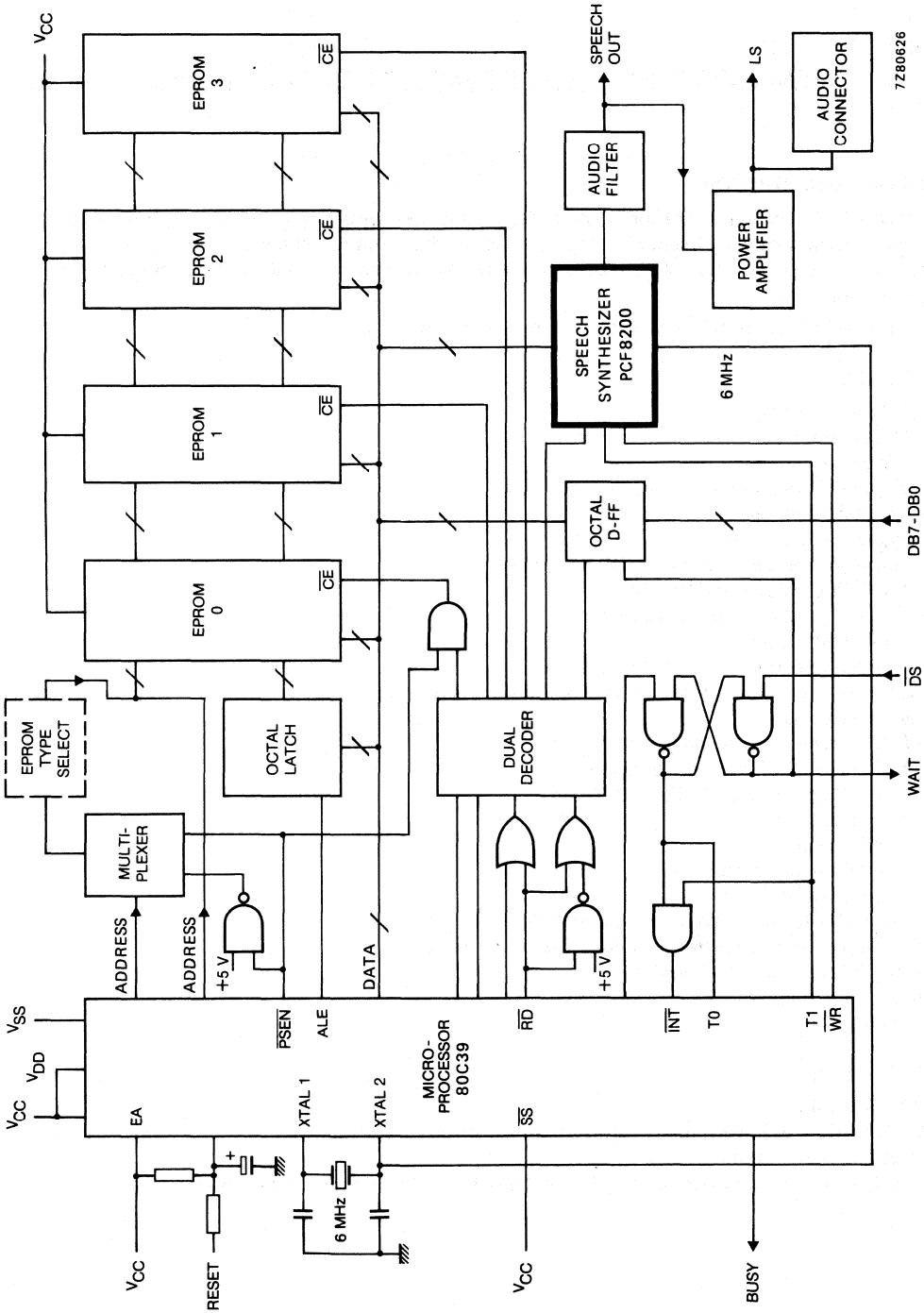


Fig. 1 Block diagram.

OPERATION

HARDWARE DESCRIPTION

The main controlling microprocessor is an 80C39 running at 6 MHz. This device supplies all of the main controlling signals for the board operation and the interfacing to any external system.
Four sockets are provided for EPROMS which contain speech coding. These may be 27C16 types, through to 27C256 types; the sockets will be a low insertion force type to allow for easy customizing.
The board will be supplied with one socket occupied by a 27C64 which will contain the control program and some speech examples. All four EPROM sockets must contain the same EPROM type.

The speech synthesizer PCF8200 converts the coding into a speech output. This synthesizer has been designed to simulate the human vocal tract using five formants for male and four formants for female speech. Periodic updating of the parameters for these formants can produce very high quality speech.

The output of the synthesizer can be fed into an audio amplifier, TDA7050, via a resistor-capacitor filter network which provides a frequency cut-off above 5 kHz of about 25 dB. The configuration of the audio amplifier used on this board gives an output of 140 mW peak power into a 25 Ω speaker from a 5 V supply.

Connections are made to the board via a standard DIN/IEC connector. This allows access to the 8-bit parallel data bus so that speech coding from an external source may be used, if implemented, and allows the selection of speech phrases by an external system, such as a microcomputer or even a bank of switches. The same connector also permits the addition of a volume control, loudspeaker, a high impedance audio output, and power supply. The control signals RESET, BUSY, WAIT and DS are also taken to the outside of the board. There is also a loudspeaker plug on the board.

All components are contained on a standard single Eurocard, and therefore suitable for rack mounted equipment.

SOFTWARE DESCRIPTION

All the software required to operate the board is contained in the only EPROM supplied. The software is written in modular from so that it is possible for a customer to alter or add to any particular function which suits his applications. An industrial standard microprocessor was chosen so that readily available development systems could be used to facilitate this modification.

There are four main modes of operation:

- ROM Selection
- Word Sequence
- Repeat Word
- Speaking Speed Selection

These modes are all controlled by software.

ROM Selection mode permits access to an individual EPROM and pronounces the first utterence from that EPROM.

Word Sequence gives the next word (activated by repeated access to the same EPROM) and if continually exercised will keep looping on the words in that EPROM.

The Repeat Word command allows indefinate repetition of the last utterance pronounced.

The Speaking Speed Selection allows the utterence to be pronounced at a different speed.

The software also controls the address sequencing within the utterance and ensures that the required data is supplied to the synthesizer.

There are also some examples of words/utterences encoded in the remainder of the supplied EPROM. These words are intended for demonstration purposes and will show the features of the synthesizer when selected. The main features being illustrated are:

- Male speech in several languages
- Female speech in several languages
- Programmable speaking speed

ORDERING INFORMATION

Product name: Low Cost Speech Demonstration Board

Type number: OM8200

Ordering code: 9337 541 30000

Orders should be placed with your local Philips/Signetics agency.

SPEECH DEMONSTRATION BOX

GENERAL DESCRIPTION

Speech demonstration box OM8201 is designed to be used in conjunction with the low cost speech demonstration board OM8200. The box contains all the necessary components to drive the board. The combination of these two components make an extremely attractive demonstration unit.

FEATURES

- Low cost
- Can use unmodified OM8200 board which allows access to all features of the OM8200
- Single + 9 V supply
  - Low power consumption therefore permits battery operation
  - External power supplies may also be used
  - Voltage is regulated and dropped to a standard + 5 V for the OM8200 board
- Simple mechanical construction
  - Allows easy access to the OM8200 for changing EPROMS
- Contains all peripherals needed to drive the OM8200

HARDWARE DESCRIPTION

The box contains a set of eight keypad switches which are connected to the data bus. Four switches can select which EPROM your speech data is derived from. Repeated pressing of an EPROM switch increments the expression number which will be uttered. To repeat the last expression, a separate switch must be activated.

It is possible in the PCF8200 to change the rate of speaking to 73%, 123% or 145% of the normal speed. A switch has been included on the box which will sequence through the speed options making the same utterance every time.

One of the two remaining switches is the master reset for the program and the other is for future enhancements of the box.

Included in the box are, the volume control for the amplifier, the loudspeaker, and a high impedance audio output.

The final piece of electronics is the power supply. This can be supplied from a + 9 V internal battery or from a + 9 V external supply. The + 9 V is regulated to a + 5 V supply which is then fed to other parts of the box and to the OM8200.

The box is of simple construction and allows easy access to the OM8200 for changing of EPROMS.

SOFTWARE DESCRIPTION

There is no software in the OM8201. The software of the OM8200 may be used in an unmodified form without any problems. However, if changes have been made to the control program of the OM8200 then different functions for the switches of the box can be achieved.

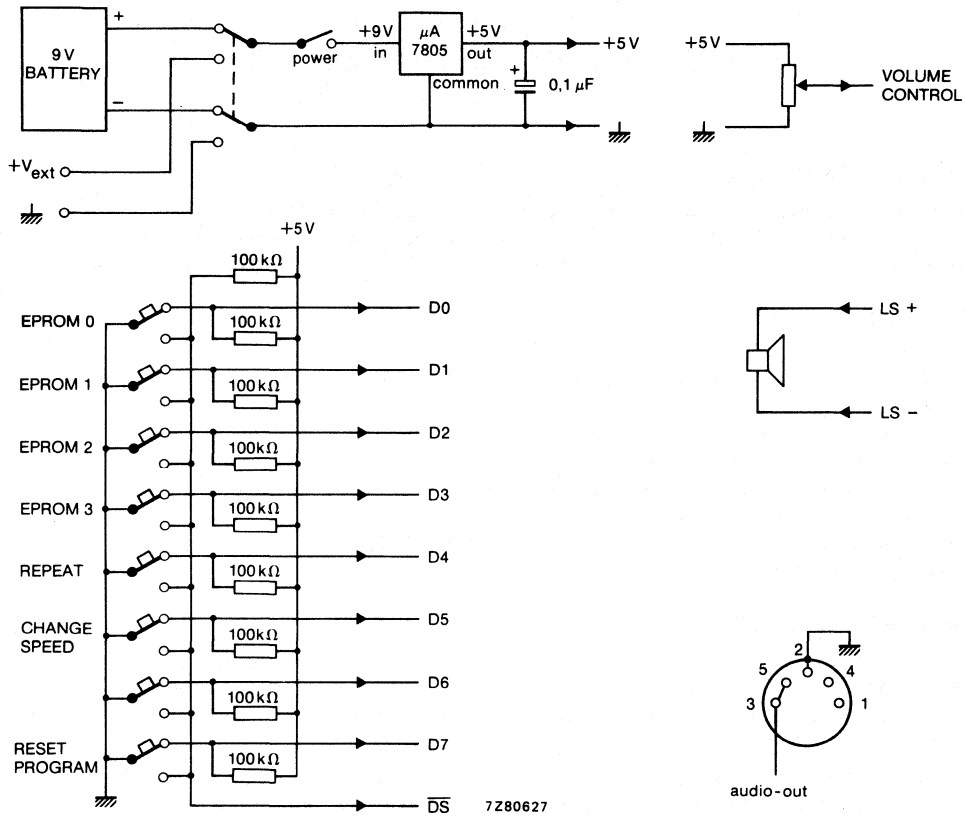


Fig. 1 Schematic diagram.

ORDERING INFORMATION

Product name: Speech Demonstration Box

Type number: OM8201

Ordering code: 9337 541 40000

N.B. OM8200 must be ordered as well if this box is to be used in demonstration mode. The order number for the OM8200 is 9337 541 30000.

Orders should be placed with your local Philips/Signetics agent.

SPEECH ANALYSIS/EDITING SYSTEM

GENERAL DESCRIPTION

The OM8210 is a speech analysing/editing system, and comprises of a speech adapter box and associated software. The system uses either the HP9816S or IBM-PC personal computer.
The OM8210 and the computer function together to produce speech coding for the PCF8200.
The system has many commands available, mostly single key operations, which gives it flexability.

FEATURES

- Input sampling of analogue speech signals
- Speech analysis
- Graphic parameter representation
- Parameter editing screen
- Conversion of parameters to PCF8200 synthesizer
- EPROM programming
- Parameter storage on floppy disc
- Speech output via PCF8200 voice synthesizer

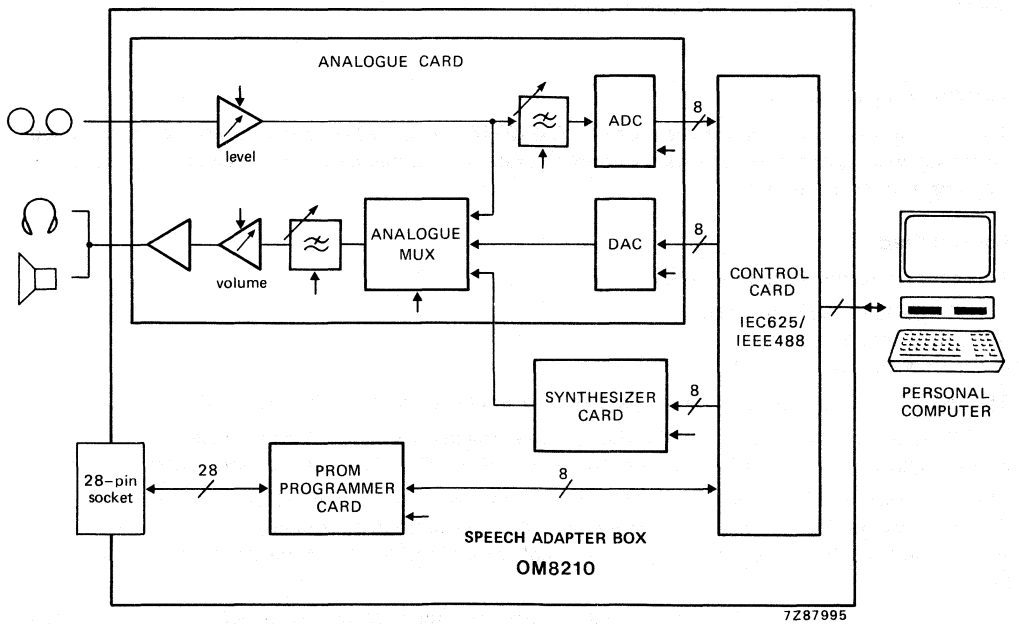


Fig. 1 Block diagram.

HARDWARE DESCRIPTION

The hardware for the OM8210 is contained in an attractive box with access to all the interconnections (IEC 625, interface loudspeaker, headphones, tape input, and EPROM socket), from the front panel. There are four single Eurocards and a power supply forming the speech adapter box.
These cards are:

- Analogue Card
- Synthesizer Card
- EPROM Card
- Control Card

Analogue Card

On this card, the level of the recorded audio input signal is adjusted by an electronic potentiometer. Before the audio is sampled, frequencies higher than half the sampling frequency are removed by a switched capacitor filter of the type normally used for codecs. A 12-bit analogue-to-digital converter (ADC) produces the digital samples that are sent to the control card. An 8-bit digital-to-analogue converter (DAC) on the analogue card allows the sampled speech to be output. The audio input signal, the sampled speech and the synthesized speech are selected by an analogue multiplexer, filtered, and adjusted for volume before reproduction by a loudspeaker.

The use of integrated electronic potentiometers and codec filters substantially reduces the number of components required while maintaining high performance.

Synthesizer Card

This card accommodates the PCF8200 voice synthesizer and a small amount of peripheral components and a socket for the MEA8000 voice synthesizer.

EPROM Programmer Card

This card allows four different types of EPROM (2716, 2732, 2732A and 2764) to be programmed under software control. All the hardware to generate the programming voltages and the programming waveforms are on this card.

Control Card

This card performs three functions:

- IEC 625/IEEE 488 interface
- Control sequencer
- Clock generator

The IEC/IEEE interface is a simple talker/listener implementation with a HEF4738 circuit.

An FPLA control sequencer provides the handshake signals for IEC/IEEE interface and the chip enable signals for the rest of the system (the ADC, the DAC, the synthesizer and control circuits).

The filter sampling frequency is generated with a software programmable PLL frequency synthesizer. The speech sampling frequency is derived from the filter sampling frequency by frequency division. Hence, the filter frequency cut-off and the sample rate of the ADC and the DAC are automatically linked.

The hardware includes all the necessary cables, adapter plug, loudspeaker, headphone and power supply.

SOFTWARE DESCRIPTION

The software for this speech coding system has been developed and arranged for optimum user convenience. There are eight modes available.

Each mode and each command in the mode is selected by single key entries. Commands that can destroy data have to be confirmed before they are executed. More than 100 commands are available. The modes are:

Sample Mode	Samples and digitizes the recorded speech, the amplitude can be checked and speech segments selected. The sampled speech is stored in a memory and can be displayed or made audible.
Analysis Mode	Generates speech parameters from samples. The analysis selects the voiced/unvoiced sections, extracts the formants (5 for male and 4 for female), amplitude, and the pitch, and quantisizes the speech parameters.
Parameter Edit Mode	Speech parameters are displayed graphically on the VDU and can be edited to correct errors in the analysis, improve speech quality by altering contours, or amplitudes, concatenate sounds and optimize data rate by editing the frame duration.
Code Mode	Generates PCF8200 code and permits the arrangement of utterences in the optimum order of application. This mode also generates the address map at the head of the EPROM.
EPROM Mode	Used to program/read EPROMS with data for the code memory also possible is a new check, bit check and verification commands.
File Mode	Stores speech parameters or codes on disc, can also assemble code speech segment from an already existing library.
Media Mode	For diskette initialization and making back-up copies.
Option Mode	Allows the system configuration to be read or changed.

The software is supplied on two diskettes, one labelled 'BOOT' which wakes up the system and also contains the system library routines. The other diskette labelled 'SPEECH' contains the speech program, the disc initialization and the file handler programs. The 'BOOT' disc is not required during operation, giving a free disc drive with the system for a diskette to store speech parameter files.

Computer System

The following equipment is required to make a complete Hewlett Packard based editing system:
- HP9816S-630 (optimum computer type) or HP9817
- HP9121D (dual floppy disc)
- Additional memory card for the HP9816S (512 K bytes total required)

The following equipment is required to make a complete IBM based editing system:
- IBM-PC or PC-XT or Philips P3100
- Additional memory (512 K recommended)
- Display graphics card (Hercules monochrome)
- IEEE488 card (Tecmar Rev. D.)

ORDERING INFORMATION

Product name:	Speech Analysis/Editing System
Type number:	OM8210
Ordering code:	9337 561 50112

The computer system should be purchased from your local agents.
The OM8210 should be ordered through your local Philips/Signetics agent.

PAGING DECODER

GENERAL DESCRIPTION

The PCA5000T is a fully integrated decoder for the CCIR Radio Paging Code number 1 (POCSAG-code). It supports two basic modes of operation:

Alert-Only-Pager. This is a stand-alone mode in which the PCA5000T scans inputs from three external switches that relate to the states ON, OFF and SILENT. Only a few external components are required to build an Alert-Only pager.

Display-Pager. In this mode, received calls and messages are transferred via the IC's serial communication interface to an external microcontroller. A built-in voltage converter can double the supply voltage output and perform level shifting on the interface signals.

Call-alert cadences are generated when valid calls and messages are received, and status cadences to indicate the present state of the decoder are generated following a status interrogation. An on-chip 5 x 9-bit static RAM with battery back-up is provided for programming two user-addresses and for special functions. Synchronization of the input data stream is achieved by the built-in ACCESS algorithm which allows data to be synchronized without preamble detection and minimizes battery power consumption by receiver-enable control. One of three error correction algorithms is applied to received code words to optimize the call success rate.

The PCA5000T is fabricated in SACMOS-technology to ensure low power consumption at low supply voltages. Typical applications are alert-only pagers, numeric/alphanumeric display pagers, cellular radio and data/telemetry decoders.

Features

- Wide operating supply voltage range (1.7 to 6.0 V)
- Very low supply current (15 μA typ.)
- Decodes CCIR Radio Paging Code number 1
- Data rate: 512 bits/s
- Powerful 'ACCESS' synchronisation algorithm
- Supports two user addresses
- Four cadences per user address
- Silent call storage, up to four different calls
- Interfaces directly to the UAA2033 digital paging receiver
- Directly drives a 2 kHz bleeper
- High-level alert facility requires only a single external transistor
- Receiver-enable control for battery economy
- On-chip static RAM, non-volatile with battery back-up
- On-chip voltage converter
- Level-shifted microcontroller interface
- Battery-low alert
- Out-of-range indication (optional)

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A.)

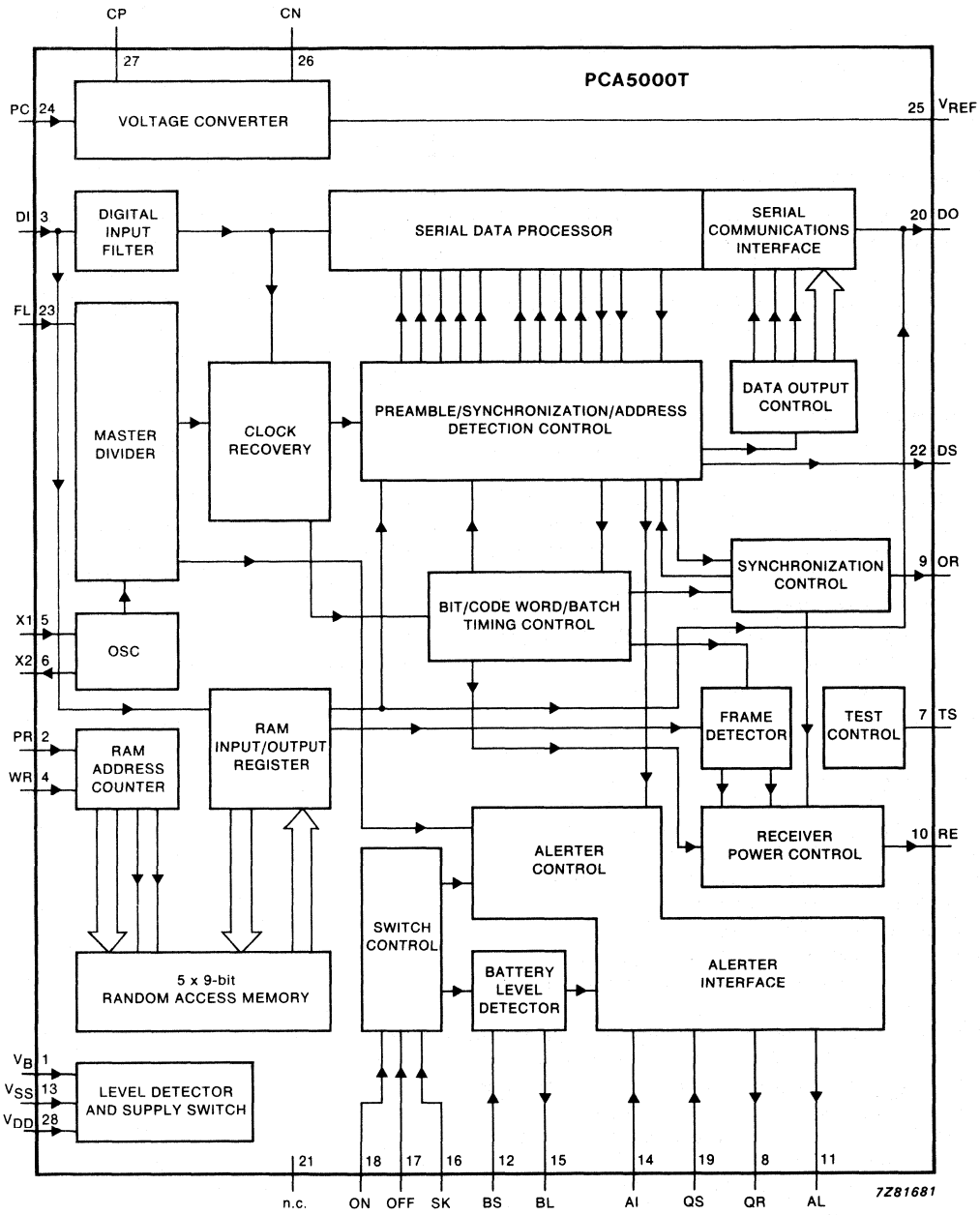


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

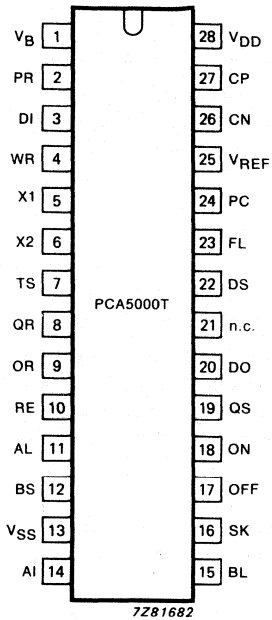


Fig. 2 Pinning diagram.

pin	mnemonic	description
1	V_B	RAM back-up negative supply voltage
2	PR	programming enable input
3	DI	serial data input
4	WR	programming WRITE input
5	X1	oscillator input
6	X2	oscillator output
7	TS	test mode enable input
8	QR	alert high-level output/vibrator output
9	OR	out-of-range output
10	RE	receiver enable output
11	AL	alert low-level output
12	BS	battery sense input
13	V_{SS}	negative supply voltage
14	AI	alarm input
15	BL	battery-low output
16	SK	silent key/mute input
17	OFF	off key/reset input
18	ON	on key/on-off input
19	QS	vibrator enable input
20	DO	received data output
21	n.c.	not connected
22	DS	received data strobe output
23	FL	frequency reference output
24	PC	power control input to voltage converter
25	V_{REF}	microcontroller interface negative reference voltage
26	CN	voltage converter external capacitor (negative)
27	CP	voltage converter external capacitor (positive)
28	V_{DD}	positive supply voltage (common)

FUNCTIONAL DESCRIPTION

Operating modes

The decoder has two basic operating modes; alert-only-pager and display-pager. There is also a programming mode in which the contents of the internal RAM are programmed or verified. The RAM holds two user-addresses and special function bits.

Alert-Only-Pager

No external microcontroller is required in this mode.

Tone-alert cadences are generated when valid calls are received. Four different alert cadences are available and are called by combinations of the special function bits. The voltage doubler is disabled in this mode.

The decoder continually scans the inputs ON, OFF and SK from the external switches ON, OFF and SILENT that determine the internal operating status. Operating one of the switches first causes the cadence of the existing internal status to be generated and then, 1.5 s after switch operation, generation of a cadence to indicate the new internal status of the decoder.

Display-Pager

In this mode the decoder receives calls/messages and directs those addressed to one of the two stored user addresses to an external microcontroller for post-processing and display. Tone-alert cadences are generated when valid calls are received.

The decoder provides a doubled supply voltage output to the microcontroller and associated hardware, and the interface signals are level-shifted to allow direct coupling to the microcontroller.

The internal state of the decoder is determined by the logic levels on the static inputs ON and SK.

Internal states

If the decoder is in one of the two operating modes, its internal status is always one of the following:

OFF state. This is the power-saving inactive state in which no decoding takes place and the paging receiver is disabled. Scanning of the ON, OFF and SK inputs is maintained to allow state-changes to be effected.

ON state. This is the normal active state of the decoder. Received calls and messages are compared with the two user addresses stored in the RAM. When the validity of incoming calls is confirmed, appropriate cadences are generated and data is shifted out via the serial microcontroller interface.

SILENT state. This is the same as the ON state except that alert cadences are not generated following valid calls. Instead, if programmed as an alert-only pager, the decoder stores up to four different calls. The appropriate alert cadences are generated after the decoder has been returned to the ON-state, the stored calls are then shifted out via the serial communication interface.

DEVELOPMENT DATA

POCSAG code structure

A transmission using the CCIR Radio Paging Code No. 1 (POCSAG code) is structured according to the following rules (see Fig. 3)

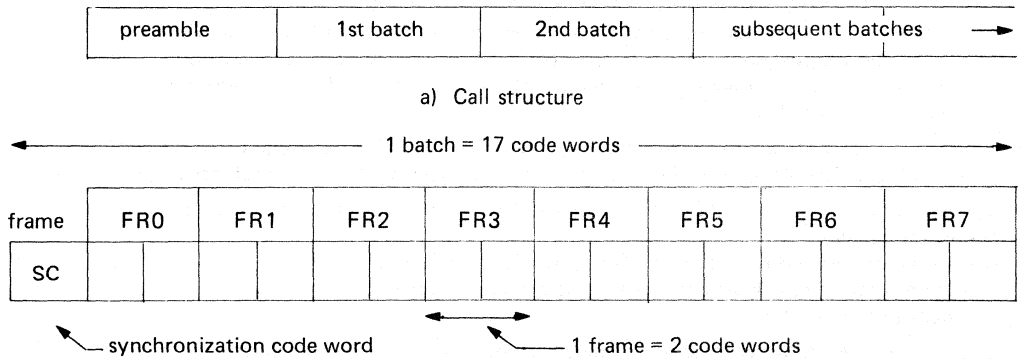
The transmission is started by sending a preamble which is a sequence of at least 576 continually alternating bits (01010101 . . .). The preamble precedes a number of batch blocks. The transmission is terminated after the last batch.

Every batch comprises a synchronisation code word with a fixed 32-bit pattern followed by eight frames (numbered 0 to 7). Only complete batches are transmitted.

A frame comprises two code words, each 32 bits long. A code word is either an address, message or an idle code word. Idle code words are transmitted to fill empty batches or to separate messages.

An address code word is coded as shown in Fig. 3; 18 bits of the 21-bit user address are coded in the code word and are protected against transmission errors by a CRC check word (bits 22 to 31). The other three bits of the user address are coded in the number of the frame in which the address code word is transmitted. Two function bits (bits 20 and 21) allow distinction between four different calls to one user address.

A message code word contains 20 bits of any information, these are also protected by a check word.



a) Call structure

b) Batch structure

bit	1	2 to 19	20	21	22 to 31	32
	0	user address	FC	FC	parity check	

c) Address code word structure (FC are function code bits)

bit	1	2 to 21	22 to 31	32
	1	message	parity check	

d) Message code word structure

Fig. 3 POCSAG coding structure.

FUNCTIONAL DESCRIPTION (continued)

Decoding

The POCSAG-coded input data is first noise-filtered by a digital filter. A sampling clock, synchronous to the 512 bits/s data rate, is derived from the filtered data.

Synchronization is performed on the POCSAG code structure using the ACCESS algorithm, which is a five-stage state mechanism.

The decoder first searches the data stream for preamble or synchronization code word patterns. Before synchronism can be achieved, the decoder must ascertain that synchronization code words are correctly positioned at the beginning of each batch. When the correct structure is detected, the decoder switches to the 'receive mode'. (The receiver enable output (RE) is active before input data is required.)

Error correction algorithms are applied to the data before the preamble and synchronization code word patterns are checked.

If synchronization is lost (i.e. no synchronization code word found at the beginning of the next batch) the decoder enters a two-step recovery mechanism. In the first step, over the next 15 batches, the decoder attempts to resynchronize by bit-wise shifting its frame window. A 'carrier off' state is entered in the second step, in this the data stream is tested convolutionally for a preamble or synchronization code word at every effective bit position within a continuous stream of at least 17 batches. When synchronization is regained, the decoder returns to the 'receive mode'.

In the 'receive mode', the input data stream is sampled at the frame position pointed to by the RAM program and the sampled code words are error-corrected. If they are address code words, they are compared with the two user addresses from the RAM. If the result of this comparison is 'true', the following actions take place:

- a store is set for a call-alert cadence. The cadence will relate to the combination of the special function bits in the accepted code word but will not be generated until the call has been terminated;
- the receiver enable output (RE) is held active so that reception of the call can continue. This condition remains until
  - another address code word or an IDLE instruction is received
  - the error-correction algorithm fails to generate a code word
  - synchronisation is lost;
- message code words attached to the validated address code word are transferred via the serial communication interface to the external microcontroller.

Programming

The on-chip RAM is organized in five 9-bit words (Fig. 4). It is used to store two user addresses (receiver identification codes) and six programmed special function bits. A lithium back-up battery maintains data retention when the main power supply is removed.

	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
word 0	A08	A07	A06	A05	A04	A03	A02	A01	A00
word 1	A17	A16	A15	A14	A13	A12	A11	A10	A09
word 2	B08	B07	B06	B05	B04	B03	B02	B01	B00
word 3	B17	B16	B15	B14	B13	B12	B11	B10	B09
word 4	FR2	FR1	FR0	SP6	SP5	SP4	SP3	SP2	SP1

where:

AXX are 18 bits of user address 'A'
BXX are 18 bits of user address 'B'
FR2 to FR0 are frame number bits common to both addresses 'A' and 'B'
SP6 to SP1 are special function bits.

Fig. 4 RAM organization.

A user address in POCSAG code comprises 21 bits, three of which are coded in the frame number. In the PCA5000T the frame number is common to both user addresses.

The special function bits are programmable to select from the following:

bit SP1: 0 alert-only-pager mode; silent override enabled on address 'B'
1 display-pager mode

SP2: 0 enable voltage converter (SP1 = 0)
1 disable voltage converter (SP1 = 1); cadence 1 (also for FC = 11)

SP3: 0 1-bit error-correction on message code words
1 4-bit burst error-correction on message code words on address 'B' (FC = 00 or 11)

SP4: free for user-application

SP5: 0 silent override enabled on address 'B' (FC = 01 or 10)
1 silent override enabled on address 'B' (FC = 00 or 11)

SP6: 0 silent override disabled on address 'A' (FC = 10)
1 silent override enabled on address 'A' (FC = 10)

The programming mode is entered by holding input PR at V_{DD} during power-on; exit from the programming mode is made by removing the main power supply. The back-up battery must remain connected to the PCA5000T to keep the RAM contents when the main power supply is removed. During programming, inputs ON, OFF and SK must not all be '1' at the same time.

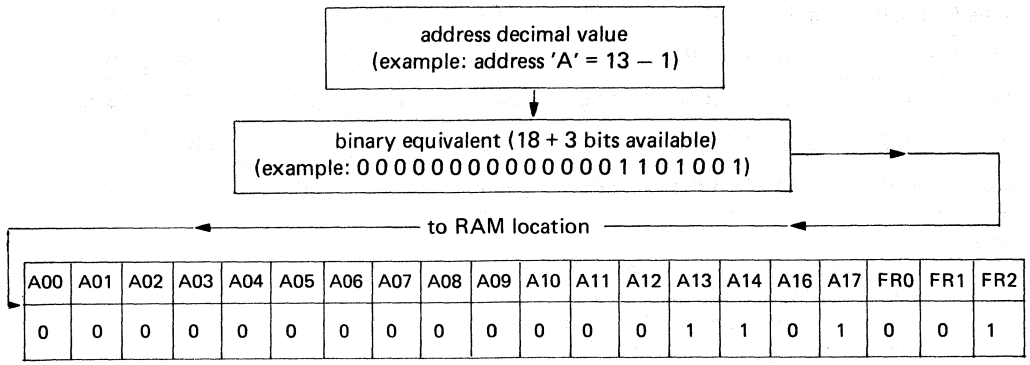
Programming of the RAM and verifying its contents is performed in a sequence starting with word 0, bit 0 and progressing through each of the five words in turn. Input and output is a serial operation; X1 is the shift clock input and DI, DO are respectively the data input and output.

During the RAM programming operation, a negative-going pulse first on WR and then on PR copies the 9 bits just shifted in into the RAM and switches to the next word (see Fig. 10).

During the RAM verify operation, reading the first word is triggered by a negative-going pulse on PR, which also switches to the next word in the sequence after 9 bits have been read (see Fig. 11).

Exit from the programming mode should be made after programming or verification of the RAM contents has been performed on all five words.

FUNCTIONAL DESCRIPTION (continued)



A00	A01	A02	A03	A04	A05	A06	A07	A08	A09	A10	A11	A12	A13	A14	A16	A17	FR0	FR1	FR2
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	1

Fig. 5 Example of bit conversion in user address programming.

Generation of output signals

Alerter interface

The alerter interface provides for the acoustic signalling of calls received (Fig. 8) and of changes of pager status (Fig. 9).

When valid calls are received and the pager is in the ON state, the decoder generates 2 kHz squarewave output signals to produce tone alert cadences via a magnetic or piezoceramic 2 kHz bleeper. The cadence signals differ in modulation according to the two function bits FC in the address code word (Fig. 6b). The PCA5000T supports two levels of alerter loudness: during the first four seconds, cadences are generated at low intensity (output AL active, output QR inactive); during the following twelve seconds, the intensity is increased (outputs AL and QR both active).

The alert tone generation is automatically terminated after sixteen seconds. Alert cadences are also terminated by an ON, OFF or SILENT input when in alert-only-pager mode, or by pulsing the status/reset input in display-pager mode.

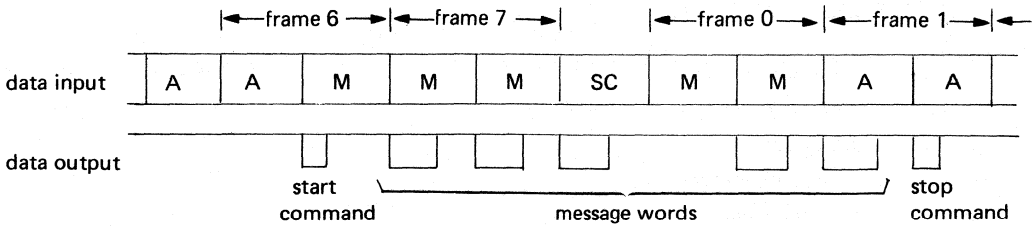
If the call is a message with subsequent message code words, alert cadence generation begins after the message has been terminated.

The alerter generates cadences to indicate the present internal status when interrogated and, when the main supply is low, gives a battery-low indicator output and generates an alarm tone.

Serial communication interface

This interface facilitates communication with an external microcontroller. Data is transmitted serially in the format shown in Fig. 6.

After receiving a valid address code word, transmission commences by sending a start command. The start command contains function data from the RAM, user address called (A or B) and function control bits FC from the address code word. The transmission continues with message words that contain the data from the received message code words. The end of a message transfer is marked by the sending of a stop command or another start command. In a stop command, bit 2 indicates that the call was successfully terminated.



a) Message format

bit

0	1	2	3	4	5	6	7
0	1	SP3	SP6	SP5	user address A or B	address bit 20 (FC)	address bit 21 (FC)

b) Start command format

bit

0	1	2	3	
1	1	1	1	message code word bits 2 to 21 as received

4 to 23

c) Message word format

bit

0	1	2	3	4	5	6	7
0	0	successful termination	$\overline{QS}$ input	SP4	SP2	not used	not used

d) Stop command format

Fig. 6 Serial communication interface.

DEVELOPMENT DATA

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
V_{DD} is referred to as 0 V (ground)

parameter	symbol	min.	max.	unit
Supply voltage	$V_{SS} = V_{13-28}$	+ 0.5	−7.0	V
RAM back-up supply voltage	V_B	V_{SS} + 0.8	−6.0	V
Input voltage on pins ON, OFF, SK, AI, PC, FL, BL, DS, DO	V_I	0.8	V_{REF}−0.8	V
Input voltage on any other pin	V_I	0.8	V_{SS}−0.8	V
Power dissipation per output	P_O	−	100	mW
Total power dissipation	P_{tot}	−	250	mW
Operating ambient temperature range	T_{amb}	−10	+ 60	°C
Storage temperature range	T_{stg}	−55	+ 125	°C

CHARACTERISTICS: Alert-Only-Pager (SP1 = 0)

V_{DD} = 0 V; V_{SS} = −2.7 V; V_{REF} = −2.7 V; V_B = −3.0 V; T_{amb} = 25 °C; quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 12) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	−2.7	−6.0	V
Operating supply current	all outputs open; all inputs at V_{SS}; voltage converter off	I_{SS}	−	−	−22.0	μA
Level at which RAM switches to V_B		$V_{SS(sw)}$	−1.2	−	−1.7	V
Supply current; peak value	AL = LOW	I_{SSM}	−	−	−45.0	mA
Input voltage LOW						
PR, DI, BS, QS, WR, TS		V_{IL}	0.7 V_{SS}	−	−	V
AI, ON, OFF, SK, PC		V_{IL}	0.7 V_{REF}	−	−	V
Input voltage HIGH						
PR, DI, BS, QS, WR, TS		V_{IH}	−	−	0.3 V_{SS}	V
AI, ON, OFF, SK, PC		V_{IH}	−	−	0.3 V_{REF}	V

CHARACTERISTICS: Alert-Only-Pager (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Input current						
PR, TS, BS	$V_I = V_{DD}$	I_I	7.0	–	18.0	μA
WR	$V_I = V_{SS}$	I_I	−9.0	–	−28.0	μA
DI	$V_I = V_{DD}$; $V_{RE} = V_{SS}$	I_I	85	–	260	μA
PR, TS, BS, DI, QS	$V_I = V_{SS}$	I_I	–	–	−0.1	μA
WR, QS	$V_I = V_{DD}$	I_I	–	–	0.1	μA
AI, ON, OFF, SK, PC	$V_I = V_{DD}$	I_I	6.0	–	16.0	μA
AI, ON, OFF, SK, PC	$V_I = V_{SS}$	I_I	–	–	−0.1	μA
Input capacitance						
BS, DI, PR, WR, QS, TS		C_I	–	–	5	pF
AI, ON, OFF, SK, PC		C_I	–	–	5	pF
X1		C_I	–	–	5	pF
Output current LOW						
RE, OR, QR	$V_{OL} = -1.35$ V	I_{OL}	−10.0	–	–	μA
DO, DS, BL, FL	$V_{OL} = -1.35$ V	I_{OL}	−10.0	–	–	μA
AL	$V_{OL} = -1.5$ V	I_{OL}	−17.5	–	−41.5	mA
Output current HIGH						
RE	$V_{OH} = -1.35$ V	I_{OH}	−10.0	–	–	μA
OR, QR	$V_{OH} = -1.35$ V	I_{OH}	−10.0	–	0.75	mA
DO, DS, BL, FL	$V_{OH} = -1.35$ V	I_{OH}	−10.0	–	–	μA
AL	AL = high impedance	I_{OH}	–	–	0.2	μA
Output capacitance						
X2		C_O	19	–	23	pF

DEVELOPMENT DATA

CHARACTERISTICS: Display-pager; alphanumeric mode (SP1 = 1, SP2 = 1)

CN and CP open circuit;
$V_{DD} = 0$ V; $V_{SS} = -3.0$ V; $V_{REF} = -6.0$ V; $T_{amb} = 25$ °C; quartz crystal f = 32.768 kHz, $R_{Smax} = 40$ kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	–	−3.0	V
Microcontroller interface negative reference		V_{REF}	V_{SS}	–	−6.0	V
Input current AI, ON, OFF, SK	$V_I = V_{REF}$ or V_{DD}	I_I	–	–	0.1	μA

CHARACTERISTICS: Display-pager; numeric mode (SP1 = 1, SP2 = 0)

220 nF capacitor connected to CN, CP;
V_{DD} = 0 V; V_{SS} = −3.0 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage range		V_{SS}	−1.7	–	−3.0	V
Voltage converter V_{REF} output: output voltage	V_{SS} = −3.0 V; no load	V_{REF}	−5.95	–	−6.0	V
	V_{SS} = −2.0 V; I_{VREF} = 150 μA; PC = 0	V_{REF}	−2.7	–	–	V
	V_{SS} = −2.0 V; I_{VREF} = 45 μA; PC = 1	V_{REF}	−2.7	–	–	V
output current	V_{SS} = −2.0 V; PC = 0	I_{VREF}	−150	–	–	μA
	V_{SS} = −2.0 V; PC = 1	I_{VREF}	−45	–	–	μA
Input current AI, ON, OFF, SK	V_I = V_{REF} or V_{DD}	I_I	–	–	0.1	μA

TIMING: Display-pager (SP1 = 1)

V_{DD} = 0 V; V_{SS} = −2.7 V; T_{amb} = 25 °C;
quartz crystal f = 32.768 kHz, R_{Smax} = 40 kΩ, C1 (Fig. 13) = 8 to 40 pF

parameter	conditions	symbol	min.	typ.	max.	unit
Oscillator frequency		f_{osc}	–	32.768	–	kHz
Alerter frequency		f_{alert}	–	2048	–	Hz
Data input rate		f_{DI}	–	512	–	bits/s
Frequency reference FL output		f_{FL}	–	16.384	–	kHz
Data input transition time		t_{TDI}	–	–	100	μs
Preamble duration			1125	–	–	ms
Batch duration		t_{BAT}	–	1062.5	–	ms
Bit period		t_{BIT}	–	1.9531	–	ms
Data output rate		f_{DO}	–	512	–	bit/s
Data output transition time		t_{DTO}	–	–	100	ns
Data strobe clock period		t_{DS}	–	1.9531	–	ms
Data output set-up time		t_{DOS}	–	1.77	–	ms
Data strobe pulse width		t_{DSW}	61	122	–	μs
Data hold time		t_{DH}	30.5	61	–	μs
Call alert period		t_{ALT}	–	16	–	s
Call alert (low level) AL output only		t_{ALL}	–	4.0	–	s
Call alert (high level) QR and AL outputs		t_{ALH}	–	12.0	–	s

parameter	conditions	symbol	min.	typ.	max.	unit
Call alert cycle period		t_{ALC}	–	1.0	–	s
Call alert pulse period		t_{ALP}	–	125	–	ms
Status pulse set-up time		t_{STP}	10.0	330	–	μs
Status pulse duration		t_{STD}	10.0	330	–	μs
Status alert period		t_{STON}	–	62.5	–	ms
Status alert delay		t_{STOF}	–	62.5	–	ms
Receiver control RE transition time	C1 = 5 pF	t_{RXT}	–	–	100	ns
RE establishment time		t_{RXON}	–	31.2	–	ms
Programming:						
data clock period		t_{PDC}	–	100	–	μs
data settling time		t_{PDS}	20.0	–	–	μs
write set-up time		t_{WSU}	20.0	–	–	μs
write pulse width		t_{WP}	10.0	–	–	μs
program input pulse width		t_{PR}	10.0	–	–	μs
program input settling time		t_{PRS}	–	–	20.0	μs
Power-on reset pulse width		t_{POR}	7.5	–	–	μs
Program start delay time		t_{CSU}	20.0	–	–	μs
Data hold time		t_{PDE}	10.0	–	–	μs
Data clock period LOW		t_{X1}	10.0	50.0	–	μs

DEVELOPMENT DATA

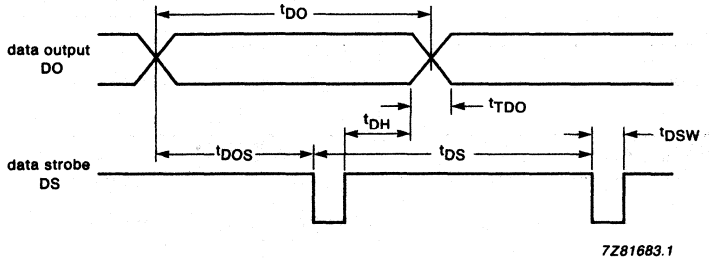


Fig. 7 Serial communications interface timing.

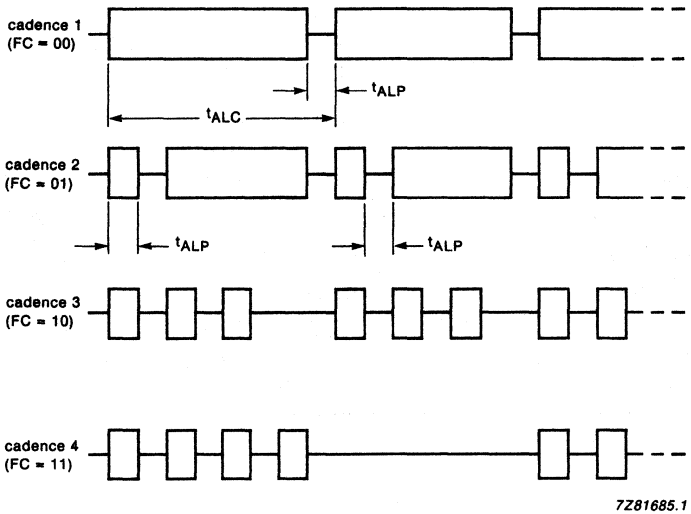


Fig. 8 Call alert cadences; FC refers to function control bits 20 and 21 in the address code word.

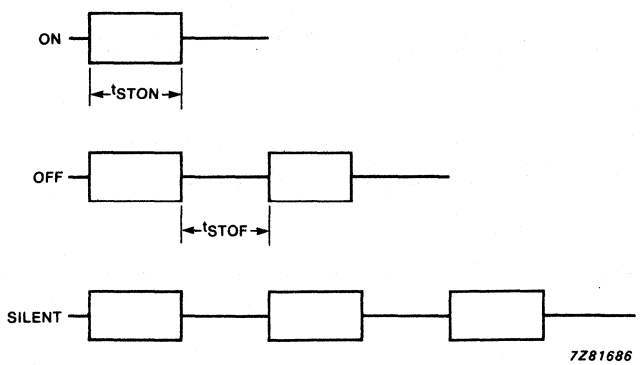


Fig. 9 Status indication cadences.

DEVELOPMENT DATA

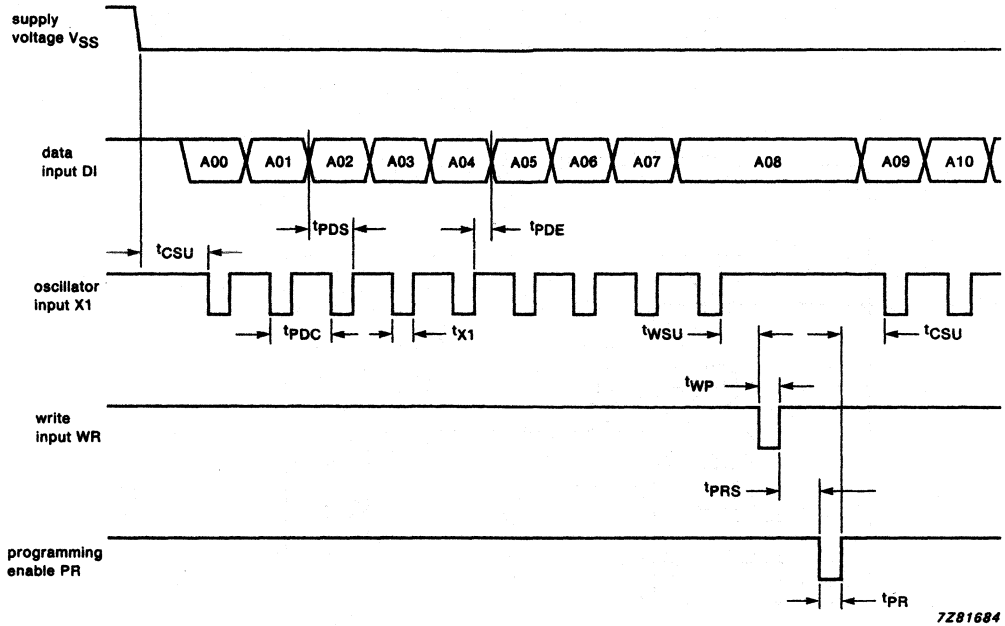


Fig. 10 Timing of RAM programming operation.

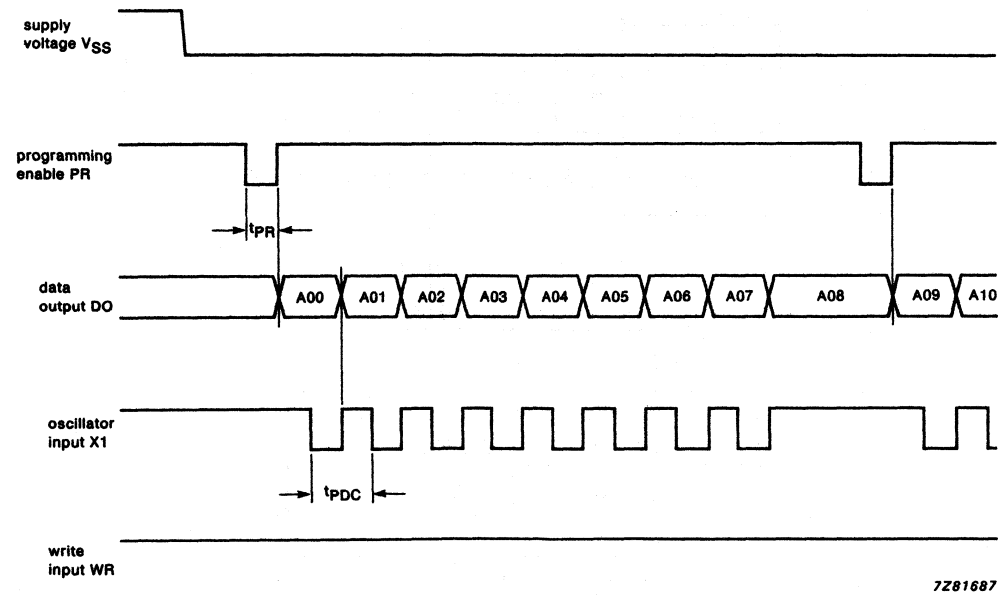


Fig. 11 Timing of RAM verify operation.

APPLICATION INFORMATION

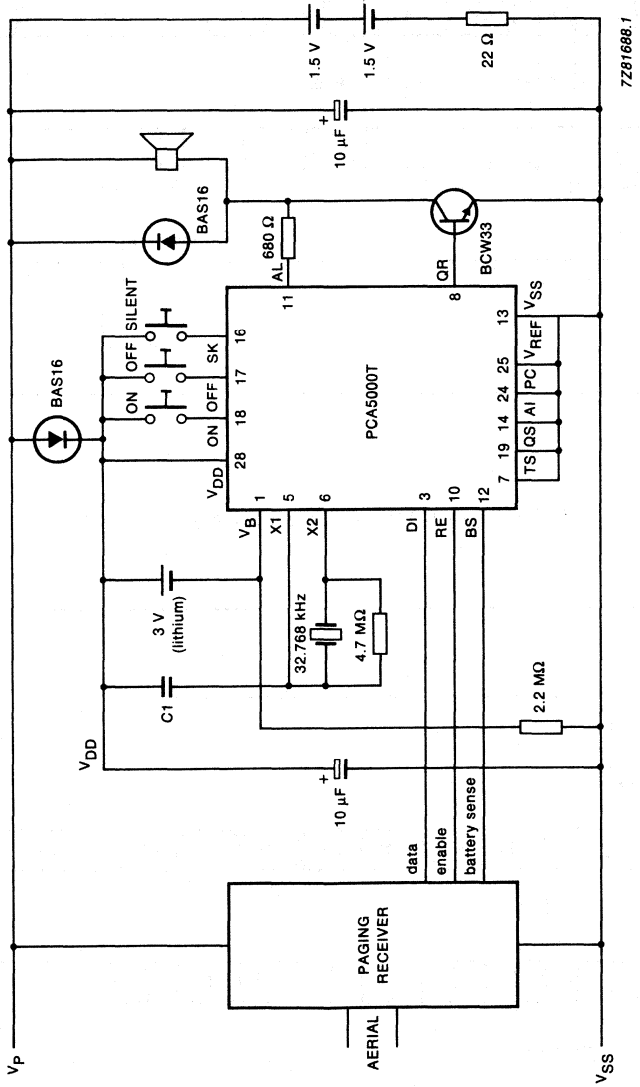


Fig. 12 Example of alert-only pager.

DEVELOPMENT DATA

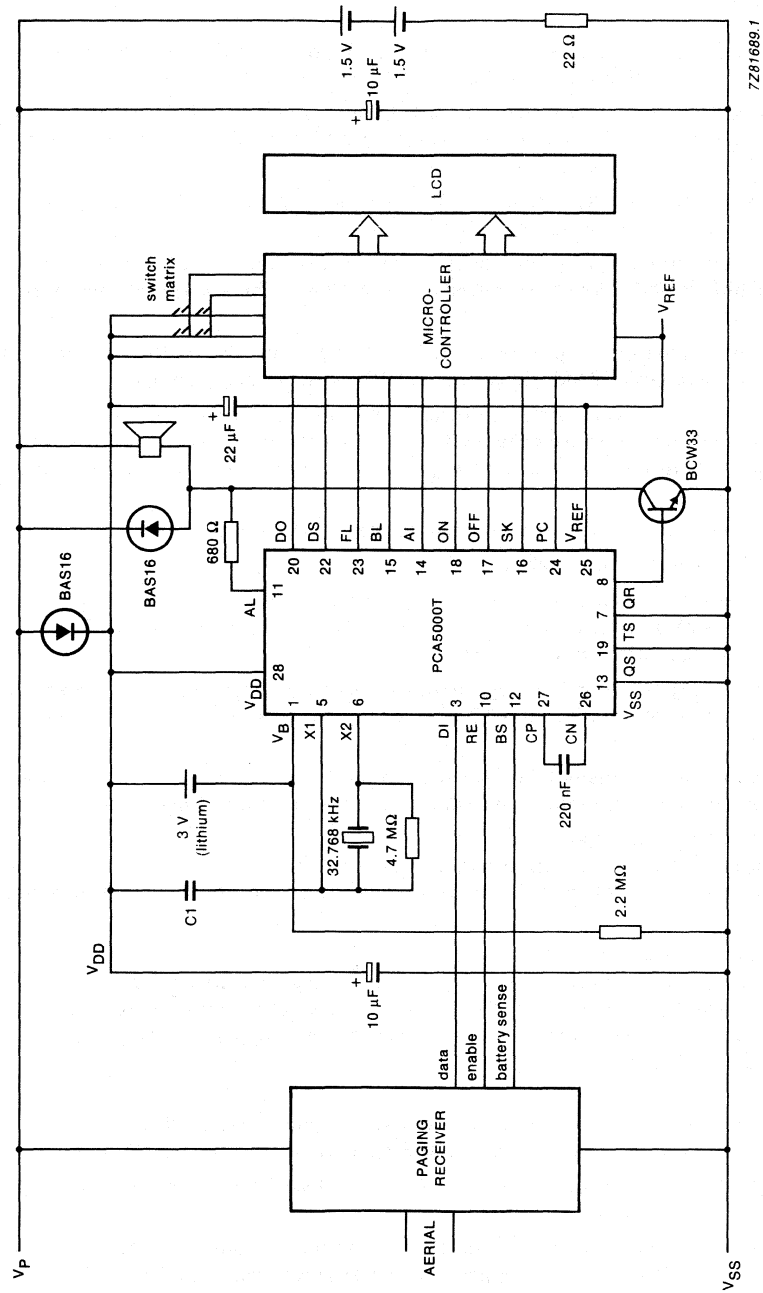


Fig. 13 Example of display-pager in alphanumeric mode with voltage converter enabled.

Application notes

Input pins

The programming control inputs have internal biasing resistors of sufficiently low impedance to provide safe operation even if the pins are left open circuit.

Pin 1 (V_B): RAM back-up battery negative supply. Connect this pin to the negative terminal of a lithium battery and connect the positive battery terminal to V_{DD}. This battery supply ensures data retention when the main supply voltage is removed.

Pin 2 (PR): programming enable, normally LOW. To enter the programming mode, pull this input HIGH when connecting the main supply voltage.

Pin 3 (DI): serial data input. During normal operation, POCSAG-coded data is received via this pin. When in programming mode, data to be stored in the internal RAM is read from this input whenever a pulse on X1 occurs.

Pin 4 (WR): programming write input, normally HIGH. A positive edge on this pin copies the preceding word shifted into the internal RAM. Keep this pin HIGH during RAM-read operations.

Pin 5 (X1): oscillator input. Connect a 32 kHz crystal to this pin during normal operation. When in programming write mode, a positive edge on X1 shifts the data present on DI to the internal register. When in programming read mode, a positive edge on X1 moves the next bit from the internal register to DO.

Pin 6 (X2): oscillator output. Return connection to the 32 kHz crystal.

Pin 7 (TS): test mode enable input, **always** LOW.

Pin 12 (BS): battery sense input. The decoder samples this input when it is in the ON state and the receiver is enabled. Every single sample is copied to the BL output. A continuous high-level alert tone is generated if four sequential samples are HIGH.

Pin 13 (V_{SS}): main negative supply voltage. Remove the voltage from this pin to leave the programming mode. The RC combination of 22 Ω and 10 μF (Figs 12 and 13) should remain connected; disconnect the battery only.

Pin 14 (AI): alarm input, normally LOW. A HIGH on this input causes a continuous high-level alert tone to be generated. The input may be pulsed to modulate the output tone.

Pin 16 (SK): silent key/mute input.
Alert-Only-Pager: push-button switch input, pushing the switch selects SILENT state.
Display-Pager: static input, when HIGH no calls are stored and no alert tones are generated for calls received.

Pin 17 (OFF): off key/reset input.
Alert-Only-Pager: push-button switch input, pushing the switch selects OFF state.
Display-Pager: static input, normally LOW. A positive-going pulse on this input causes (a) status indication cadences to be generated if the decoder is not generating or resetting an alert call or (b) a battery-low alert if BS is active.

Pin 18 (ON): on key/on-off input.
Alert-Only-Pager: push-button switch input. Pushing the switch selects ON state.
Display-pager: static input. LOW level selects OFF state, HIGH level selects ON state.

Pin 19 (QS): vibrator enable input, normally LOW. A HIGH level enables the vibrator output logic and switches QR to vibrator output.

Pin 24 (PC): voltage converter power control. The level on this pin determines the output impedance of the voltage converter. LOW selects low impedance, HIGH selects high impedance.

Pin 26 (CN): voltage converter external capacitor, negative connection.

Input pins (continued)

Pin 27 (CP): voltage converter external capacitor, positive connection.

Pin 28 (V_{DD}): main positive supply input. This pin is common to all supply voltages and is referred to as GROUND.

Output pins

Pin 8 (QR): alert high-level output/vibrator output. This output can directly drive an external bipolar transistor to control a vibrator-type alerter if QS is set HIGH, or supports high-level alerting in conjunction with AL.

Pin 9 (OR): out-of-range output, active HIGH. If the decoder detects 'carrier-off', an output is generated for the duration of the synchronization scan period. Connecting OR to QR provides alert tone generation during 'carrier-off'.

Pin 10 (RE): receiver enable output, active HIGH. Connect the radio paging receiver power control input to this pin to minimize power consumption. Whenever no input data is required, the PCA5000T will disable the paging receiver to conserve power.

Pin 11 (AL): alert low-level output, active LOW. The low-level alert tone is generated via this output; the alert becomes high-level in conjunction with QR.

Pin 15 (BL): battery-low output, active HIGH. Every time the PCA5000T samples the BS input, data sensed is output on this pin.

Pin 20 (DO): received data output. During normal operation, accepted calls and possibly subsequent message code words are output via this pin at a rate of 512 bits/s. When in programming read mode, data read from the internal RAM is presented bit-by-bit on this pin.

Pin 22 (DS): received data strobe output, active LOW. In normal operation, every time this output goes LOW, the next bit on the DO output is valid.

Pin 23 (FL): frequency reference output. If the decoder is programmed as a Display-Pager, a 16 kHz squarewave reference is output from this pin.

Pin 25 (V_{REF}): microcontroller interface negative reference voltage. The LOW level of pins FL, BL, DO, DS, AI, ON, OFF, SK and PC is related to the voltage on V_{REF}.

Alert-Only-Pager: Connect V_{REF} output to V_{SS}.

Display-Pager: The doubled negative supply voltage generated by the internal voltage converter is output from V_{REF}. The V_{REF} pin may also be driven from an external supply if the capacitor across CN/CP is removed and CN/CP are left open circuit.

IST BUS INTERFACE (IBI)

HOW TO USE THIS DATA SHEET

- **Section 1** introduces the IST bus interface. The functional areas of the circuit are shown with a block diagram and all input and output signals are described. The physical locations of the signals are indicated in a pinning diagram. Ordering information is found in this section.

- **Section 2** describes the functioning of the IST bus interface and follows the functional areas established by the block diagram in section 1. This section also describes how the functional areas are controlled by programmed instructions.

- **Section 3** provides the electrical characteristics. This section is used when designing system hardware.

- **Section 4** provides application information.

- **Section 5** gives details of the PCB2310 packaging.

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1.2 Ordering information
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1.0 INTRODUCTION

The PCB2310 is a CMOS integrated VLSI circuit offering a full layer 1 and 2 interface for the IST bus. It operates as the interface between the IST bus at one side and at the other side it interfaces to intra terminal interfaces such as Terminal Highway (THW), Subscriber Line Data (SLD) bus and an 8-bit microcontroller with multiplexed address/data I/O lines.

The PCB2310 is one of a set of circuits required to complete the modular terminal architecture for Integrated Services Digital Network (ISDN) terminals. For contemporary analogue telephone functions the PCB2310 in conjunction with the PCB2060 (signal processing codec filter) requires only a microcontroller, a power supply, a transformer and some discrete components.

The IBI is an interface between different buses namely:

- The IST bus is a Local Area Network (LAN) with a maximum length of at least 300 metres (see IST bus specification). It offers a low-cost local communication medium for voice and data communications and is compatible with the ISDN according to CCITT-I series of recommendations. The IST bus can also be used with current analogue and digital networks.
- The SLD bus is a standardized 8 kHz syndrome communication bus for on-board routing of B, S and C channels. The C (control) and S (signalling) channels of the SLD bus are accessed via the microcontroller I/O port.
- The 8-bit microcontroller is an MAB8051 compatible microcontroller bus. The data and address lines are multiplexed.
- The THW is a PCM highway with a transmission rate of 2048 Mbit/s.

The eight 64 kbit/s circuit-switched IST bus channels are mapped on time slots on the THW which can be switched to the two B channels of the SLD bus. The 64 kbit/s packet-switched channel is routed to the 8-bit microcontroller parallel I/O port. The PCB2310 offers layer 1 and 2 services of the 7-layer hierarchy of the Open Systems Interconnection (OSI) model developed by the International Standardization Organization (ISO) in this packet-switched channel of the IST bus.

Table 2.6-6 gives a quick reference to the PCB2310.

1.1 Features

- Designed to interface with a twisted-pair cable via a coupling transformer for galvanic isolation and/or d.c. supply
- On-chip 8192 kHz clock generator
- 8 kHz synchronous frame
- External 8 kHz synchronization input for gateways
- Alternative Mark Inversion (AMI) line code
- Receiver input phase locked to the IST bus channels
- Automatic frame word transmitter allocation
- Eight 64 kbit/s half duplex circuit-switched channels which are fixed mapped on time slots of the Terminal Highway (THW)
- Three-wire 2 Mbit/s 32-channel Terminal Highway (THW):
  THDA: Terminal Highway data I/O 3-state pin
  THCL: Terminal Highway clock 2048 kHz clock input/output
  THSC: Terminal Highway synchronization 8 kHz input/output
- 4096 kHz and 8192 kHz clock output
- Three-wire SLD bus:
  SIP : SLD data I/O 3-state pin
  SCLK : SLD clock input/output pin
  ESC/SDIR: 8 kHz synchronization input/output
- On-chip B channel switches and interface for SLD bus
- Time slot assignment control for the two B channels
- Distributed collision-free circuit-switched channel access mechanism, no central controller required
- Circuit-switched channel transfer facility for register recall services on duplex links
- One half duplex 64 kbit/s packet-switched common signalling and data channel (bd) with the following features:
  full layer 1 and 2 interface (OSI)
  single frame protocol
  immediate packet acknowledgement
  100% guaranteed channel access based on CSMA/CD (Carrier Sense Multiple Access/with Collision Detection)
  layer 2 service offers error-free packet transmission; transmission errors are recovered by re-transmissions
  error detection based on Frame Check Sequence (FCS) using Cyclic Redundancy Check (CRC) divider. The divider is:

$$X^{16} + X^{12} + X^5 + 1$$

  and the initial remainder is '00'
  separate program-sized transmit and receive buffers for signalling (s) packets and data (d) packets
  signalling packets have transmission priority over data packets
- 8-bit microcontroller I/O port including a 16-byte FIFO
- Access to S and C channels of SLD bus via 8-bit I/O port
- On-chip power-on reset circuit
- Monitor mode for bd channel
- Separate + 5 V supplies for analogue and digital parts

1.2 Ordering information

TYPE NUMBER	TEMPERATURE RANGE °C	PACKAGE
PCB2310WP	0 to +70	44-pin PLCC

DEVELOPMENT DATA

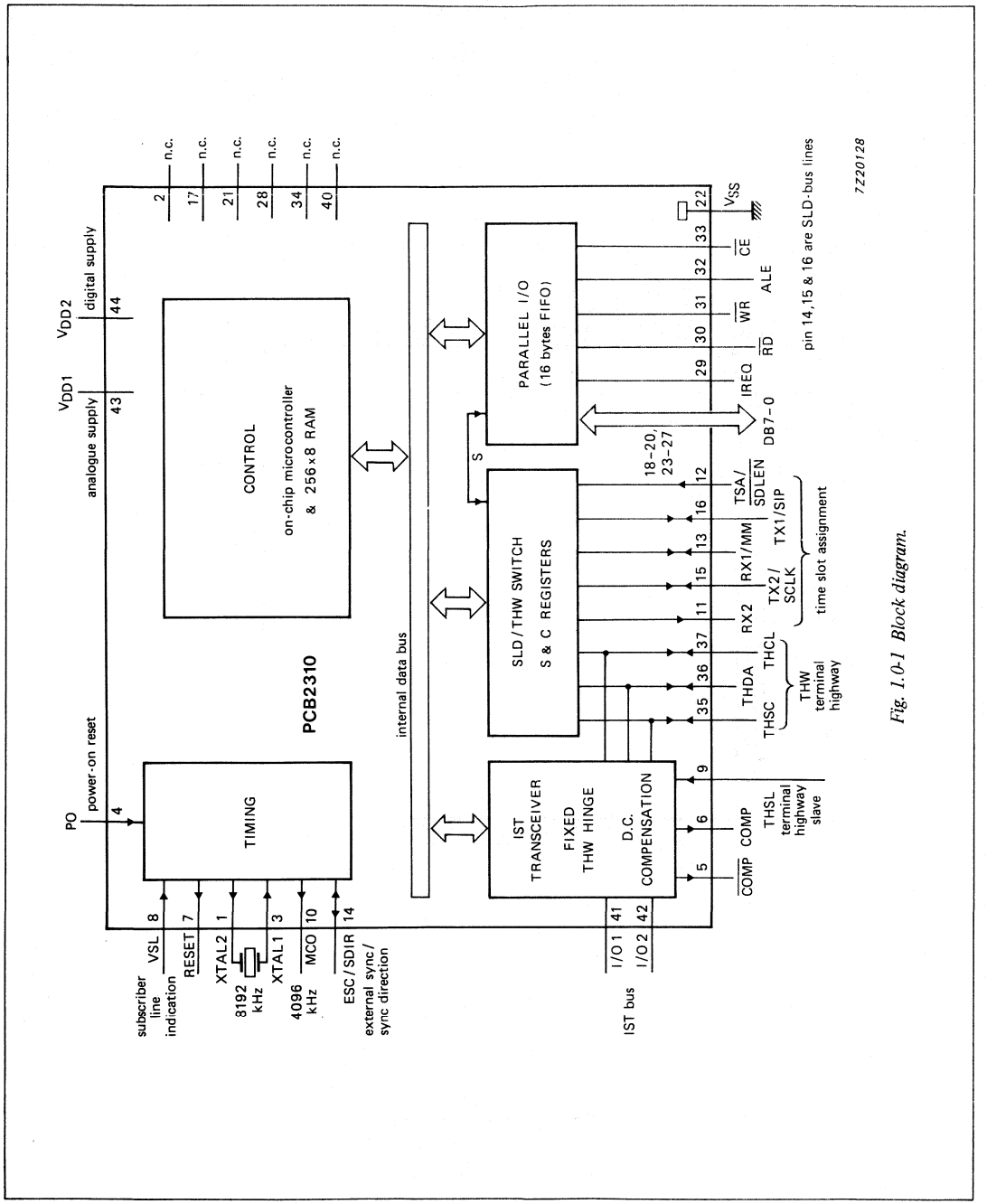


Fig. 1.0-1 Block diagram.

1.3 Signal description

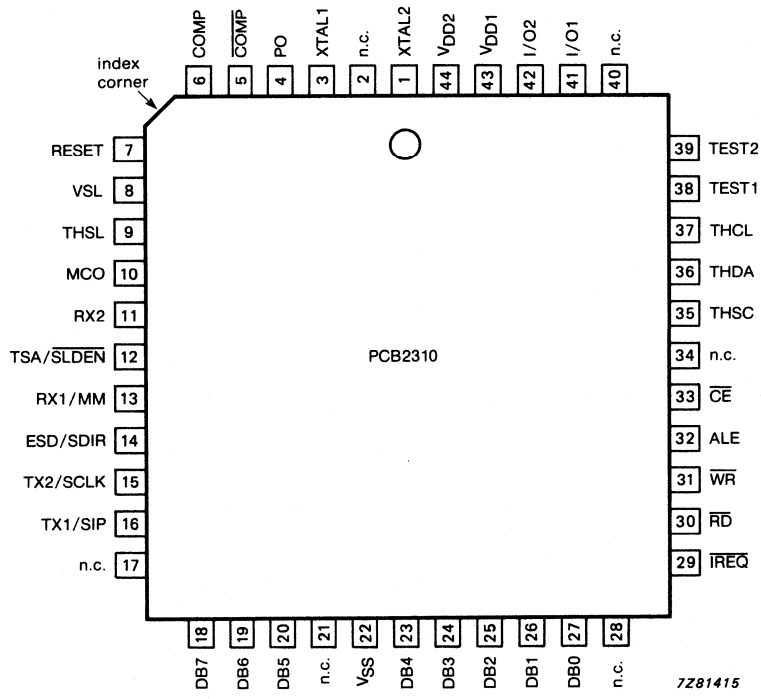


Fig. 1.3-1 Pinning diagram.

DEVELOPMENT DATA

General

All inputs, outputs and input/outputs are TTL compatible. Unless otherwise specified all outputs can drive 2 TTL (= 8 LSTTL) inputs and equivalent CMOS inputs.

1 XTAL2 Inverting buffer output; part of clock generator circuit. One side of the crystal is connected to pin 1. This pin could drive other circuits provided the capacitive load is less than 15 pF. When using an external clock generator pin 1 is not connected.

2 n.c. not connected.

3 XTAL1 Inverting buffer input. The other side of the crystal is connected to pin 3. An 8192 kHz ± 100 ppm crystal must be used. An external clock generator can also be connected to this pin.

4 PO Power On/reset active LOW* input. If there is a LOW pulse of $> 1\ \mu s$, while the clock is running, the PCB2310 will be reset. If pin 4 is HIGH it will be automatically reset by an internal circuit provided the voltage on V_{DD1} (pin 43) is $< 1{,}2$ V and rising to 5 V with a slope > 5 V/ms.

5 $\overline{\text{COMP}}$ Compensation active LOW output.
6 COMP Compensation active HIGH output.
These two outputs are used to compensate the change in inductive current in the transformer (Fig. 4.0-3).

7 RESET Active HIGH output. When pin 7 is HIGH the PCB2310 can only be used to perform an internal reset. Pin 7 could also reset the microcontroller. After power up this pin will be HIGH for 1 ms.

8 VSL Subscriber line connection input.
VSL = HIGH indicates that the PCB2310 is part of a gateway to other network(s) such as ISDN 'S reference point'.

9 THSL Terminal highway slave mode selection input.
THSL = LOW puts the Terminal Highway (THW) interface to the normal master mode.
THSL = HIGH switches the PCB2310 to the slave mode on the Terminal Highway. In this mode THCL (pin 37) and THSC (pin 35) are external inputs.

10 MCO Master clock output (4096 kHz). This output can be used as a clock output to drive peripheral circuits. The output is the crystal frequency divided by 2 with a duty cycle of 50%.

11 RX2 THW time slot assignment output.
RX2 = HIGH during time slot on the THW that is set by the command <SBS> (see section 2.7.5).

12 TSA/ $\overline{\text{SLDEN}}$ Input signal to select between time slot assignment and SLD bus signals. If TSA = LOW pins SIP (pin 16), SCLK (pin 15) and MM (pin 13) are in the SLD mode. If TSA = HIGH these pins are switched to Time Slot Assignment mode.

13 RX1/MM THW time slot assignment output/Master Mode selection input. If TSA = HIGH, this pin is an output, and the signal is HIGH during the time slot on the THW that is set by the command <SBS>.

If in the SLD mode (TSA = LOW) this is an input pin and selects between the master mode or the slave mode on the SLD bus:
MM = HIGH = Master mode;
MM = LOW = Slave mode.

14 ESC/ SDIR External synchronization/Frame synchronization input/output. If in the master mode on the SLD bus (MM = HIGH and TSA = LOW) this pin is an output for the 8 kHz synchronization signal of the SLD bus. If in the slave mode or in the TSA mode (MM = LOW or TSA = HIGH) this pin is an input and the PCB2310 synchronizes on to the 8 kHz ESC signal if VSL = HIGH and the PCB2310 is master on the IST bus.

15 TX2/ SCLK THW time slot assignment output or SLD clock input/output. If TSA = HIGH this pin is an output, and the signal is HIGH during the time slot on the THW that is set by the command <SBS>.

If master on the SLD bus (TSA = HIGH; MM = HIGH) SCLK provides the 512 kHz clock signal, if slave (TSA = HIGH; MM = LOW) the 512 kHz clock is input to this pin.

* LOW means voltage on pin 4 is equal to V_{SS} (pin 22).
HIGH means voltage on pin 4 is equal to V_{DD2} (pin 44).

1.3 Signal description (continued)

16	TX1/ SIP	THW time slot assignment output/SLD data I/O** pin. If TSA = HIGH this pin is an output, and the signal is HIGH during the time slot on the THW that is set by the command <SBS>. If slave on the SLD bus (TSA = HIGH; MM = LOW) data can be transmitted in the B_1 and B_2 channels when ESC (pin 13) is LOW and in the other channels when the output is 3-state. Both B_1 and/or B_2 channels can be programmed to output a high impedance. If master on the SLD bus (TSA = HIGH; MM = HIGH) the B_1, B_2, S and C channels are transmitted when ESC is HIGH. Data is put on the SIP output at a positive transition of SCLK. The idle code in the B_1, B_2 and C channels is all logic 1's and in the S channel the initial code is all logic 0's.
17	n.c.	not connected.
18-20 23-27	DB7-0	Combined address input and data I/O port. These pins are used to access internal registers P80 to P83. The selection between address and data is made by ALE (pin 32). $\overline{WR}$ (pin 31) and $\overline{RD}$ (pin 30) will select input or output respectively.
21	n.c.	not connected.
22	V_{SS}	Ground.
28	n.c.	not connected.
29	$\overline{IREQ}$	Interrupt request is an open drain output. This signal is active LOW. If a bit is set in the interrupt register PO, pin 4 is made LOW. If the interrupt is serviced by reading register PO the interrupt will be reset.
30	$\overline{RD}$	Read active LOW input. If this input is LOW data will be put on the DB7-0 I/O port from the addressed register.
31	$\overline{WR}$	Write active LOW input. If this input is LOW data on the BD7-0 I/O port will be written into the addressed register.
32	ALE	Address latch enable input. A HIGH on this pin latches the data on the DB7-0 I/O port into the address latch provided $\overline{CE}$ (pin 33) is LOW.
33	$\overline{CE}$	Chip enable active LOW input.
34	n.c.	not connected.
35	THSC	Terminal highway synchronization input/output. When THW interface is in master mode (THSL = LOW) pin 35 is a 2048 kHz output pulse with a repetition frequency of 8 kHz. When THW interface is in slave mode (THSL = HIGH) pin 35 becomes an input.
36	THDA	Terminal highway data input/output/3-state pin. Data is put on this line on a positive transition of THCL (pin 37).
37	THCL	Terminal highway clock input/output pin. This output can drive 4 TTL (= 16 LSTTL) inputs. When THW interface is in master mode this pin is the output for a 2048 kHz clock. When THW interface is in slave mode this pin is the input for a 2048 kHz clock.
38 39	TEST1 TEST2	These pins are for production test and both must be LOW for normal operation.
40	n.c.	not connected.
41	I/O1	IST bus I/O pin**. Special I/O to drive the IST bus. The connection to the IST bus is via a transformer. Pin 41 can be directly connected to one side of this transformer (see section 2.3 and IST bus specification).
42	I/O2	IST bus reference pin. This pin outputs a voltage of $V_{DD}/2$. The other side of the transformer should be connected to this pin.
43	V_{DD1}	Supply voltage for the analogue parts of the PCB2310. $V_{DD1} - V_{SS} = 5\ V \pm 5\%$.
44	V_{DD2}	Supply voltage for the digital parts of the PCB2310. $V_{DD2} - V_{SS} = 5\ V \pm 5\%$.

** I/O indicates a 3-state pin; HIGH, LOW or high impedance.

2.0 FUNCTIONAL DESCRIPTION

2.1 General description

The PCB2310 performs the electrical interface and the protocols on the IST bus as described in the IST bus specification. A brief description of the IST bus is given in section 2.2.

The circuit-switched channels on the IST bus (b1 to b8) are mapped on specific Terminal Highway (THW) time slots and can be routed to SLD B_1 and B_2 channels and vice versa.

$$\text{IST b1 to b8} \xleftrightarrow[\text{MAPPING}]{\text{FIXED}} \text{THW} \xleftrightarrow[\text{ALLOCATION}]{\text{CONTROLLABLE}} \text{SLD}(B_1, B_2)$$

The packet-switched bd channel on the IST bus is routed through layer 1 and layer 2 entity. The service access point on the layer 2 service is performed by the microcontroller I/O port.

The microcontroller I/O port performs the interface for the control stages of the PCB2310 and is also the access point for the C and S channels on the SLD bus.

An on-chip reset circuit and clock generator minimizes the number of external components.

2.2 IST bus description

The PCB2310 is fully developed to operate according to the IST bus specification. The PCB2310 can be connected direct to the IST bus via a transformer.

The 8 kHz (125 μs) synchronous IST bus frame contains ten time division multiplexed channels as shown in Fig. 2.2-1:

- 1 x 5-bit synchronization channel; Frame (F)
- 1 x 64 kbit/s packet-switched channel; Data (bd)
- 8 x 64 kbit/s circuit-switched channels; Data/voice (b1 to b8)

Each channel is preceded with an 'occupied' bit which is logic 1 if the channel is occupied.

2.2.1 bd channel

The PCB2310 interfaces the bd channel with the 8-bit microcontroller I/O port, for which it performs a full layer 1 and 2 service as defined in the IST bus specification. It performs all the requirements for error detection and correction by re-transmissions and flow control on the packets transmitted in the bd channel. Layer 2 packets for re-transmission can be stored in the 256 x 8 internal RAM.

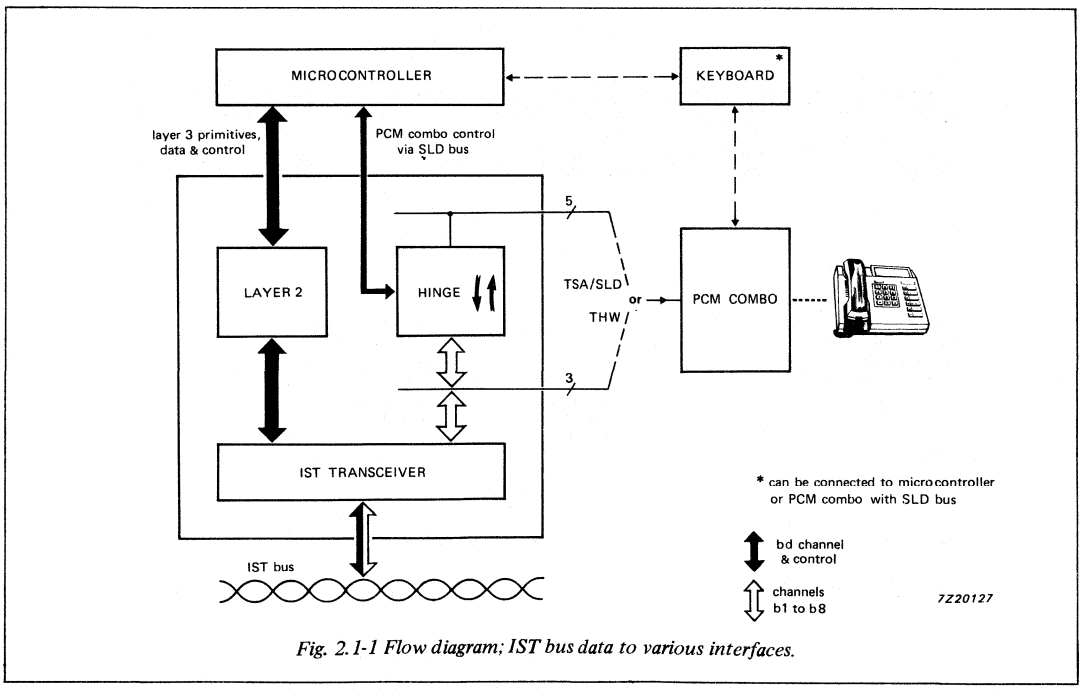


Fig. 2.1-1 Flow diagram; IST bus data to various interfaces.

2.2.2 b channels

The PCB2310 also handles the circuit-switched channel connections; the access mechanism being completely distributed. There is no network manager. Command <FFC> (see Table 2.6-6) orders the PCB2310 to access a free b1 to b8 circuit-switched channel. A b1 to b8 channel is fetched by transmitting an 'occupied' bit (see Fig. 2.2-1) and the data on the corresponding THW time slot will be mapped upon this IST bus b1 to b8 channel. With command <OAR> the ordered channel will be occupied as soon as it is released.

A channel is seen **free** if the 'occupied' bit of that channel is logic 0 for at least **two consecutive frames.**
A channel is seen **released** if the 'occupied' bit is logic 0 for at least **one frame.**

2.2.3 Frame channel

The PCB2310 can operate on the IST bus in two modes; master or slave. In the PCB2310 the complete distributed master/slave arbitration protocol is implemented (see IST bus specification). All IST slaves will synchronize on the frame channel as transmitted by the IST master. If VSL (pin 8) is HIGH and the PCB2310 is master on the IST bus, the PCB2310 will synchronize on the 8 kHz external input signal at ESC/SDIR (pin 14).

The PCB2310 also performs some maintenance functions such as IST BUS_DOWN and IST BUS_UP.

2.3 IST bus I/O stage

The IST bus I/O stage consists of a receiver and a transmitter. The line code is Alternative Mark Inversion (AMI).
The bit rate is 1024 kbit/s based on an 8,192 kHz crystal. I/O1 (pin 41) drives the IST bus while I/O2 (pin 42) is held at $V_{DD}/2 \pm 60$ mV. The nominal output voltage on I/O1 when driven is ($V_{DD1} - 150$ mV) ± 100 mV or (V_{SS} + 150 mV) ± 100 mV. To buffer I/O2 an external 100 nF capacitor should be connected between pin 42 and V_{SS}. To handle the IST bus specification a transformer with a ratio – IST bus: PCB2310 = 1 : 2 is required.

I/O1 is also the input pin for the receiver comparator. The comparator reference voltage is derived from the voltage on pin 42. There is some hysteresis built in to the comparator. The comparator can handle input pulse limits as defined in Fig. 2.3-1.

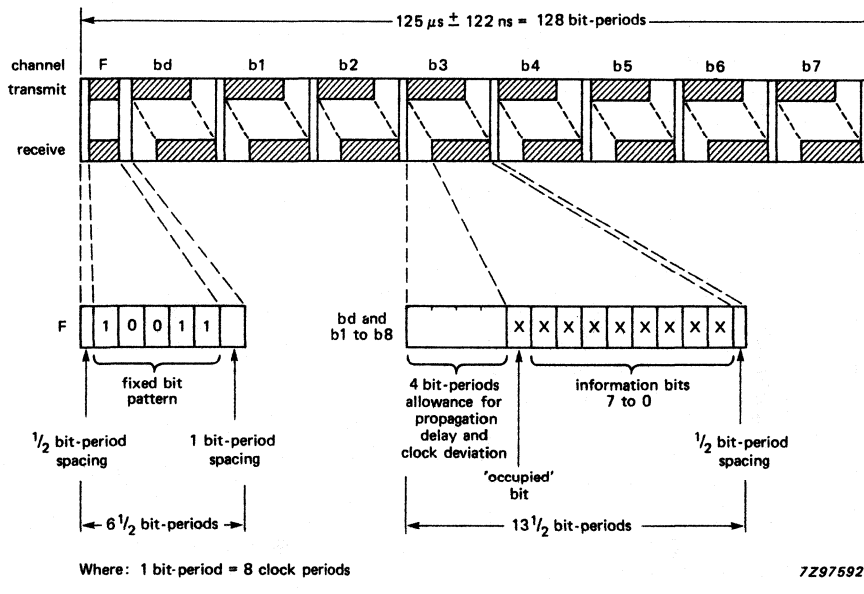


Fig. 2.2-1 IST bus 10 channel frame structure.

DEVELOPMENT DATA

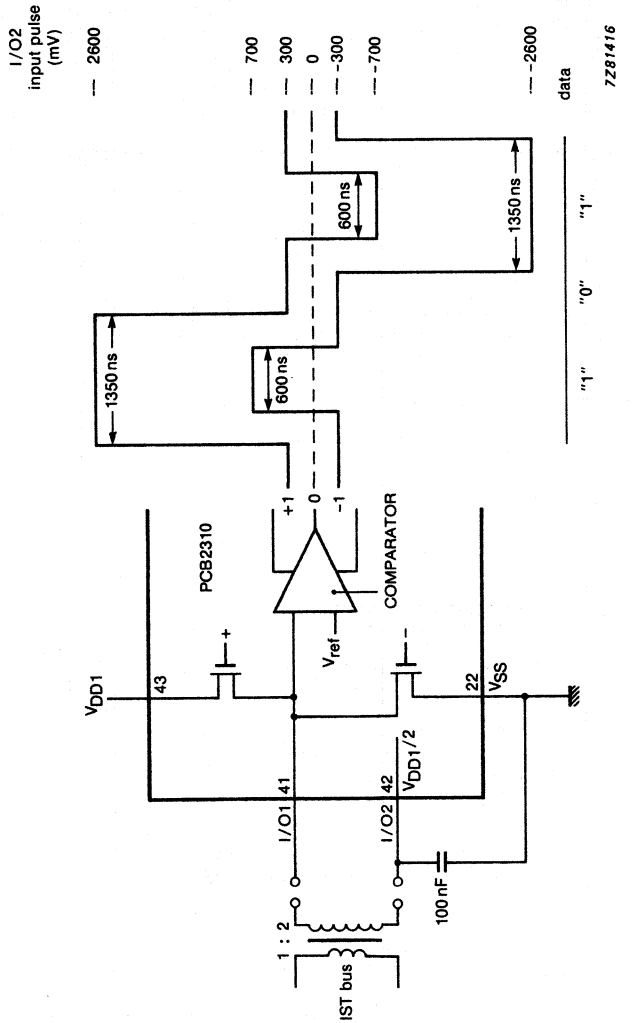
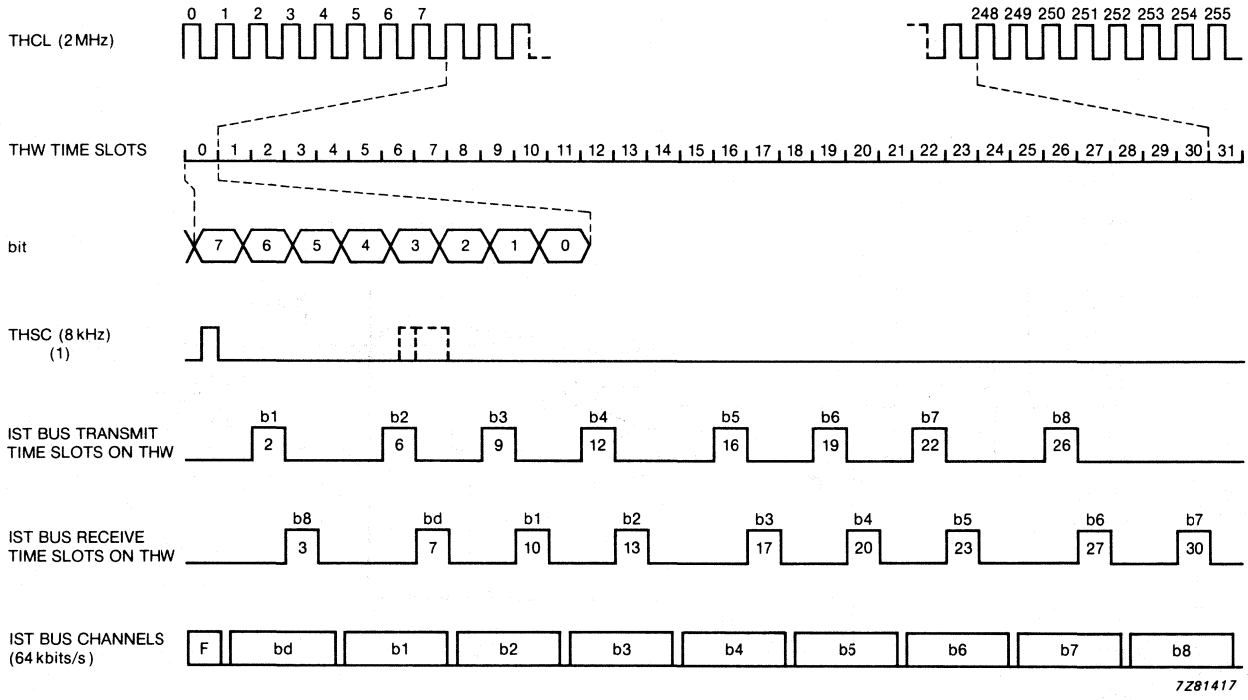


Fig. 2.3-1 IST bus: (a) line driver output stage; (b) receiver input stage.



(1)

THW normal mode – THSC falls over bit 1 of THW time slot 0.
THW monitor mode (IST bd not occupied) – THSC falls over bit 0 of THW time slot 6.
THW monitor mode (IST bd occupied) – THSC falls over bit 0 of THW time slot 6 and bit 7 to 0 of time slot 7.

Fig. 2.4-1 IST <----> THW mapping.

2.4 Terminal highway interface

The Terminal Highway (THW) is a 2 Mbit/s three-wire fully duplex PCM highway for 64 kbit/s circuit-switched channels. The THW will normally be used to interconnect a PCM codec filter or a data terminal that transmits in one of the IST b1 to b8 channels.

The THW offers 32 time slots, 17 of which are used to transmit and receive the IST bus channels. Channels b1 to b8 and bd are mapped upon fixed time slots on the THW (see Fig. 2.4-1). The remaining 14 time slots are 'free'. The THDA data is clocked with the 2048 kHz clock. However, time slots 0 and 31 may be temporarily clocked with a clock period that varies by 25% for synchronization.

The THW interface can operate in 3 separate modes:

- Master
- Slave
- Monitor

When THSL (pin 9) is LOW either the THW master mode or the THW monitor mode is selected. When THSL is HIGH the THW slave mode is selected. The distinction between THW master mode and THW monitor mode is made by setting bit 2 of internal register 6. If this bit is HIGH the monitor mode is choosen. This register can be accessed using the <LOR> command (see Table 2.7-2 Register allocation).

The master mode is the normal operating mode of the THW. In this mode the PCB2310 provides the THW bus with a 2048 kHz clock output (THCL; pin 37) and an 8 kHz synchronization output (THSC; pin 35). See Fig. 3.3-1 THW timing.

The THW monitor mode can be used to monitor the bd channel on the IST bus. In this mode the PCB2310 provides a time slot assignment signal on the 8 kHz synchronization output (THSC; pin 35). If the bd channel on the IST bus is occupied the THSC sync pulse is extended with a strobe. This strobe-signal falls over time slot THW 7.

When several PCB2310s are connected together (e.g. by a PCM 30 switch) the THW slave mode is used. In this mode the terminal highway synchronization input (THSC; pin 35) and the clock input (THCL; pin 37) are provided by peripheral circuits. In this application the PCB2310 is frequency and phase locked to the external inputs, and will be master on the IST bus. The consequence of this application is that only one terminal connected to the same IST bus can have a slave connection on the THW.

2.5 SLD bus interface/time slot assignment outputs

Pins 14, 15 and 16 perform either the SLD interface or the time slot assignment on the THW. Mode selection is defined by TSA/$\overline{\text{SLDEN}}$ (pin 12); TSA/$\overline{\text{SLDEN}}$ = HIGH selects time slot assignment mode (TSA).

2.5.1 TSA mode

In the TSA mode pins 11, 13, 15 and 16 output strobe pulses that fall over specific time slots on the THW. These strobe pulses can be used to clock data to and from the THW. The time slots will be set by command <SBS> (see section 2.7.5).

2.5.2 SLD mode

When TSA/$\overline{\text{SLDEN}}$ is LOW the SLD feature switch is selected. The SLD bus is used to connect B channel devices, such as interfaces to other networks or codecs. The B_1 and B_2 channels of the SLD bus can be switched to any of the THW time slots by the SLD switch. In this way it is possible to map IST b1 to b8 channels via the THW onto the SLD B_1, B_2 channels, and vice versa.

$$\text{IST b1 to b8} \xleftrightarrow{\text{FIXED MAPPING}} \text{THW} \xleftrightarrow{\text{CONTROLLABLE ALLOCATION}} \text{SLD}(B_1, B2)$$

The selection of channels is programmable via the microcontroller I/O port with command <SBS> (see section 2.7.5).

In the SLD mode the PCB2310 can be master or slave on the SLD bus. If TSA = LOW and MM = HIGH the SLD master mode is selected. If TSA = LOW and MM = LOW the SLD slave mode is chosen.

2.5.3 Master mode

In the master mode the SLD bus is provided with the 512 kHz clock signal (SCLK; pin 15) and the 8 kHz synchronization signal (ESC/SDIR: pin 14). In the master mode the PCB2310 controls the SLD bus and thus the PCM codec filter connected to it. In the slave mode the PCB2310 expects an externally provided clock and synchronization signal.

In the master mode the B_1, B_2, C and S channels are transmitted by the PCB2310 when ESC/SDIR is HIGH. The idle code for B_1, B_2 and C channels is all logic 1's and for the S channel all logic 0's. When ESC/SDIR is LOW the SIP output pin is high impedance and data can be received on the SIP pin (see Fig. 2.5-1).

A microcontroller can control the duplex C channel via the control path of the PCB2310. The PCB2310 inserts an NOP code (= hex FF) when no information is offered by the microcontroller for transmission in this channel.

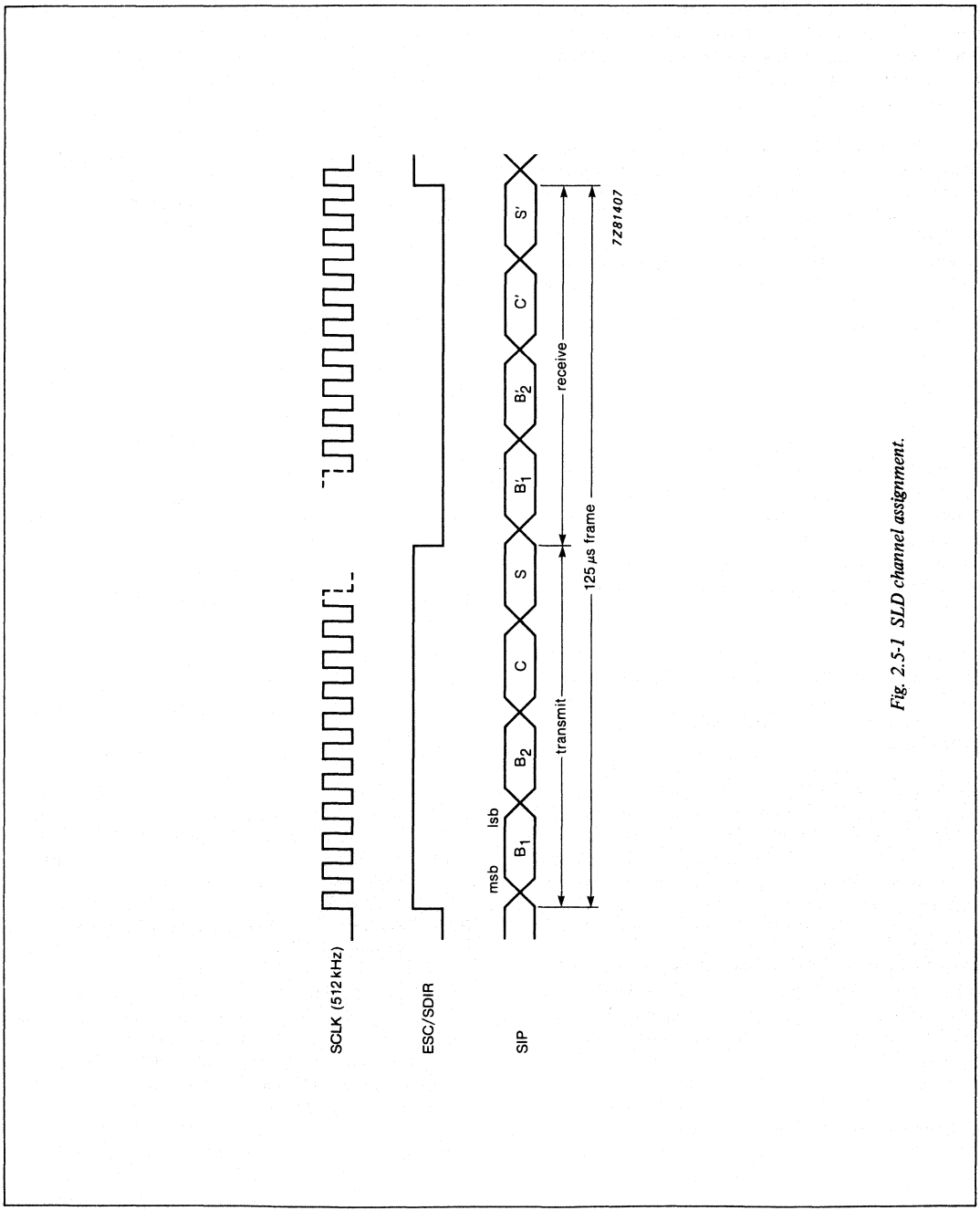


Fig. 2.5-1 SLD channel assignment.

The PCB2310 provides a transparant transmit and receive path for the microcontroller onto the duplex S channel. The receive path is equipped with a last-look detector. A maskable interrupt request ($\overline{IREQ}$) is generated by:

- Any data contents change
- Any byte being transmitted in the S transmit channel

2.5.4 Slave mode

In the slave mode the PCB2310 acts similar to an SLD codec. Another device must be master on the SLD bus. In the slave mode the PCB2310 can be programmed to transmit on either one or both the B_1 and B_2 channels when ESC/SDIR is LOW. The S and C channel outputs are high impedance.

The PCB2310 synchronizes on to the 8 kHz ESC/SDIR signal if it is IST master, SLD slave and VSL = HIGH.

2.6 8-bit microcontroller bus

The PCB2310 is completely controllable by the 8-bit microcontroller bus which is compatible with the MAB80C51 8-bit microcontroller bus.

The bus consists of:

- 8 data/address multiplexed I/O lines (DB7 to DB0; pins 18 to 20 and 23 to 27)
- An interrupt request output ($\overline{IREQ}$; pin 29)
- A read input ($\overline{RD}$; pin 30)
- A write input ($\overline{WR}$; pin 31)
- An address latch enable input (ALE; pin 32)
- A chip enable input ($\overline{CE}$; pin 33)

When ALE is HIGH and $\overline{CE}$ is LOW, data on the DB7-0 I/O port is latched into the address latch. One from four internal registers (P80 to P83; see Fig. 2.6-1) is selected. The PCB2310 stores, then writes the data-byte from the data-bus I/O port into the addressed register (see Table 2.6-1).

Table 2.6-1 Register addresses

REGISTER	ADDRESS							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P80	1	0	0	0	0	0	0	0
P81	1	0	0	0	0	0	0	1
P82	1	0	0	0	0	0	1	0
P83	1	0	0	0	0	0	1	1

The P80 to 83 registers have the following functions:

- P80; PCB2310 interrupt vector/mask register
- P81; PIO status register
- P82; main IST bus control, bd channel and SLD (C) channel I/O port (including a 16-byte FIFO)
- P83; S channel I/O of SLD bus

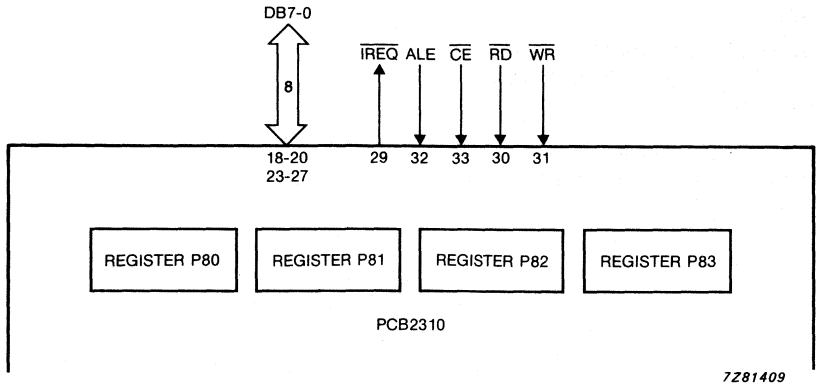


Fig. 2.6-1 8-bit microcontroller I/O port.

2.6.1 Registers P80, P81 (see Table 2.6-2)

The PCB2310 generates maskable interrupt requests ($\overline{IREQ}$) if:

- A different information byte has been received on the S'channel of the SLD bus

and

- The last byte loaded in register P83 has been transmitted in the S channel on the SLD bus for the first time
- The FIFO is loaded with data waiting for transfer to the microcontroller
- The FIFO is waiting for more information during receive mode

The microcontroller interface can be used in two modes or a mixture of both:

- Polling mode
- Interrupt mode

Table 2.6-2 Bit assignment; register P80, P81

COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
read P80	IDIR	IDOR	IRDR	ISSR	ISST	NB2	NB1	NB0
write P80	MDIR	MDOR	MRDR	MSSR	MSST			
read P81	DIR	DOR	BCE	SSR	SST	NB2	NB1	NB0
write P81	ETR	DRQ						

2.6.1.1 Polling mode

When using the polling mode all masked bits of register P80 (bits D7 to D3) must be set to logic 0. When using the mixed mode some bits could be set to logic 1.

In the polling mode the microcontroller polls each peripheral device that is connected to it. When polling the PCB2310 it reads register P81.

Table 2.6-3 Register P81; polling bits

BIT	ACTION
read	
DIR*	Data Input Request indicates FIFO is free for next part of the message (< 16 bytes). This bit will be reset if the microcontroller writes to register P82 FIFO or whenever an ETR or DRQ instruction is given. A write request to P82 FIFO should always end with a ETR or DRQ bit being written to P81.
DOR*	Data Output Request indicates that there is data waiting for output to the microcontroller. BCE is asserted when the microcontroller started the action of fetching data from the PCB2310. If BCE is logic 0 then the PCB2310 initiated the data transfer. DOR bit will be reset by reading the P82 FIFO or by writing ETR or DRQ bit to P81. Writing to P82 FIFO will overrule the data output request. Reading the P82 FIFO should always end by writing ETR bit to P81.
SSR*	SLD Signalling byte Received indicates that a change has been detected in the bytes coming from the SLD S′ channel. The last byte will be held until read by the microcontroller. The data in the SLD S′ register is valid if SSR is asserted. This bit will be reset by reading the P83 register.
SST*	SLD Signalling byte Transmitted. The byte, last loaded by the microcontroller, has been transmitted to the SLD S channel. This bit is set to logic 0 if a new byte is loaded in the P83 register.
BCE	Busy on Command Execution indicates that an operation is in progress. No new command may be entered until BCE is negated. This bit is set when a command is entered and reset when the command has been interpretted and handled. If the microcontroller is fetching data from the PCB2310, BCE will be logic 1 provided the data has been read by the microcontroller and the read cycle is ended with ETR being written to P81.
NB2 to NB0	This indicates the number of bytes in the FIFO in the event of a Data Output Request being initiated by the PCB2310 (BCE = logic 0). A data output request initiated by the microcontroller will always result in 16 bytes being loaded in the FIFO by the PCB2310; thus NB2 to NB0 will have no meaning.

Table 2.6-3 (continued)

BIT	ACTION
write	
ETR	End of transmission. The microcontroller must set this bit to indicate the end of transmission. This applies to the PCB2310 writing or reading data to the P82 FIFO. If ETR is issued during a PCB2310 data output phase, the P82 FIFO will be cleared. Afterwards a new trial will attempt to output the interrupted data.
DRQ	Data request. With this signal the microcontroller indicates to the PCB2310 that it will switch the transmission direction from WRITE to READ. It will force the PCB2310 to fill the FIFO with appropriate data and generate interrupt RDR.

2.6.1.2 Interrupt mode

In Table 2.6-3 all bits marked with an asterisk will generate an interrupt if asserted. If more interrupts are asserted at the same time only one is marked in register P80; the others are pending. However, in register P81 all valid bits are written.

Table 2.6-4 Register P80; interrupt bits

BIT	ACTION
write	
MDOR	Mask interrupt IDOR if asserted
MRDR	Mask interrupt IRDR if asserted
MDIR	Mask interrupt IDIR if asserted
MSSR	Mask interrupt ISSR if asserted
MSST	Mask interrupt ISST if asserted
	condition: power on; all masks set to logic 0; all interrupts disabled.
read	
ISSR	SSR x MSSR x priority
ISST	SST x MSST x priority
IDIR	DIR x MDIR x priority
IDOR	DOR x MDOR x BCE x priority
IRDR	DOR x MRDR x BCE x priority
	priority: ISSR has priority over ISST. ISST has priority over IDIR, IDOR and IRDR. IDIR and IDOR and IRDR are mutually exclusive and will not occur at the same time. $IREQ = (\overline{IDIR} + \overline{IDOR} + \overline{IRDR} + \overline{ISSR} + \overline{ISST})$

Interrupt bits will be reset by reading PO.

2.6.2 Register P82; FIFO data path

Register P82 is the main IST bus control, bd channel and SLD (C) channel I/O port. It includes a 16-byte FIFO for adaptation to the 8 kbyte/s processing capability of the PCB2310. The PCB2310 is a multi-function device which requires a CONTROL byte <CTRL> after P82 has been addressed, to select between the various chip functions. <CTRL> can be followed by a PARAMETER byte(s) <PAR> for extension of the data destination address (pointers, channel numbers etc.). The PCB2310 can transfer data to the microcontroller by its own initiation, or when initiated by the microcontroller.

Table 2.6-5 displays the protocol that is implemented on register P82 FIFO address. There are 3 modes: a, b and c.

- a: PCB2310 input
- b: PCB2310 input/output
- c: PCB2310 output

Table 2.6-5 Register P82; I/O commands

MODE	PROTOCOL
PCB2310 input initiated by microcontroller (< 16 bytes)	
a	P82 write <CTRL>[<PAR>] [<DATA>]; P81 write ETR.
b	P82 write <CTRL>[<PAR>] [<DATA>]; P81 write DRQ; wait for DOR and BCE = logic 1 or IRDR; P82 read <DATA>; P81 write ETR.
PCB2310 input initiated by microcontroller (> 16 bytes)	
a	P82 write (16 bytes) <CTRL>[<PAR>] [<DATA>]; wait for DIR or IDIR, P82 write (next bytes) <DATA>; P81 write ETR.
b	P82 write (16 bytes) <CTRL>[<PAR>] [<DATA>]; wait for DIR or IDIR, P82 write (next bytes) <DATA>; P81 write DRQ; wait for (DOR and BCE) or IRDR; P82 read (16 bytes) <DATA>; wait for (DOR and BCE) or IRDR; P82 read (next bytes) <DATA>; P81 write ETR.
PCB2310 output initiated internally (DOR = logic 1 and BCE = logic 0 or IDOR = logic 1)	
c	P82 read <CTRL>[<PAR>] [<DATA>]; number of bytes written in NB2 to NB0.

Where:

<CTRL> = control command byte
<PAR> = one or more parameter byte(s)
<DATA> = one or more information byte(s)
[ ] = optional

Table 2.6-6 Register P82; I/O control commands

MNEM.	OP. CODE <CTRL>	PARAMETER <PAR>	DATA [<DATA>]	MODE*	DESCRIPTION
					internal RAM/register read/write access
LOD	10	^1st address	n bytes	a	load data in RAM
LOR	11	^1st address	n bytes	a	load register RR
FED	12	^1st address	–	b	fetch data from RAM
FER	13	^1st address	–	b	fetch register
RST	00	–	–	a	soft reset and start**
					bd channel interface primitives
LSP	08	IST_DEA	[n bytes]	a	load 's' transmit buffer
LST	09	[IST_DEA]	[n bytes]	a	load 's' transmit buffer and transfer
LDP	0A	IST_DEA	[n bytes]	a	load 'd' transmit buffer
LDT	0B	[IST_DEA]	[n bytes]	a	load 'd' transmit buffer and transfer
TSC	0E	–	–	b	transfer 's' receive buffer to microcontroller
TDC	0F	–	–	b	transfer 'd' receive buffer to microcontroller
RSB	01	–	–	a	release 's' receive buffer
RDB	02	–	–	a	release 'd' receive buffer
SPR	31	–	3 bytes Δ	c	's' packet receive indication
DPR	32	–	3 bytes	c	'd' packet receive indication
SPT	33	–	–	c	's' packet transmit confirmation
DPT	34	–	–	c	'd' packet transmit confirmation
SPF	23	–	–	c	's' packet transfer failure indication
DPF	24	–	–	c	'd' packet transfer failure indication
					SLD channel control
SBS	18	TS	[TS]	a	SLD B channel/TSA selection
SCT	1A	–	[n bytes]	a or b	SLD C channel transfer
					circuit-switched channel selection
FFC	03	–	–	a	fetch free channel
OAR	0D	IST b1-8	–	a	occupy channel directly after release
RCH	0C	IST b1-8	–	a	release channel(s)
CHC	30	IST b1-8	–	c	channel has been connected

DEVELOPMENT DATA

Table 2.6-6 (continued)

MNEM.	OP. CODE <CTRL>	PARAMETER <PAR>	DATA [<DATA>]	MODE*	DESCRIPTION
					master-slave arbitration/maintenance
FMF	22	–	–	c	FCM transfer failure indication
TRM	06	–	–	c	Transmit TOM
TMP	20	–	–	c	IST bus down
TMF	21	–	–	c	IST bus up
					external synchronization procedures
ESR	04	–	–	a	external synchronization request
RES	05	–	–	a	release external synchronization
ESO	25	–	–	c	external synchronization is on
ESW	26	–	–	c	external synchronization is required
RSP	27	–	–	c	release of external synchronization will proceed

Where:

[. .] = optional

– = no parameter or data-bytes

* = modes a, b and c are as in Table 2.6-5

^1st address = pointer to first register/RAM address

IST_DEA = IST destination address. The message loaded in the PCB2310 will be transmitted in the bd channel and the IST destination address is transmitted in the control byte of the bd message.
(see bd message format Table 2.8-1).

IST b1-8 = The format of the parameter is as follows:

bit 7 0

b8	b7	b6	b5	b4	b3	b2	b1

In the commands <OAR> and <RCH> a logic 1 in one or more specific bit position(s) indicates that the applicable channel(s) should be occupied then released. In the response <CHC> a logic 1 in the specific bit position indicates that the appropriate channel has been occupied. All logic 0's in the parameter indicates that all channels are occupied at the moment.

** = <RST> command is used for initialization.

Δ = see section 2.7.4; bd channel interface primitives.

TS = Up to four parameter bytes can be given. The format of the parameter is as follows:

bit 7 0

c	c	c	c	c	d	b	b

ccccc = the 5-bit binary decoding of the THW_slot_nr

If TSA = LOW the <SBS> command controls the SLD switch

d = 0; SIP output is inactive –
SLD slave : 3-state
SLD master: all logic 1's

d = 1; SIP output is active

bb = 00; THW time slot ccccc is switched to B_1 SLD
01; THW time slot ccccc is switched to B_2 SLD
10; B_1 SLD is switched to THW time slot ccccc
11; B_2 SLD is switched to THW time slot ccccc

If TSA = HIGH the <SBS> command programs the strobe outputs

d = don't care

bb = 00; strobe signal RX1 (pin 13) falls over THW time slot ccccc
01; strobe signal RX2 (pin 11) falls over THW time slot ccccc
10; strobe signal TX1 (pin 16) falls over THW time slot ccccc
11; strobe signal TX2 (pin 15) falls over THW time slot ccccc

2.7 Command description

2.7.1 Internal RAM/register read/write access

Commands to access the internal 256 x 8 RAM:

- <FED> to READ
- <LOD> to WRITE

Commands to access the internal registers:

- <FER> to READ
- <LOR> to WRITE

Care must be taken when writing to RAM and register locations otherwise it may cause unwanted actions.

Table 2.7-1 RAM allocation map

ADDR. HEX.	CONTENTS OF LOCATION
00 01 02	temporary buffer – IST bus address*
03 .. .. 0E	these RAM byte locations are for internal use and are not allowed to be accessed by the user
0F 10 11	pointer to first address of 'd' transmit buffer** pointer to first address of 's' receive buffer pointer to first address of 'd' receive buffer
12 .. 1F	these RAM byte locations are for internal use and are not allowed to be accessed by the user
20 ..	's' transmit buffer
.. ..	'd' transmit buffer
.. ..	's' receiver buffer
.. FF	'd' receive buffer

Where:

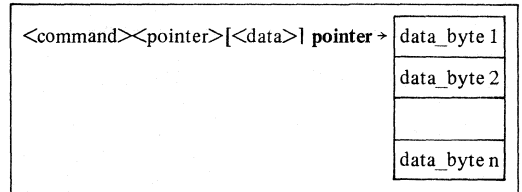
* The IST bus, 5-bit binary coded address, should be loaded at initialization by the user.

bit 7 0

xxx IST addr

Each member on the IST bus should have a different address. If an addressed packet is transmitted on the bd channel, the only PCB2310 loading the packet will be the one whose IST bus address is equal to the DEA address (see Table 2.7-1). Broadcast messages will be loaded by all PCB2310s connected to the IST bus.

** The user allocates the buffer pointers by initialization (see <RST> command Table 2.6-6).



Initially the pointer is equal to <pointer>. Each time a new <data> is written/read the pointer is incremented.

Fig. 2.7-1 Internal RAM/register read/write access.

2.7.2 Registers

The address map of the internal PCB2310 registers and data bus I/O ports is shown by Table 2.7-2. The addresses are the access codes to input or output a byte to or from the internal data bus.

Table 2.7-2 Register allocation

ADDR.	PURPOSE OF THE ADDRESS	REMARKS
RR01	RAM I/O port enable	–
RR02	RAM address register	–
RR03	PIO input/output reg.	PIO register; Port 2
RR04	TIO input/output reg.	bd channel I/O register
RR06		
	bit 0 = PIO transmit bit	PIO in output mode
	bit 1 = TIO transmit bit	TIO in output mode
	bit 2 = monitor mode bit*	testing
	bit 3 = external sync on	8 kHz on pin 13 (ESC)
	bit 4 = external reset	'1' (1 ms) during power up
	bit 5 = occupied frame	start bit F channel det.
	bit 6 = enable bd	transmit in bd channel
	bit 7 = occupied bd	start bit bd channel det.
RR0A	register A	internal register A
RR0B	register B	internal register B
RR0C	register C	main control register
RR0D	enable b1 to b8	transmit in b1 to b8 channel
RR0E	occupied b1 to b8	start bit b1 to b8 channel detected
RR0F		
	bit 0 = initialization 1	used during initialization
	bit 1 = initialization 2	used during initialization
	bit 2 = any signal on IST	signal detected on IST bus
	bit 3 = RR0F 2 delayed	used during start up
	bit 4 = not used	–
	bit 5 = VSL	connected to pin 8 (VSL)
	bit 6 = lock	locked to F channel (8 kHz)
	bit 7 = master/enable frame	transmit in F channel
RR20	SLD B_1 Transmit	THW channel/SLD driver
RR21	SLD B_2 Transmit	THW channel/SLD driver
RR22	SLD B'_1 Receive	THW channel
RR23	SLD B'_2 Receive	THW channel
RR24	SLD Control	SLD C channel I/O

Where:

* The THW monitor mode can be chosen with <LOR><06><04>.
Be aware that the <RST> command also resets the THW monitor mode.

Note: Registers not mentioned are not used.

2.7.3 Reset command

After RESET (pin 7) goes LOW (internally or externally activated; see section 2.9) a chip 'wait state' follows. In this event the IST bus address must be loaded at RAM location hex 02 using command <LOD> and the pointers to the first addresses of the various packet buffers must be loaded in RAM address hex 0F-11 (see Table 2.7-1). After reception of the command <RST> the PCB2310 enters the normal operating mode.

<LOD> and <RST> command the start up operation of PCB2310.

- 1st command : <LOD><02><IBA>
- 2nd command: <LOD><0F><--><--><-->
- 3rd command : <RST>

If the <RST> command is received during normal operation, provided the PCB2310 is an IST slave terminal and a gateway station (VSL = logic 1), it will transmit a TOM Frame Control message in the bd channel. An inhibited IST master function will be reset (see section 2.7.7; master-slave control).

2.7.4 bd channel interface primitives

Transmit

To transmit 's' or 'd' type messages the following four primitives are used:

- <LSP>; <LST>:
<'s'_type_transmission_request><<data>>
- <LDP>; <LDT>:
<'d'_type_transmission_request><<data>>

With command <LST> the 's' transmit buffer is loaded and transmitted in the bd channel.
With command <LDT> the 'd' transmit buffer is loaded and transmitted in the bd channel.
The first data byte in these buffers is used as the IST destination address in the bd message control field.
At the end of the message transfer two CRC bytes are added by the PCB2310.

With command <LSP> an 's' type message could be loaded in the 's' transmit buffer without being transmitted.
With command <LDP> a 'd' type message could be loaded in the 'd' transmit buffer without being transmitted.
The information stored in the 's' and 'd' buffers can then be transmitted with additional data bytes, if required, by commands <LST>, <LDT> respectively.

Note:

The first byte loaded by commands <LSP>, <LDP> is used as the IST destination address.

Data stored in these buffers is held until new data is loaded. Thus it is possible to re-transmit previously stored messages by command <LST> or <LDT>.

If an 's' or 'd' packet is transferred correctly an <SPT> or <DPT> transfer_confirmation primitive is given.

If an 's' or 'd' type message could not be transferred correctly an <SPF> or <DPF> error indication is issued.

If after four internally generated re-transmissions $\overline{ACK}$ is still received (see IST bus specification) this indicates that a message could not be transferred correctly.
If an internal frame control message could not be transferred correctly an <FMF> primitive is issued (see IST bus specification and section 2.8 bd channel protocol).

Receive

When an 's' or 'd' type packet is received correctly the PCB2310 initiates a message received primitive:

- <SPR>: <'s' message received indication><<data>>
- <DPR>: <'d' message received indication><<data>>

The 3 data bytes that follow these <SPR>, <DPR> primitives indicate:

- 1st byte : pointer to (last address + 1) of packet loaded in RAM
- 2nd byte: first byte of received packet
- 3rd byte : second byte of received packet

With commands <TSC>, <TDC> the received packet, minus first two bytes, is transferred to the microcontroller (first two bytes of the packet will not be transmitted again). The number of bytes to be fetched is:

(1st byte received after <SPR>, <DPR> command) – (pointer_to_first_buffer location) – 2.

Provided 's' or 'd' receive buffers are not released with command <RSB> or <RDB>, the PCB2310 will be blocked to receive any further message of the type of held in the filled buffer. The PCB2310 will now transmit an $\overline{ACK}$ on the IST bus. In effect this is flow control.

2.7.5 SLD channel control

The S channel is 'quasi transparant' through the PCB2310 and is controlled directly via address P83 on the microcontroller port.

The B_1 and B_2 channels are controlled by command <SBS> and the C channel by command <SCT>.

The <SBS> command can be used in both SLD master mode and SLD slave mode. The <SCT> command is only effective in the SLD master mode.

The <SBS> command writes directly to one or more registers that control the SLD/THW switch. Channels b1 to b8 on the IST bus are mapped upon time slots on the THW and from then on can be switched to the SLD B channels and vice versa.

In the TSA mode the <SBS> command data bytes determine the THW time slot strobe signals.

Following the <SCT> command data bytes are transferred in the SLD C channel. If there are no data bytes to be transmitted an NOP code (hex FF) is transmitted in the SLD master mode. If data is expected in return on the SLD C′ channel the <SCT> command should be ended by writing the DRQ bit instead of ETR bit in P81.
Bits DOR and BCE in the polling mode, or IRDR when in the interrupt mode, indicates that 16 bytes received on the SLD C′ channel have been loaded in the P82 FIFO. The maximum number of bytes that can be returned to this channel is 16.

2.7.6 Circuit-switched channel control (IST b1 to b8)

With command <FFC> a free IST b channel will be occupied. If a channel has been occupied, the PCB2310 issues a <CHC> primitive; the parameter following this command indicates which channel has been occupied. If there is no free channel the parameter following <CHC> is hex 00. The data on the corresponding THW time slot will be transmitted in the occupied IST b channel (see Fig. 2.4-1).

With the command <RCH> followed by a parameter the indicated IST b channel will be released. If the parameter is hex FF all channels occupied by the PCB2310 will be released.

With the <OAR> command* followed by a parameter indicating an IST b channel, that specific channel will be occupied immediately after it has been released. If the channel has been occupied a <CHC> primitive will be issued. This makes it possible to transfer IST b channel control from one PCB2310 to another.

*If an <OAR> command is issued the PCB2310 will wait until that specific channel has been released. An <FFC> command must never be released before the <OAR> command has been completed by receiving a <CHC> confirmation.

2.7.7 IST master-slave control/maintenance commands

The complete master-slave protocol as prescribed in the IST bus specification is implemented in the PCB2310. The PCB2310 initiates a data output request if there is no signal on the IST bus for at least one IST frame (125 μs). The command sent is <TMP>. When there is a signal on the IST bus the command <TMF> will be issued.

If a terminal wants to disconnect from the IST bus lines it has to issue a <TRM> command to the PCB2310. The PCB2310, if IST master, will cease transmission in the frame channel as soon as all circuit-switched IST b1 to b8 channels are free and the master/slave arbitration procedure starts again. To enable the PCB2310 again an <RST> command should be entered. If the command <TMP> followed by <TMF> is received or <TMF> only is received the terminal is allowed to disconnect from the IST bus.

2.7.8 External synchronization procedures

These procedures are used to synchronize the IST bus to an external network connected via a gateway. They also incorporate additional PCB2310s on the same IST bus being connected to an external network.

With <ESR> command the microcontroller, via the PCB2310, requests the IST bus to synchronize to an 8 kHz external source. The PCB2310 that is IST master will issue an <ESW> primitive which indicates to the microcontroller that external synchronization is requested. After external synchronization has been established the PCB2310 gives an <ESO> primitive confirmation.

Once external synchronization is established terminals can communicate via the gateway to other networks.

To terminate the external synchronization an <RES> request should be entered in the PCB2310. Provided no <ESR> primitive occurs within the next 8 seconds, the PCB2310 will ask the microcontroller to release the external synchronization by an <RSP> confirmation primitive.

2.8 bd channel protocol

The PCB2310 implements full layer 1 and 2 protocol as described in the IST bus specification. The service access point of the layer 2 entity is register P82 FIFO (see section 2.7.4 bd channel interface primitives). If the THW is in monitor mode the bd channel receiver information is mapped to the THW time slot 7 for test purposes.

Features of the bd channel layer 2 functions

- Packet-switched transmission
- Specific destination or broadcast address
- Access via microcontroller I/O port
- Error detection/correction by re-transmission
- Flow control
- Byte oriented
- Fully transparant for layer 3 messages

Table 2.8-1 bd channel message format

MESSAGE	DESCRIPTION
1	<I , s, DEA><<DATA>> <CRC><CRC><EMPT><$\overline{\text{ACK}}$>
2	<I , d, DEA><<DATA>> <CRC><CRC><EMPT><$\overline{\text{ACK}}$>
3	<C, FCM> <CRC><CRC><EMPT><$\overline{\text{ACK}}$>

Where:

< >	=	byte
<< >>	=	0 to n bytes
DEA	=	5-bit destination address (logic 0 = broadcast). DEA is the 5 least significant bits of the first byte loaded in the 's' or 'd' buffer. (see Table 2.6-5; <LST> and <LDT>)
DATA	=	data octets
CRC	=	first and second octet of the CRC word
EMPT	=	empty bd channel during one frame (no start and data bits)
$\overline{\text{ACK}}$	=	not acknowledge code (11111111)
FCM	=	frame control message
I	=	information mode (I = logic 0)
C	=	link control mode (C = logic 1)
s	=	signalling packet (s = logic 1)
d	=	data packet (d = logic 0)

2.8.1 bd channel access protocol

The bd channel access protocol makes use of the Carrier Sense Multi-Access principle with Collision Detection (CSMA/CD). Some extra features have been added which guarantee full accessability under high traffic circumstances, and give signalling messages, loaded in the 's' transmit buffer, priority over waiting data packets loaded in the 'd' transmit buffer (see Table 2.6-6; <LST> and <LDT>).

To shorten the average bus occupation time during collisions, an 'exclusive OR' function has been implemented between the bus transmitter and receiver. This facilitates immediate collision detection by not having to wait for CRC errors at the end of the complete transport. The AMI line code uses the +1 and −1 polarity to transmit a logic 1 on the bus. A logic 0 is transmitted as a floating bus potential

which will be overridden by a logic 1.
A transmitting station can detect this situation by comparing its output with the receiver signal. A collision detected in this way is serviced by transmitting the all logic 1's code in the next frame and then stops transmission. The other stations now have the possibility of detecting the collision and immediately stop transmissions. All stations transmit the $\overline{\text{ACK}}$ code in the N frame and re-transmissions can start by the previously described protocol.

2.9 Reset (see Fig. 2.9-1)

The PCB2310 internal reset circuit will be activated when V_{DD1} is below 1,2 V and rising to 5 V with a slope greater than 5 V/ms and connected to PO (pin 4). It is also possible to reset the PCB2310 externally by a pulse of $> 1\ \mu s$ being applied to PO (active LOW). After reset the PCB2310 initializes all register and RAM locations to zero. At this time the RESET output (pin 7) is active HIGH. This output is used to reset other circuits such as the microcontroller. After pin 7 goes LOW again the PCB2310 expects data to be filled in the RAM followed by the <RST> command (see section 2.7.3; reset command). After reception of the command <RST> the PCB2310 is initialized and enters the normal operating mode. There is no power down mode.

2.10 Monitor mode

The circuit has a built-in mode for monitoring the bd channel. Monitor mode is selected with address RR06 bit 2 (see Table 2.7-2). In this mode the THSC sync pulse has two states:

- Idle bd channel
  THSC pulse has a 1-bit duration and falls over bit 0 of time slot 6
- Busy bd channel
  THSC pulse has a 9-bit duration and falls over bit 0 of time slot 6 and bit 7 to 0 of time slot 7.

2.11 Crystal connection circuit (see Fig. 2.11-1)

One side of the crystal is connected to pin 1. When using an external clock generator pin 1 is not connected. The other side of the crystal is connected to pin 3. An 8192 kHz ± 100 ppm crystal must be used. An external clock generator can also be connected to pin 3.

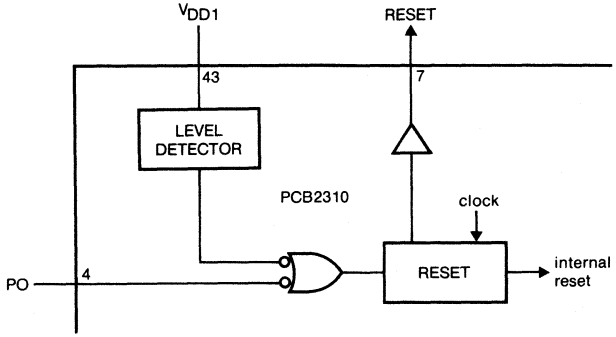


Fig. 2.9-1 Reset circuit (simplified). 7Z81410

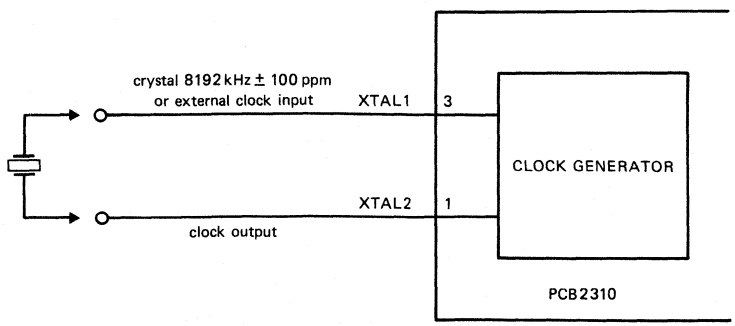


Fig. 2.11-1 Crystal connection. 7Z81408

3.0 ELECTRICAL SPECIFICATION

3.1 Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134).
Voltages are referenced to GND (ground = 0 V)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
DC supply voltage		V_{DD}	−0,5	7,0	V
DC input diode current	$V_I < -0,5$ V or $V_I > V_{DD}$ +0,5 V	$\pm I_{IK}$	–	10	mA
DC output diode current	$V_O < -0,5$ V or $V_O > V_{DD}$ +0,5 V	$\pm I_{OK}$	–	10	mA
DC output source or sink current	$-0,5$ V $< V_O < V_{DD}$ +0,5 V	$\pm I_O$	–	10	mA
DC V_{DD} current		$\pm I_{DD}$	–	50	mA
DC GND current		$\pm I_{GND}$	–	50	mA
Voltage on any pin		V_n	0	V_{DD}	V
Storage temperature range		T_{stg}	−65	+125	°C
Operating ambient temperature range		T_{amb}	0	+70	°C
Total power dissipation	temperature range: 0 to +70 °C above +60 °C: derate linearly with 8 mW/K	P_{tot}	–	500	mW

3.2 DC Characteristics

V_{DD} = 5 V ± 0,25 V; V_{SS} = GND = 0 V; T_{amb} = 0 to +70 °C, unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC supply voltage						
analogue		V_{DD1}*	4,75	5,0	5,25	V
digital		V_{DD2}	4,75	5,0	5,25	V
Inputs						
Threshold voltage						
positive-going	V_{DD} = 5,25 V	V_{T+}	–	–	1,9	V
negative-going	V_{DD} = 4,75 V	V_{T-}	0,5	–	–	V
Hysteresis voltage		V_H	0,5	–	–	V
Input leakage current	T_{amb} = 25 °C; V_I = V_{DD} to 0 V	I_{IL}	−1	–	+1	μA
Outputs						
Output voltage LOW	V_{DD} = 4,75 V; I_{OL} = 20 μA	V_{OL}	–	–	0,05	V
Output voltage LOW THCL; I/O1	V_{DD} = 4,75 V; I_{OL} = 8 μA	V_{OL}	–	–	0,25	V
Output voltage LOW all outputs except THCL; I/O1	V_{DD} = 4,75 V; I_{OL} = 4 mA	V_{OL}	–	–	0,25	V
Output voltage HIGH	V_{DD} = 4,75 V; $-I_{OH}$ = 20 μA	V_{OH}	4,7	–	–	V
Output voltage HIGH THCL; I/O1	V_{DD} = 4,75 V; $-I_{OH}$ = 8 mA	V_{OH}	4,5	–	–	V
Output voltage HIGH all outputs except THCL; I/O1	V_{DD} = 4,75 V; $-I_{OH}$ = 4 mA	V_{OH}	4,5	–	–	V
3-state OFF current	T_{amb} = 25 °C; V_O = V_{DD} to 0 V; I_O = 0	± I_{OZ}	–	–	5	μA
Output current LOW IREQ	V_{OL} = 0,25 V	I_{OL}	–	–	4	mA

* Noise on analogue supply voltage V_{DD1} must be less than 25 mV for frequencies above 1 kHz.

DEVELOPMENT DATA

3.2.1 Capacitance

V_{SS} = GND = 0 V; T_{amb} = +25 °C

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	f = 1 MHz	C_I	–	–	5	pF
Input/output capacitance		$C_{I/O}$	–	–	20	pF
Output capacitance	other outputs to GND	C_O	–	–	15	pF

3.3 AC Characteristics

V_{DD} = 5 V ± 0,25 V; V_{SS} = GND = 0 V; T_{amb} = 0 to +70 °C, unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Terminal Highway (Fig. 3.3-1)	C_L = 200 pF					
THCL						
rise and fall times	note 1	t_r, t_f	–	–	50	ns
clock period		t_W	–	488	–	ns
THDA delay time with respect to THCL						
in master mode		t_d	–	–	30	ns
in slave mode		t_d	–	–	210	ns
rise and fall times		t_r, t_f	–	–	150	ns
THSC						
set-up and hold times		t_{SU}, t_{HD}	–	–	30	ns
rise and fall times		t_r, t_f	–	–	150	ns
THSL	note 2					
SLD bus (Fig. 3.3-2)	C_L = 200 pF					
SCLK rise and fall times		t_r, t_f	–	–	50	ns
SCLK clock period		t_W	–	192	–	ns
SIP delay time with respect to SCLK		t_d	–	–	30	ns
rise and fall times		t_r, t_f	–	–	50	ns
ESC/SDIR delay time with respect to SCLK		t_d	–	–	30	ns
rise and fall times		t_r, t_f	–	–	190	ns
MM	note 2					

DEVELOPMENT DATA

3.3 AC Characteristics (continued)

PARAMETER	CONDITIONS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Microcontroller bus (Fig. 3.3-3)	C_L = 100 pF					
ALE pulse duration		t_{LL}	100	–	–	ns
Address to ALE set-up time		t_{AL}	20	–	–	ns
Address hold time after ALE		t_{LA}	20	–	–	ns
$\overline{RD}$ pulse duration		t_{RR}	100	–	–	ns
$\overline{WR}$ pulse duration		t_{WW}	100	–	–	ns
Data delay time from $\overline{RD}$		t_{RD}	–	–	100	ns
Data hold time after $\overline{RD}$		t_{DR}	50	–	–	ns
Data float delay after $\overline{RD}$		t_{DFR}	–	–	95	ns
Time from ALE to $\overline{RD}$, $\overline{WR}$		t_{LW}	50	–	–	ns
Time from address to $\overline{RD}$, $\overline{WR}$		t_{AW}	20	–	–	ns
Time from $\overline{RD}$, $\overline{WR}$ HIGH to ALE HIGH		t_{WHLH}	20	–	–	ns
Data valid to $\overline{WR}$ transition		t_{DWX}	0	–	–	ns
Data set-up time before $\overline{WR}$		t_{DW}	100	–	–	ns
Data hold time after $\overline{WR}$		t_{WD}	20	–	–	ns
Address float delay after $\overline{RD}$		t_{AFR}	–	–	50	ns
TX1, TX2, RX1, RX2	C_L = 100 pF					
delay time		t_d	–	–	30	ns
rise and fall times		t_r, t_f	–	–	50	ns
IST bus I/O						
Input impedance I/O1, I/O2	f = 0–1 MHz	Z_I	–	–	40	kΩ
positive pulse/ negative pulse		Adt	–	–	5	%

Notes to the a.c. characteristics

1. Terminal Highway cannot be used in time slots 0 to 31. In these time slots clock periods can vary by 25%.
2. Inputs THSL and MM are fixed inputs.

3.3.1 Timing

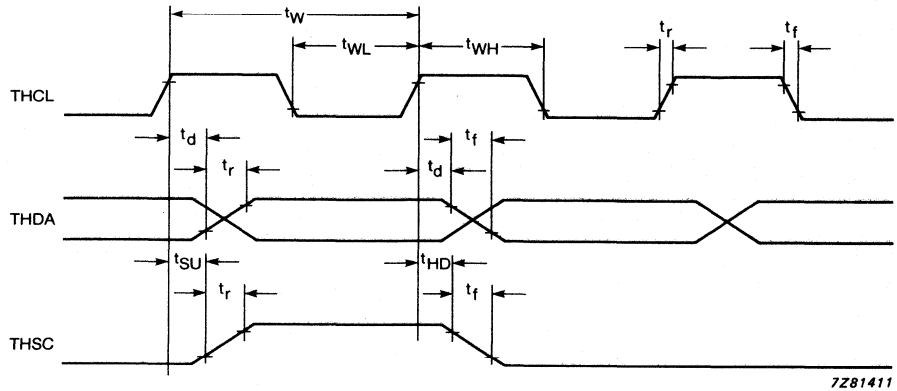


Fig. 3.3-1 Terminal Highway.

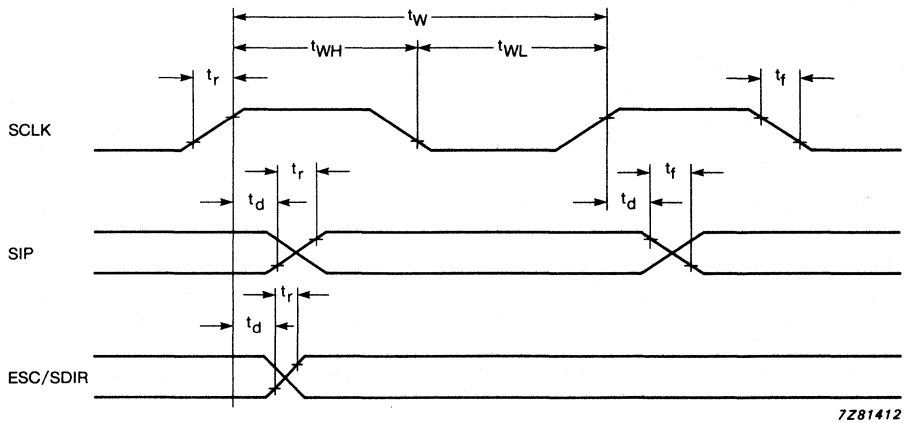
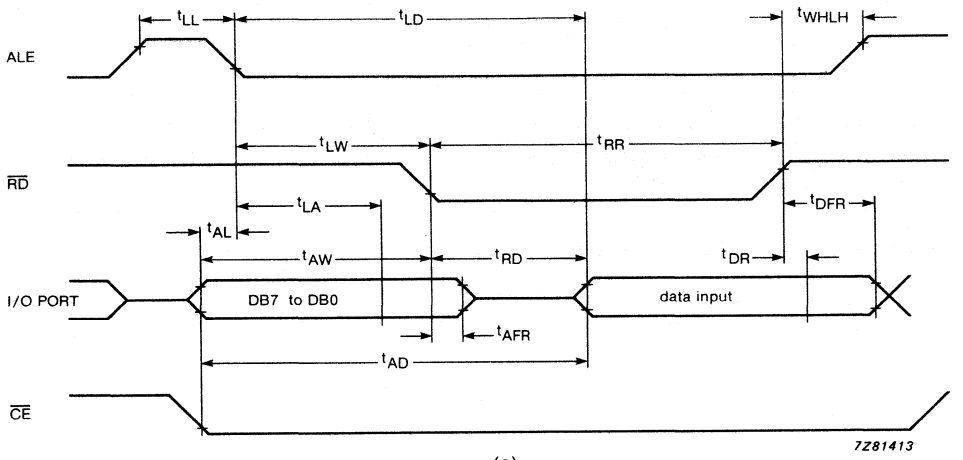
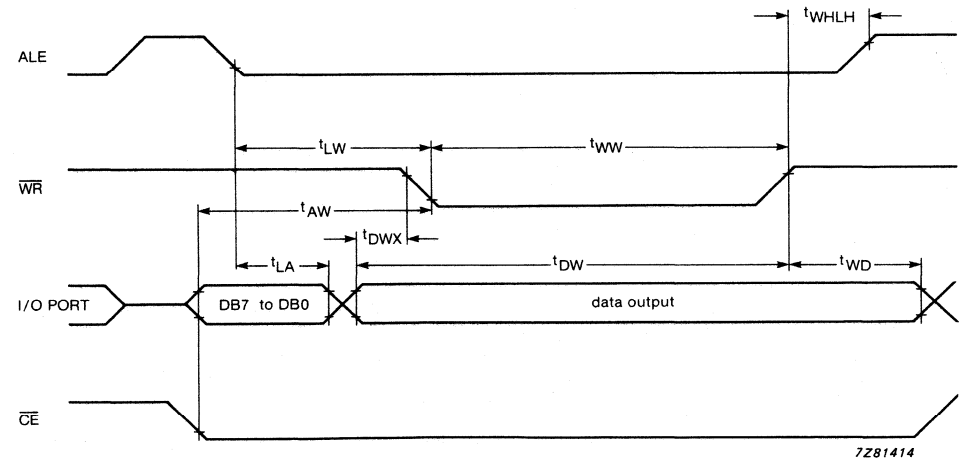


Fig. 3.3-2 Subscriber Line Data bus.

DEVELOPMENT DATA



(a)



(b)

Fig. 3.3-3 Microcontroller bus: (a) read from PCB2310 data memory; (b) write to PCB2310 data memory.

3.4 AC testing

Inputs for a.c. testing are 2,4 V for a logic 1 and 0,45 V for a logic 0.
Timing measurements are made at 2,0 V for a logic 1 and 0,8 V for a logic 0.

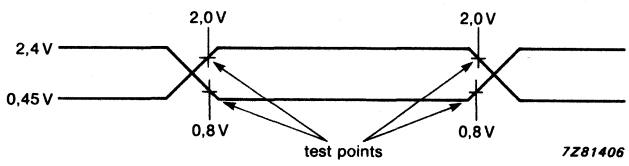


Fig. 3.4-1 Input and output waveforms for a.c. testing.

4.0 APPLICATION INFORMATION

DEVELOPMENT DATA

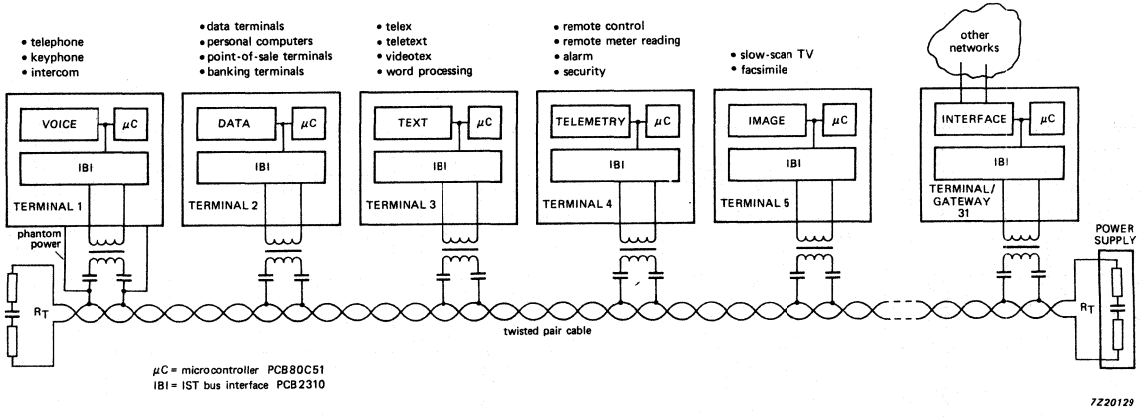
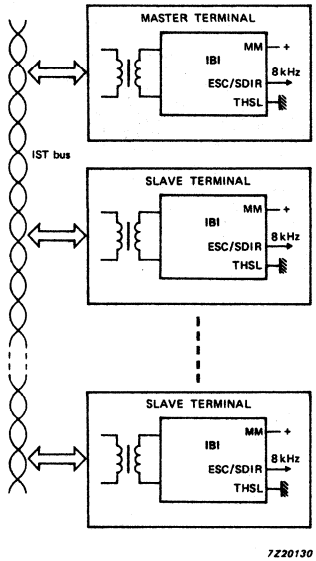
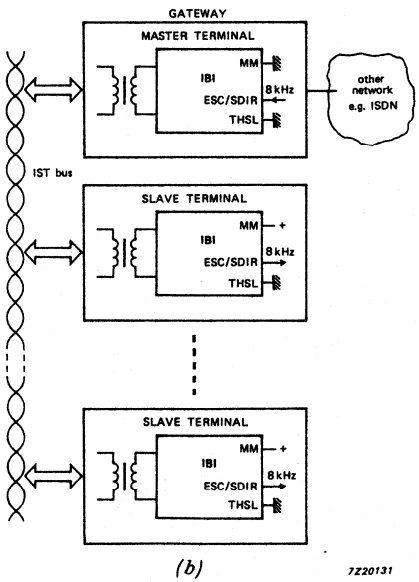


Fig. 4.0-1 IST bus configuration.



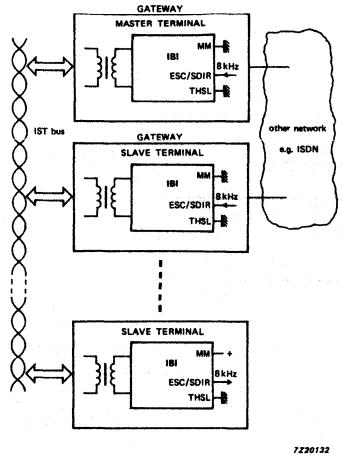
(a)



(b)

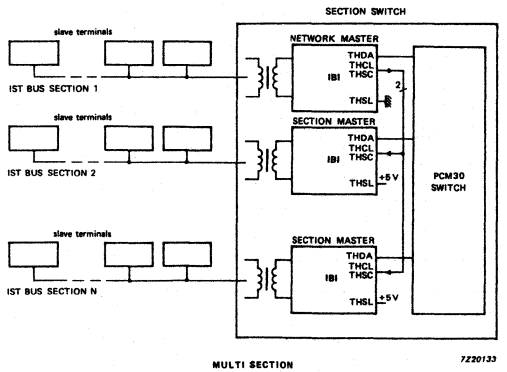
Fig. 4.0-2 IST bus networks: (a) stand alone;
(b) with one gateway/gateway terminal.

DEVELOPMENT DATA



WITH TWO OR MORE GATEWAYS/GATEWAY TERMINALS

(c)



(d)

Fig. 4.0-2 IST bus networks: (c) with two or more gateways/terminals. (d) multi section.

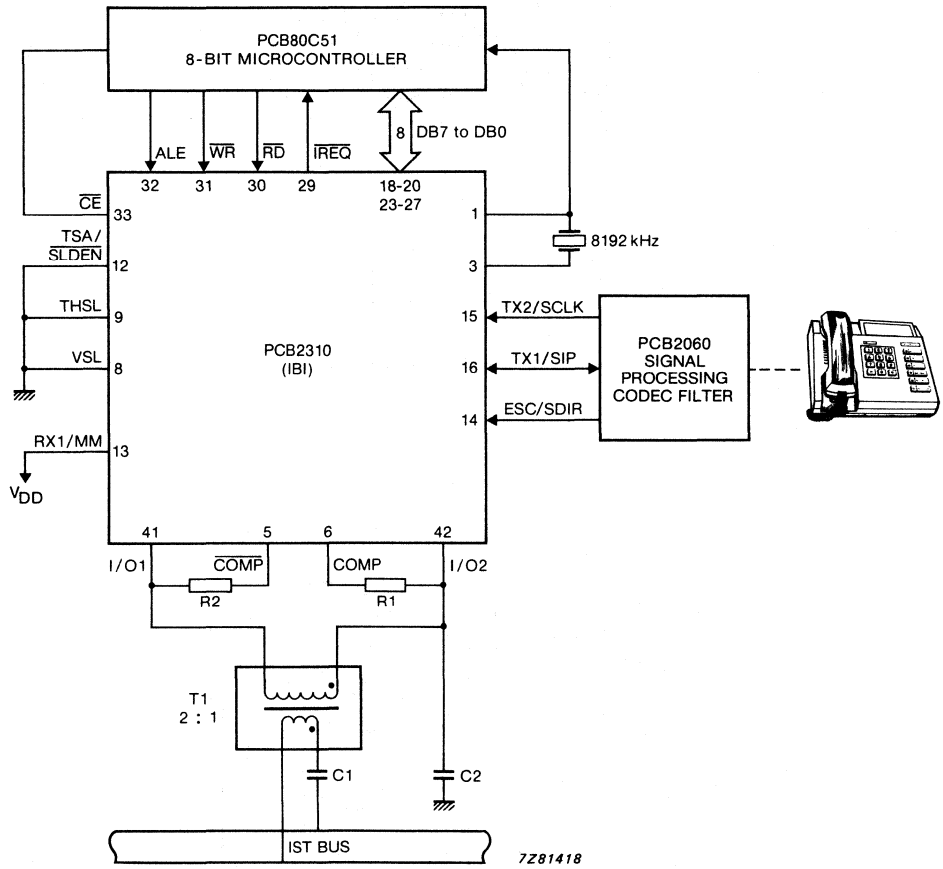


Fig. 4.0-3 Voice terminal: THW normal mode; SLD master mode.

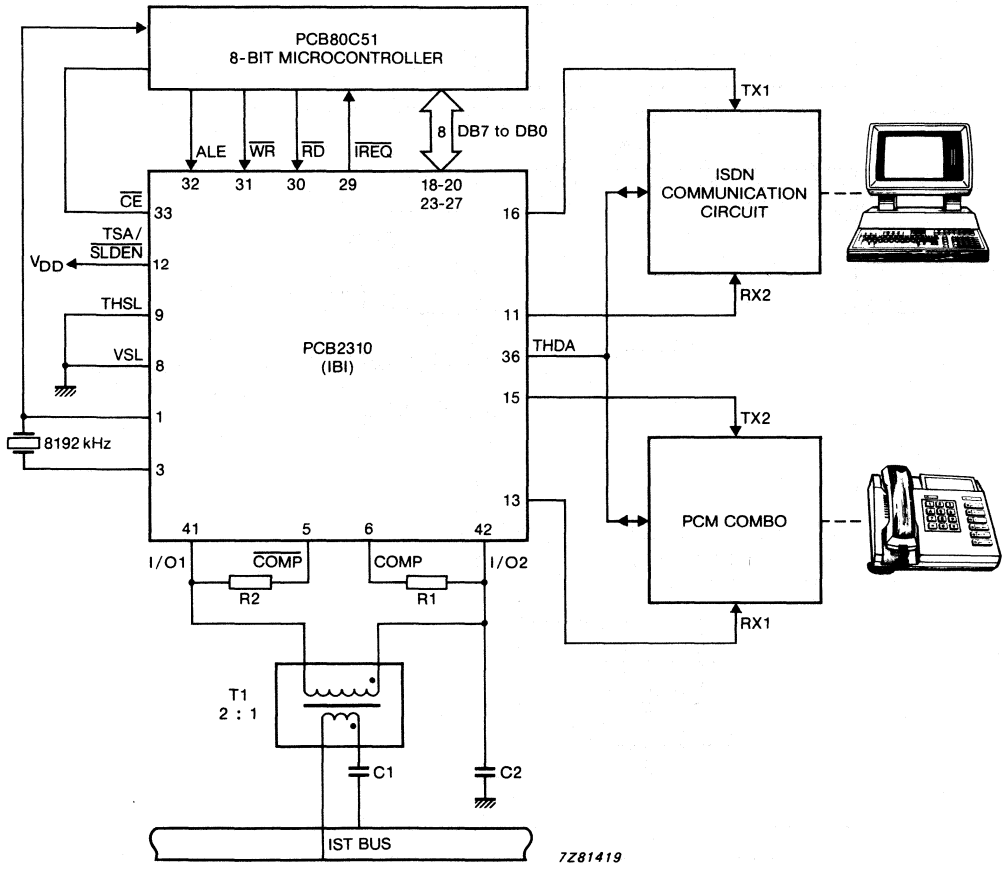


Fig. 4.0-4 Voice/data terminal: THW master mode; TSA mode.

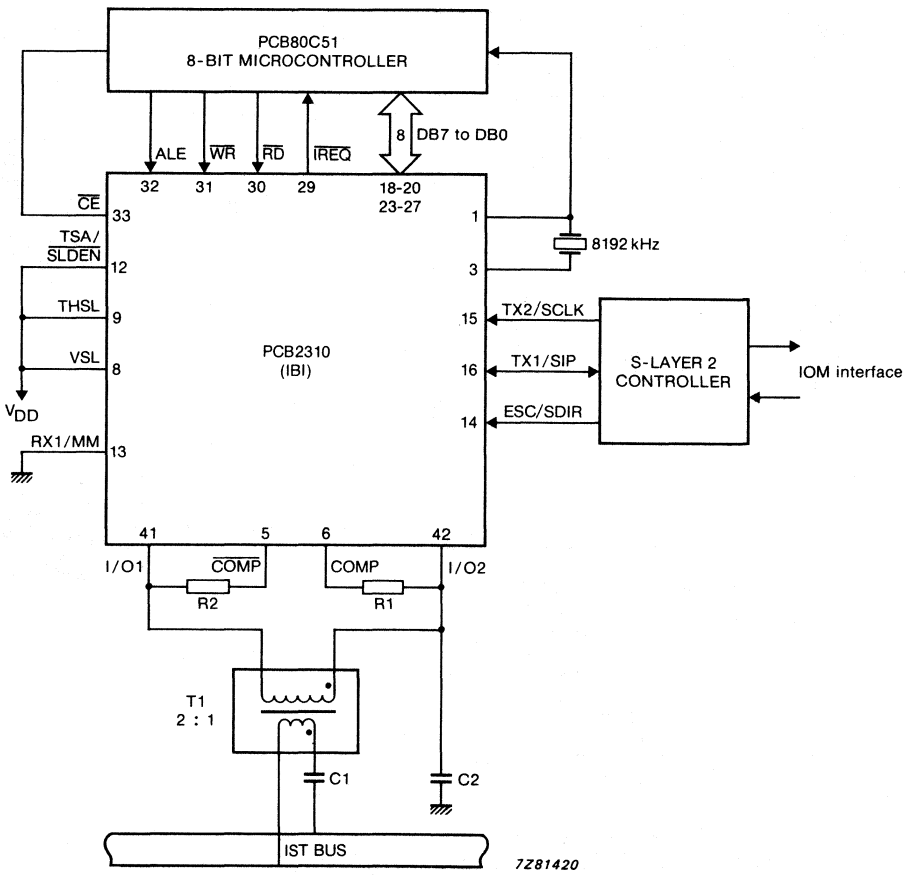


Fig. 4.0-5 IOM interface: THW master mode; SLD slave mode.*

* IOM is a trade mark ISDN-Oriented Modular

DEVELOPMENT DATA

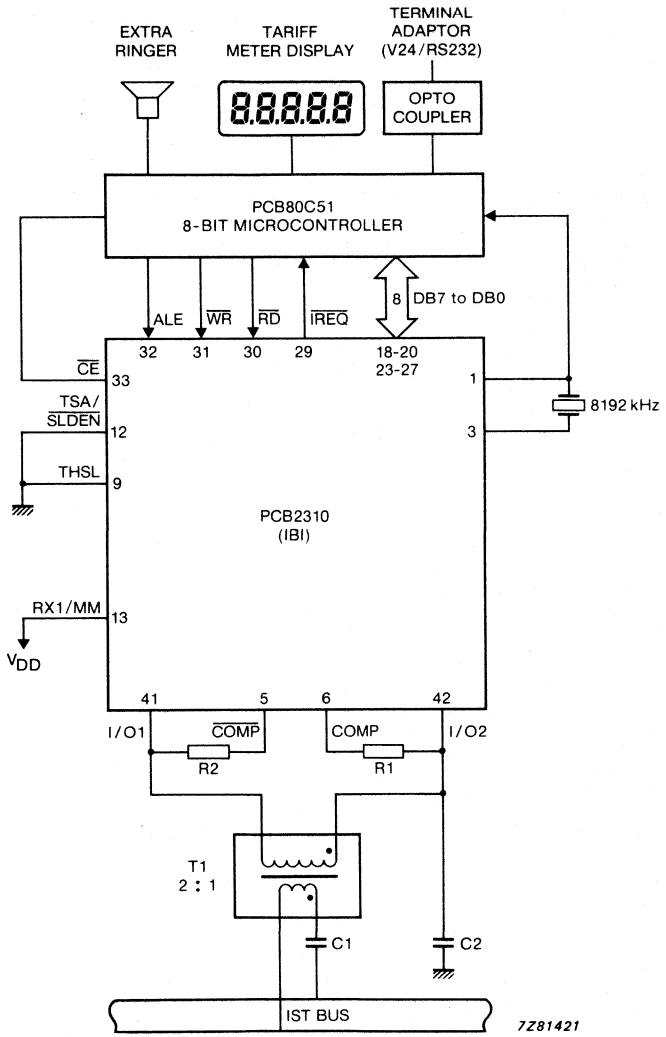


Fig. 4.0-6 Additional application examples.

LTT-4B/3T ECHO CANCELLER

HOW TO USE THIS DATA SHEET

- **Section 1** introduces the LTT-4B/3T echo canceller. The architecture of the circuit is shown with a block diagram. This section also describes the features plus a quick reference to the U- and IOM*-interface. Ordering information is found in this section.
- **Section 2** describes the functioning of the LTT-4B/3T echo canceller and follows the architectural areas established by the block diagram in section 1.
- **Section 3** provides application information.
- **Section 4** gives details of the PCB2390 packaging.

* IOM is a trade Mark. ISDN-Oriented Modular

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1.0 INTRODUCTION

1.1 Features

1.2 Quick reference data

1.3 Ordering information

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2.1.1 Line interface
2.1.2 Signal Processor
2.1.3 Line Frame Formatter/Receiver
2.1.4 IOM Handler
2.1.5 Control Mode

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3.0.2 Timing recovery
3.0.3 Non-linear correction
3.0.4 Signal processor receiver
3.0.5 Interface and components

4.0 PACKAGE OUTLINE

4.1 to be detailed

1.0 INTRODUCTION

The PCB2390 LTT-4B/3T echo canceller is a CMOS integrated circuit intended for Integrated Services Digital Networks (ISDN) transmission system for two 64 kbit/s B-channels (2B) of encoded voice or data plus a 16 kbit/s D-channel (D) of signalling and low-speed data. This data stream for basic access to ISDN must be transferred transparently on the existing 2-wire subscriber line at a rate of 144 kbit/s (full duplex; CCITT U-reference point).

There are four application modes as shown in Fig. 3.0-12:

- Line termination at the exchange end of the line
- Network termination at the subscriber's end of the line
- Repeater mode with installation versus exchange
- Repeater mode with installation versus subscriber

The PCB2390 complies with the U_{k0} specification of the West German administration.
The U_{k0} specification has been defined to guarantee compatibility with equipment made by different manufacturers. The specified loop length capability is based on the West German subscriber cable network which is characterized by large serving areas and thus can be considered internationally as a "worst case". It is defined in terms of two reference loops. The maximum line length is 4,2 km of 0,4 mm wire or 8 km of 0,6 mm wire. However this can be extended to a maximum of 14 km by adding a repeater comprising two additional PCB2390s.

The loop attenuation is related on the capacitance of the cable; the worst situation (an 0,6 mm 47,5 nF/km cable) gives an attenuation of 38 dB at 80 kHz for the specified maximum length of 8 km.

The line code chosen for the U_{k0} interface is a block type 4B/3T, in which 4 binary bits are mapped on 3 ternary symbols, thereby reducing the signalling rate to 108 kbaud. The encoding is applied on scrambled 2B + D data. Together with an 11-symbol frame word and a 1 kbaud maintenance channel the line rate is 120 kbaud.

The U_{k0} interface includes functions for maintenance and activation/de-activation of the transmission link and power feeding of an emergency telephone function at the subscribers premises. These functions are all implemented in the device.

The maintenance functions provide for:

- Switching of test loops at different sites of the link
- Access to a 1 kbit/s service channel
- Indication of transmission errors

Error indication is based on the detection of a violation of the coding rule.

To provide for an ISDN oriented modular (IOM) system architecture, the PCB2390 has a component interface called the IOM-interface. On this interface, the 2B + D channels and control information is interchanged with an S-bus circuit at the subscriber's end of the line, and a layer-2 circuit in the exchange.
The IOM-interface consists of:

- Data line downstream (DD) from exchange
- Data line upstream (DU) to exchange
- 8 kHz frame
- 512 kHz clock

DEVELOPMENT DATA

1.1 Features

- Component for ISDN 144 kbit/s basic access
- Four application modes
- Fulfils the West German U_{k0} interface specification
- 2-wire full duplex transmission system with adaptive echo cancellation and decision feedback equalization
- Digital signal processor for adaptive filters
- Line length up to 8 km; repeater mode for extended line
- Bridged taps handled in subscriber line
- Possibility of remote power feeding
- Supports activation/de-activation procedures
- Switching of test loops and monitoring of transmission errors implemented
- Equipped with standard IOM component interface
- Single 5 V power supply
- Power consumption: 180 mW (active); 6 mW (stand-by)
- 3,84 MHz master clock

1.2 Quick reference data

Table 1.2-1 U-interface

PARAMETER	SPECIFICATION
line code	4B/3T
line rate	120 kbaud
frame length	1 ms
frame word	11 symbols
service channel	1 kbit/s
line length	4,2 km of 0,4 mm cable 8,0 km of 0,6 mm cable
pulse amplitude	2 V (peak value)
termination resistance	150 Ω (nominal)

Table 1.2-2 IOM-interface

PARAMETER	SPECIFICATION
data rate	256 kbit/s
frame length	125 μs
bit clock	512 kHz
inputs/outputs	CMOS: TTL compatible

1.3 Ordering information

TYPE NUMBER	TEMPERATURE RANGE °C	PACKAGE
PCB2390		

DEVELOPMENT DATA

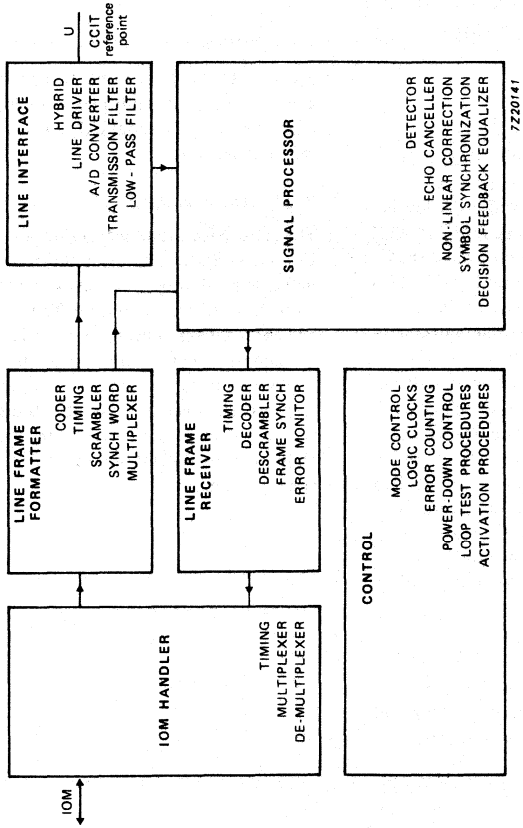

Fig. 1.0-1 Architecture of the LTT-4B/3T Echo Canceller; PCB2390.

2.0 FUNCTIONAL DESCRIPTION

2.1 General description

The architecture of the LTT-4B/3T echo canceller is shown in Fig. 1.0-1. The most important part is the signal processor which is responsible for processing the line signal to determine incoming symbols in the presence of echos. However the other modules are equally essential to form a complete transmission system.

The analogue functions are performed by the subscriber line interface. The digital part is made of modules that perform bit or word oriented operations.

2.1.1 Line Interface

This part contains the circuits for driving the line transformer, a hybrid, a low-pass filter and a 10-bit ADC. An activation signal amplifier detects the activation (wake-up) signal of the U-interface. The third order low-pass filter attenuates the out-of-band interference in the receive path. The transmitted spectrum is limited by a pulse shaping network in the line driver. The A/D converter (ADC) which encodes the complete line signal including echos, has a 10-bit resolution and is made with a two-stroke pipe-lined successive approximation method; by applying conversion in the front-end all signal processing can be implemented in digital technology. This has the advantage that full benefit can be obtained from developments in digital CMOS VLSI. To keep the master clock frequency low, in spite of the substantial amount of signal processing operations that have to be performed, the ADC and signal processor operate on the baud rate. This choice enables the use of a master clock frequency of 3,84 MHz, consistent with low power consumption, but requiring a specific timing extraction method.

2.1.2 Signal Processor

The signal processor operates on a word-wide basis. The various parts are inter-connected by an internal control and data bus. The echo canceller (EC) and decision feedback equalizer (DFE) are implemented in transversal filters. The convergence time for the adaptive system, starting from the initial state, is 100 ms (typ.). The filter coefficients remain stored in the RAM after power-down, thus re-convergence time will be close to zero.

2.1.3 Line Frame Formatter/Receiver

The line frame formatter adjusts the rate, performs 2B + D scrambling and contains the 4B/3T coder. It also multiplexes the 11-digit frame pattern into the ternary stream.
The line frame receiver performs the opposite tasks in the receive direction. It also synchronizes to the incoming line frame and monitors the ternary running digital sum to signal the occurance of detection errors.

2.1.4 IOM Handler

The IOM Handler performs the interface with IOM architecture ICs. It multiplexes, de-multiplexes the data and control part of the serial I/O signals and responds to an initial activation.

2.1.5 Control Module

The control for the activation/de-activation procedure of the U-interface is carried out by the control module. It also implements all procedures associated with mode control, loop tests and error counting. The logic clocks are generated and controlled in power-down mode to save power consumption. Phase control is implemented using a crystal oscillator and a discrete phase stepper. Symbol timing recovery is derived using symbol transitions together with symbol values. The internal timing is slaved to the U-interface or the IOM-interface dependent on the application mode.

3.0 APPLICATION INFORMATION

3.0.1 Design based on line characteristics

The adaptive filters have to be designed carefully in accordance with the waveforms entering the receiver, taking into account the effects of line code, hybrid, filters and wire pair, including bridged taps (if present). The echo signal in the receiver is characterized by the pulse echo as a function of time pe(t), the response on a full T pulse sent by the local transmitter. The path between remote transmitter and local receiver is represented by the pulse response as a function of time pr(t). To account for the effect of the 4B/3T line code, pr(t) and pe(t) should be convolved with the sequence of +1, 0 and −1 symbols generated by the coder. The coding rule allows that the peak amplitude of both echo and inter-symbol interference (isi) is approximated to four times the response tail of a single pulse.

The minimum value of the received signal determines the required suppression of echo and isi. In Fig. 3.0-1 pr(t) is shown as obtained with an 8 km 0,6 mm pair of 47,5 nF/km, a transmitted pulse amplitude of 2 V and a third order low-pass shaping filter in the receiver; the time axis is in symbol intervals (T) at 120 kbaud.

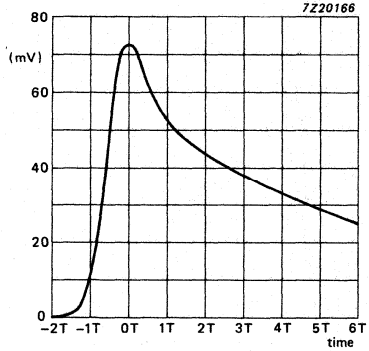

Fig. 3.0-1 Response on a 2 V full T pulse via an 8 km 0,6 mm pair; pr(t).

Fig. 3.0-1 shows that detection errors may occur if an interference peak is above 35 mV. To allow for design and application margins the peak amplitude of residual echo and isi is limited to 10 mV. Curve (a) in Fig. 3.0-2 and Fig. 3.0-3 is the echo response due to a single transmitted pulse; it shows that the required suppression can be achieved with an FIR filter compensating the tails of 35 previously transmitted symbols.

This, however, does not include any effect of a line coupling transformer. If a transformer with a parallel inductance of 100 mH is used on both sides of the connection, curve (b) is obtained, indicating that an adaptive filter with a length > 100 T is required, which is an impractical value. The large pulse tail is caused by the fact that the hybrid balance network does not compensate for the inductance. An effective measure is the use of a high-pass filter in the receive section. A five-tap transversal filter performs the high-pass function: a main tap of +1 and four delayed taps of −1/4. The echo response shown by curve (c) of Fig. 3.0-2 and Fig. 3.0-3 is evidence that an echo canceller with a length of 30 T meets the 10 mV target.

The effect obtained from the high-pass filter is also suitable for the DFE.

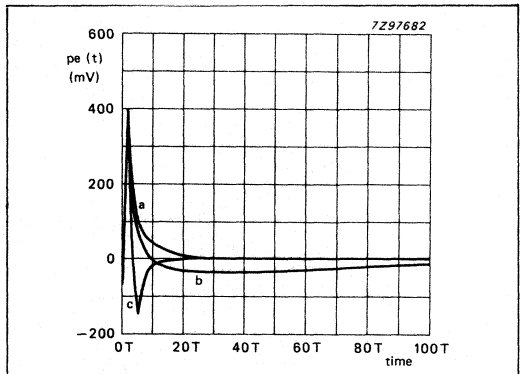

Fig. 3.0-2 Response of the echo path on a 2 V full T pulse; pe(t):
(a) effect of mismatch between pair and hybrid balance network;
(b) including the effect of the line transformer;
(c) tail reduction obtained with high-pass filter.

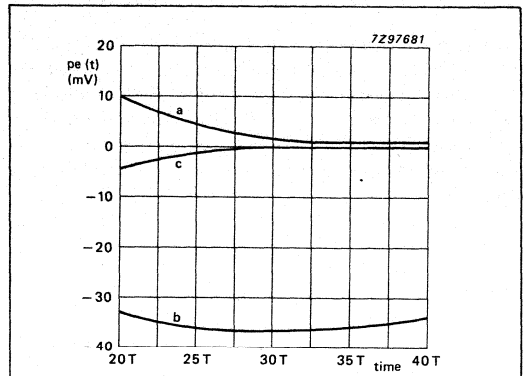

Fig. 3.0-3 Response of the echo path on a 2 V full T pulse pe(t) zoomed in at a range between 20 and 40 symbol intervals after the pulse was transmitted:
(a) effect of mismatch between pair and hybrid balance network;
(b) including the effect of the line transformer;
(c) tail reduction obtained with high-pass filter.

In Fig. 3.0-4 the path between remote transmitter and local receiver (pr(t)) is shown for the same three conditions (a), (b) and (c) as in Fig. 3.0-2. Curve (c) shows that by using a high-pass filter the DFE has to compensate the tails of the previous 20 symbols. The complexity reduction obtained with a high-pass section is significant, but the penalty is a slight increase in the noise signal at the detector. The overall effect is negligible because less and smaller DFE coefficients are required leading to lower error multiplication.

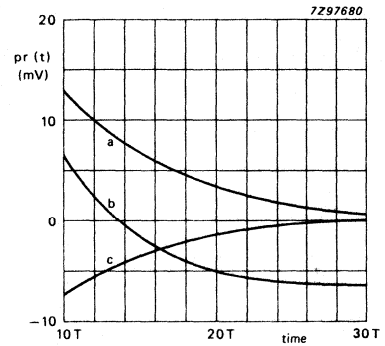

Fig. 3.0-4 Response on pulse from remote transmitter; pr(t):
(a) effect of mismatch between pair and hybrid balance network;
(b) including the effect of the line transformer;
(c) tail reduction obtained with high-pass filter.

Although not part of the West German U_{k0} specification the adaptive filters can handle loops containing bridged taps. Fig. 3.0-5 shows the echo response of 8 km loop with and without a 1 km bridged tap 200 metres from the system. This shows that only a short term influence can be accommodated to give the echo canceller sufficient dynamic range.

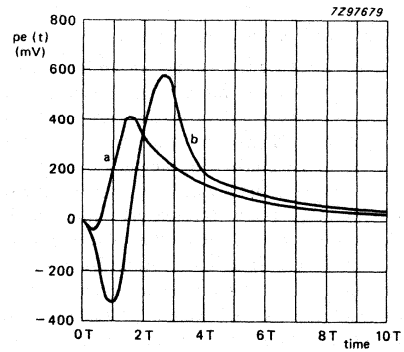

Fig. 3.0-5 Influence on the echo response of a 1 km bridged tap 200 metres from the system:
(a) without bridged tap; (b) with bridged tap.

A more significant influence can be observed in the received signal (see Fig. 3.0-6). Thus for a given level of external interference (cross-talk and impulse noise) bridged taps can only be accommodated if the loop length is reduced.

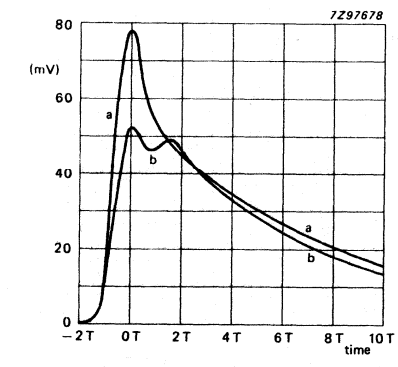

Fig. 3.0-6 Influence on the received signal of a 1 km bridged tap 1 km from the system:
(a) without bridged tap; (b) with bridged tap.

3.0.2 Timing recovery

The timing recovery has to extract phase information from the sampled data representation of a received signal which suffers from linear but unpredictable distortion due to the loop characteristics.

The timing control information is derived on-line by matching the phase on each received mark (+1, −1). This ensures stable phase locking independent of Frame formats.

In the PCB2390 the correlation method is applied where the rising edge of the response to a received symbol is used to derive the phase control. A combined timing control and precursor compensation is shown in Fig. 3.0-7. The precursor is compensated behind the ADC by a two-tap FIR filter with fixed coefficients −1/8 and +1. If the sampling phase is misaligned, the sampled precursor does not match the compensation and the timing will be shifted until optimum compensation is achieved.

3.0.3 Non-linear compensation

Non-linearities in the analogue circuitry of the transmitter and receiver are responsible for signal components that cannot be compensated with adaptive filters based on simple transversal structures. The distortion consists of transmitter unbalance and receiver non-linearity. The unbalance in the transmitter is compensated by associating a separate transversal filter coefficient with each signal level (see Fig. 3.0-8):

- One coefficient Ci for "+" and "−" symbols
- A separate coefficient Zi for "0" symbols

Zi only handles the range of the unbalance and can be left out completely for taps that are too small to contribute to the unbalance. The range chosen for Zi is 5% and the "zero canceller" has a length of 14 symbol intervals.

DEVELOPMENT DATA

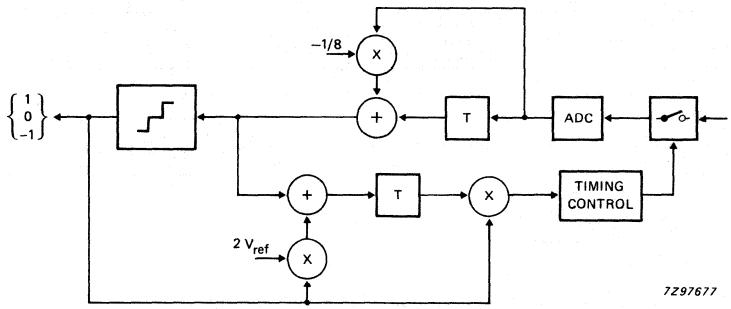

Fig. 3.0-7 Combined timing control and precursor compensation.

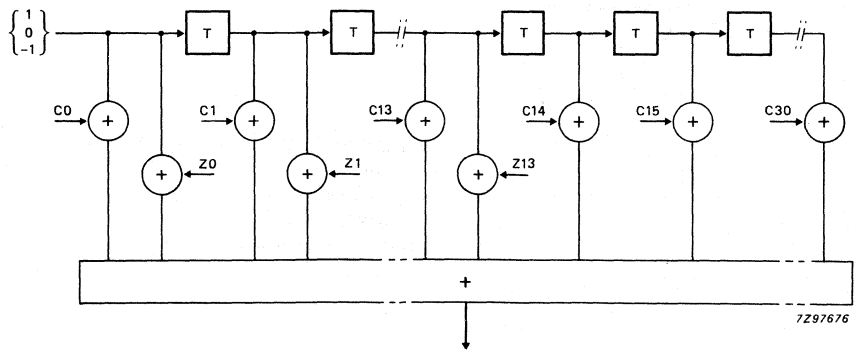

Fig. 3.0-8 Adaptive cancellation of transmitter unbalance.

The receiver non-linearity caused by the ADC is compensated before the ADC (see Fig. 3.0-9) with a value retrieved from a table which is addressed with the most significant bits (MSB) of the output signal of the ADC. Each entry in the table is adapted automatically so that its value compensates the average non-linearity error for the segment it represents. The table has 32 entries, sufficient to handle a 5% differential non-linearity in the ADC.

3.0.4 Signal processor receiver (see Fig. 3.0-9)

The receiver non-linearity is compensated after analogue-to-digital conversion (see section 3.0.3). Subsequently the linearized sample is filtered by a transversal high-pass filter with coefficients $-1/8$, 1, $-1/4$, $-1/4$, $-1/4$, $-1/8$ forming the cascade of the tail reduction function and the precursor compensation. The inter-symbol and echo replica are subtracted from the filtered signal.

An adaptive reference signal which is controlled to half the amplitude of the received signal is formed. It is used as a detection threshold. The control signal for updating the adaptive systems is the next signal after all linear corrections are performed and the symbol value itself is subtracted from it.

The dynamic behaviour of the adaptive processes is shown in Fig. 3.0-10. In the curve (a) the total misalignment of all adaptive filters is shown, starting with a random content for all coefficients. The system converges in approximately 100 ms, without using any specific training sequence. Included is the concurrent acquisition of the timing phase. It is shown in the system "exchange mode", which is the most difficult because an adaptation in the timing phase immediately de-converges the echo canceller again.

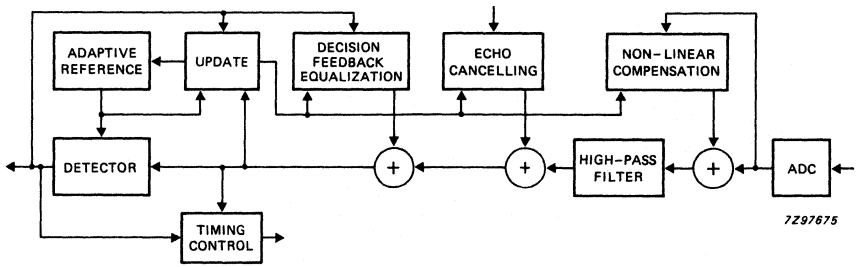

Fig. 3.0-9 Functional structure of the signal processor receiver.

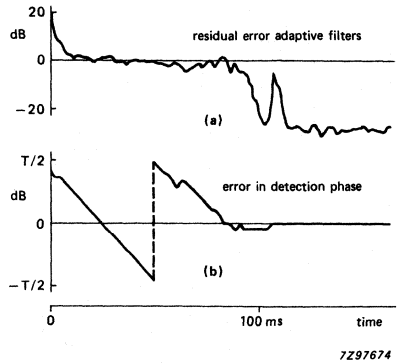

Fig. 3.0-10 Convergence behaviour of the adaptive systems:
(a) sum of amplitude errors with respect to received signal;
(b) timing phase with respect to optimum.

The architecture of the signal processor receiver does not quite resemble its functional structure. It is optimized to obtain maximum design flexibility and compromises between a low master clock frequency and minimum silicon area. The implemented structure is shown in Fig. 3.0-11. The signal processor receiver contains several autonomous units which operate concurrently. Each slave unit has its own microprogram that is slaved to a central timing reference.

Each microprogram performs 32 instructions per symbol interval. The DFE and EC are realized in two separate convolution units; since the DFE resembles the EC they can share the control unit and adaptation register.
Both filters have a pipe-lined internal structure to realize the adaptation and accumulation of 30 coefficients.
Coefficients and data vectors are stored in static RAMs.

The main processing of the digital signal sample occurs in the Arithmetic Logic Unit (ALU).
The ALU performs:

- Non-linearity compensation
- High-pass filtering
- Subtraction of echo and inter-symbol replica
- Timing acquisition
- Adaptation of the reference level
- Adaptation of the non-linearity canceller
- Symbol detection

The ALU uses a microprogrammed register bank for storage of intermediate results. The intermediate results are transferred over a 14-bit wide data bus.

All digital processing has additional 2-bit resolution; as a result a 12 dB higher loop loss can be accommodated provided that the ADC is also extended by two bits.

DEVELOPMENT DATA

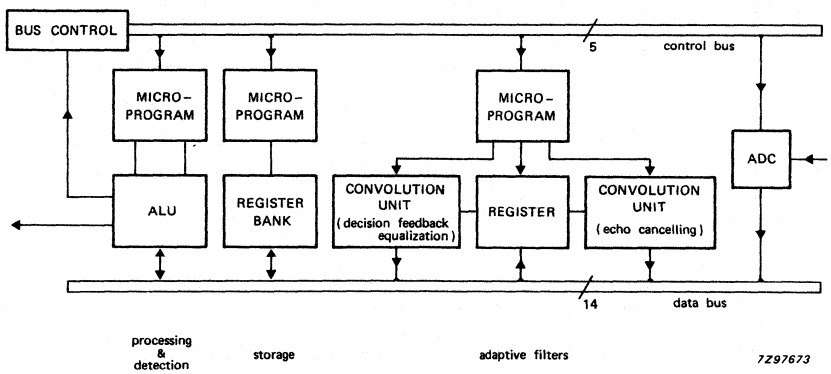

Fig. 3.0-11 Architecture of the signal processor receiver.

3.0.3 Interfaces and components

The functions that implement layer of 1 of the ISDN basic access have been mapped on components in a way that the present uncertainty with respect to the international U-interface definition does not penetrate deeply into system products. A component interface that supports all functions defined by the basic access is the IOM-interface. Measures have been taken to achieve compatibility with equivalent interfaces by other manufacturers.
In Fig. 3.0-12 the component configuration is shown with LTT-4B/3T echo canceller in its various applications.

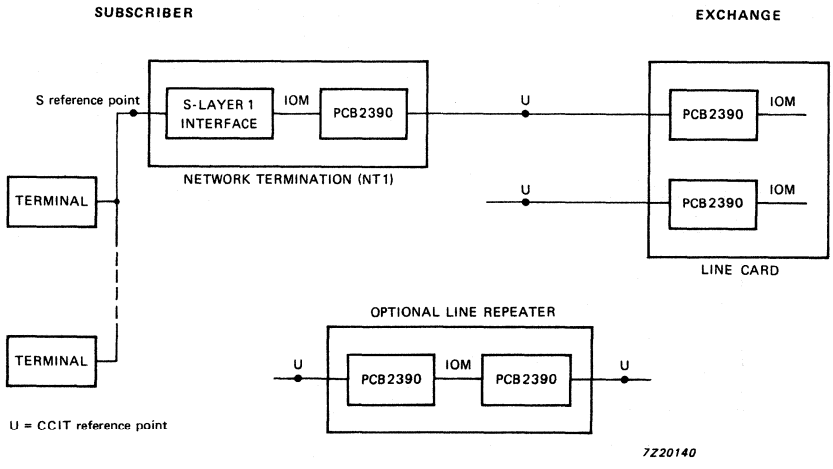

Fig. 3.0-12 Application modes: layer 2 components for the ISDN basic access.

SINGLE-CHIP DIGITAL SIGNAL PROCESSOR

HOW TO USE THIS DATA SHEET

- **Section 1** contains ordering information and the main features of the PCB5010 and PCB5011.
- **Section 2** describes the signals of the PCB5010 and PCB5011, with block diagrams and full descriptions of what functions can be performed by each block.
- **Section 3** describes how the blocks are controlled by the instructions given by the programmer. This section is used during programming, it assumes however, a full knowledge of section 2.0. Programming can be simplified by using the software tools available.
- **Section 4** describes all the electrical characteristics. This section is used during the design of system hardware.
- **Section 5** gives details of the PCB5010 and PCB5011 packages.

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APPENDIX A: INSTRUCTION SUMMARY (see centre pages)

1.0 INTRODUCTION

The PCB5010 and PCB5011 are part of our SP 50 family of digital signal processors that contains devices for various applications. These CMOS devices have a common processor structure and are accompanied by a common set of development tools.

The processor structure is characterized by a double data bus, a two operand hardware multiply/accumulate unit and a two operand ALU to improve throughput. Powerful parallel and serial interfaces enable communication with external devices. Large on-chip data memories, each with its own programmable address computation unit (ACU), offer the possibility to make systems with only a few components.

The PCB5010 and PCB5011 are the optimal solutions for implementing DSP functions in telecommunications, and can also be used to advantage in speech processing, high-speed control, image processing and many other fields.

- PCB 5010: Version with on-chip ROM (mask programmable)
- PCB 5011: ROMless bond-out version, for use with external program/data memory

DEVELOPMENT DATA

ORDERING INFORMATION

order number	speed (MHz)	operating ambient temperature (°C)	package
PCB5010WP-8	8	0 to +70	68-pin PLCC
PCF5010WP-8*	8	−40 to +85	68-pin PLCC
PCB5011YC-8	8	0 to +70	144 PGA
PCF5011YC-8*	8	−40 to +85	144 PGA

* The PCF versions will be identical to the PCB versions except that they have an extended operating ambient temperature range. However, minor variations may occur in the AC characteristics.

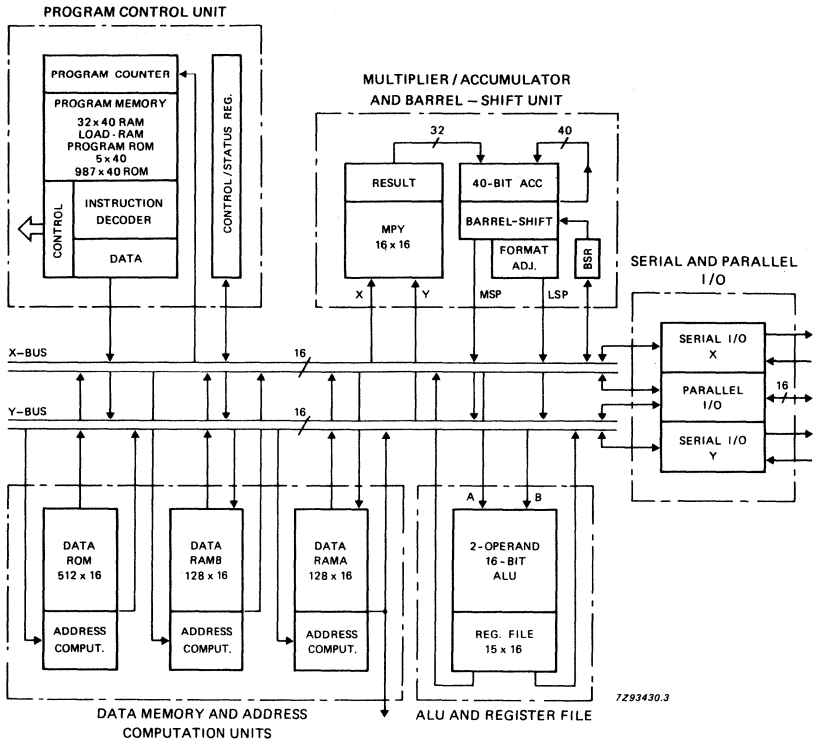


Fig. 1.0-1 Simplified block diagram of the PCB5010.

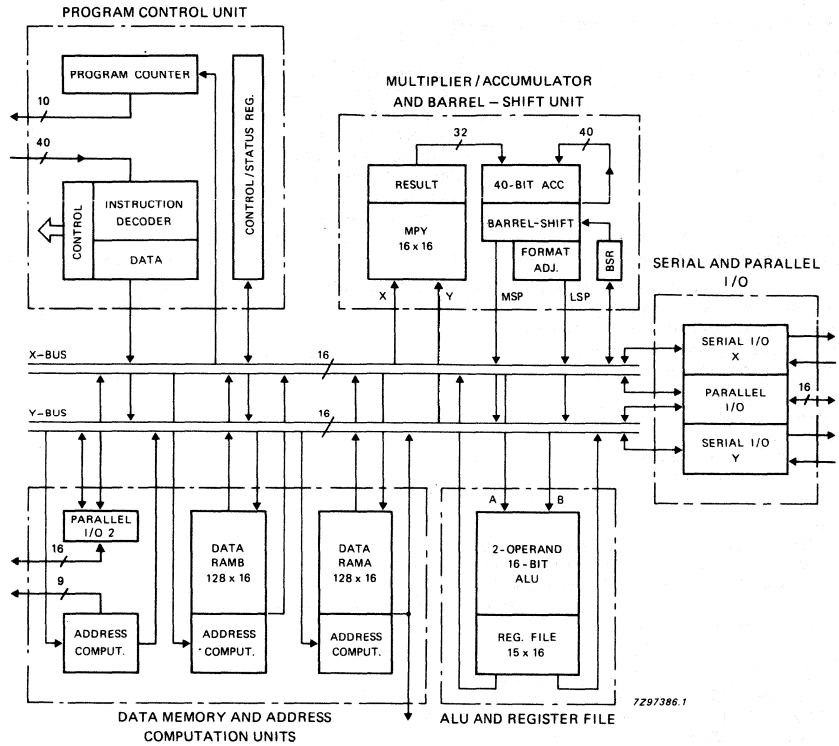


Fig. 1.0-2 Simplified block diagram of the PCB5011.

FEATURES

- Harvard architecture with two data buses of 16 bit width
- 4 instruction types:
  - multiply/accumulate operation + 2 data moves + 3 address calculations/memory read accesses
  - alu operation + 2 data moves + 3 address calculations/memory read accesses
  - load immediate data + 3 address calculations/memory read accesses
  - branch + 3 address calculations/memory read accesses

  Note: a high degree of parallel processing allows up to 6 basic operations to be performed simultaneously.
- Hardware two's complement 16 x 16 multiplier with 40-bit accumulator, full range barrel-shifter and format adjuster:
  - 45 different multiply/accumulate operations
  - multi-precision multiplication support
  - result bit-reversal possibility
  - 4 status flags
- 16-bit 2-operand ALU with:
  - 31 different operations
  - multi-precision operation support
  - 15 x 16-bit 3-port register-file
  - 5 status flags
- Program memory:
  PCB5010: 987 x 40-bit on-chip ROM (mask programmable)
  32 x 40-bit on-chip RAM (loaded via the X-bus)
  5 x 40-bit on-chip ROM (fixed load RAM program)
  PCB5011: 1024 x 40-bit external memory (or 64K x 40-bit when some external logic is added)
- Data memory:
  PCB5010: 512 x 16 bit on-chip ROM (mask programmable)
  2 x (128 x 16) on-chip static RAM
  PCB5011: 512 x 16 bit external memory (read and write possible)
  2 x (128 x 16) on-chip static RAM
- 3 powerful programmable address computation units (ACU's) for the data ROM and both data RAMs and also for 16 pages of 4096 x 16 bit external data memory
  - each ACU has 8 different operations
  - 1 status flag for each ACU
- 5 level deep hardware stack (software extendable)
- 16-bit parallel I/O to access external data memory
  - 8 million words/s
  - WAIT facility so that "slow" peripherals can be connected
- 2 independent serial inputs and outputs (one pair for each data bus), with a maximum speed of 4 million bit/s under the control of external clocks
- 4 user input flags
- Maskable interrupt
- Repeat possibility of single instruction
- Maximum clock rate 8 MHz
- Pipelined (P) and Non-pipelined (NP) modes under programmer control:
  P-mode: a new instruction can start every 125 ns
  NP-mode: a new instruction can start every 250 ns
- Single 5 V power supply (±5%)
- All I/O are TTL compatible
- Operating ambient temperature range:
  PCB5010/11: 0 to +70 °C
  PCF5010/11: −40 to +85 °C

2.0 FUNCTIONAL DESCRIPTION

2.1 GENERAL DESCRIPTION

The detailed block diagram of the PCB5010 and PCB5011 are shown in Fig. 2.1-1 and Fig. 2.1-2. The signals of the processors are described briefly in the table below.

SIGNAL DESCRIPTION

SIGNAL	DESCRIPTION
V_{DD}	Supply voltage: 5V ±5%
V_{SS}	Ground
CLK	Clock (input)
$\overline{RST}$	Reset (input)
D15 . . . D0	16-bit wide parallel I/O port (input/output)
A15 . . . A0	16-bit wide address for 64K-words in external data memory (output)
R/$\overline{W}$	Read/write signal for control of external memory (output)
$\overline{DS}$	Data strobe (output)
$\overline{WAIT}$	Wait signal for synchronization of parallel I/O (input)
DIX	Serial data input (input) for the X-bus
$\overline{SIXEN}$	Serial data enable (input) for the X-bus
$\overline{SIXRQ}$	Serial input request (output) for the X-bus
CIX	Serial input clock (input) for the X-bus
DIY	Serial data input (input) for the Y-bus
$\overline{SIYEN}$	Serial input enable (input) for the Y-bus
$\overline{SIYRQ}$	Serial input request (output) for the Y-bus
CIY	Serial input clock (input) for the Y-bus
DOX	Serial data output (output) for the X-bus
$\overline{SOXEN}$	Serial output enable (input) for the X-bus
$\overline{SOXRQ}$	Serial output request (output) for the X-bus
COX	Serial output clock (input) for the X-bus
DOY	Serial data output (output) for the Y-bus
$\overline{SOYEN}$	Serial output enable (input) for the Y-bus
$\overline{SOYRQ}$	Serial output request (output) for the Y-bus
COY	Serial output clock (input) for the Y-bus
$\overline{INT}$	Maskable interrupt (input)
$\overline{IACK}$	Interrupt acknowledge (output)
SYNC	Synchronization signal; indicates where execution of a new instruction starts (output)
IFA	User flag (input)
IFB	User flag (input)
IFC	User flag (input)
IFD	User flag (input)

(continued on next page)

SIGNAL DESCRIPTION (Cont'd)

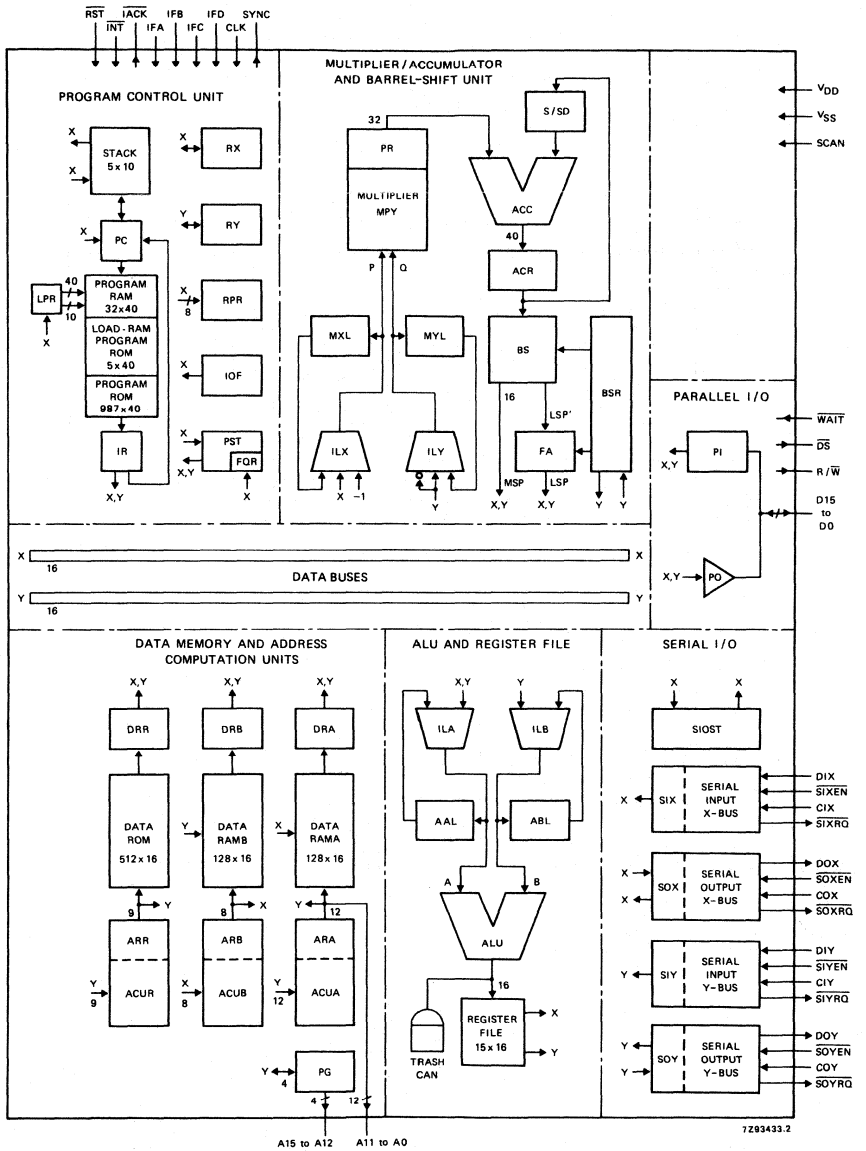
SIGNAL	DESCRIPTION
PCB5011 only:	
PA9 . . . PA0	External program memory address (output)
PD39 . . . PD0	External program word (input)
ARR8 . . . ARR0	9-bit address for 512 words in external data memory (output)
RD15 . . . RD0	Second 16-bit parallel I/O port (input/output)
$\overline{RR}/W$	Read/write signal for second 16-bit parallel I/O port (output)
$\overline{RDS}$	Data strobe for second 16-bit parallel I/O port (output)

The main blocks of PCB5010/11 are:

- Program control unit with:
  - Program ROM (only for PCB5010)
  - IR (instruction register)
  - Sync pin
  - PC (program counter)
  - RPR (instruction repeat register)
  - Stack
  - PST (processor status register)
  - IOF (input/output status and user flag register)
  - User flag pins
  - $\overline{INT}$ pin and $\overline{IACK}$ pin
  - Bus-save registers RX and RY
  - $\overline{RST}$ pin
  - External program memory port (only PCB5011)
  - External program memory address port (only PCB5011)
- Data memory and address computation units with:
  - RAMA, ACUA (address computation unit A), DRA (data register A)
  - PG (page register)
  - RAMB, ACUB (address computation unit B), DRB (data register B)
  - ROM (only PCB5010), ACUR (address computation unit R), DRR (data register R)
  - External data word pins (only PCB5011)
  - External data memory address pins (only PCB5011)
- Multiplier/accumulator and barrel-shift unit with:
  - Input selectors ILX and ILY
  - Latches MXL and MYL
  - MPY (multiplier)
  - Accumulator with ACC (adder), ACR (multiplication/accumulation register) and S/SD (sign/scale-down block)
  - BS (barrelshifter)
  - FA (format adjuster)
  - BSR (barrelshift and format adjust control register)
- ALU and register file with:
  - Input selectors ILA and ILB
  - Latches AAL and ABL
  - ALU (arithmetic logic unit)
  - R1-R15 (register file)
  - Trash can
- Parallel I/O with:
  - PI (parallel data input latch)
  - PO (parallel data output buffer)
  - Parallel I/O data and control pins
- Serial I/O with:
  - SIX (serial input latch connected to X bus)
  - SOX (serial output latch connected to X bus)
  - SIY (serial input latch connected to Y bus)
  - SOY (serial output latch connected to Y bus)
  - SIOST (serial I/O control register)
  - Serial I/O data and control pins
- Data buses with:
  - 16 bits X-bus
  - 16 bits Y-bus

The working of the main blocks is described in the following sections. The instruction set is described in the section 3.0.

DEVELOPMENT DATA

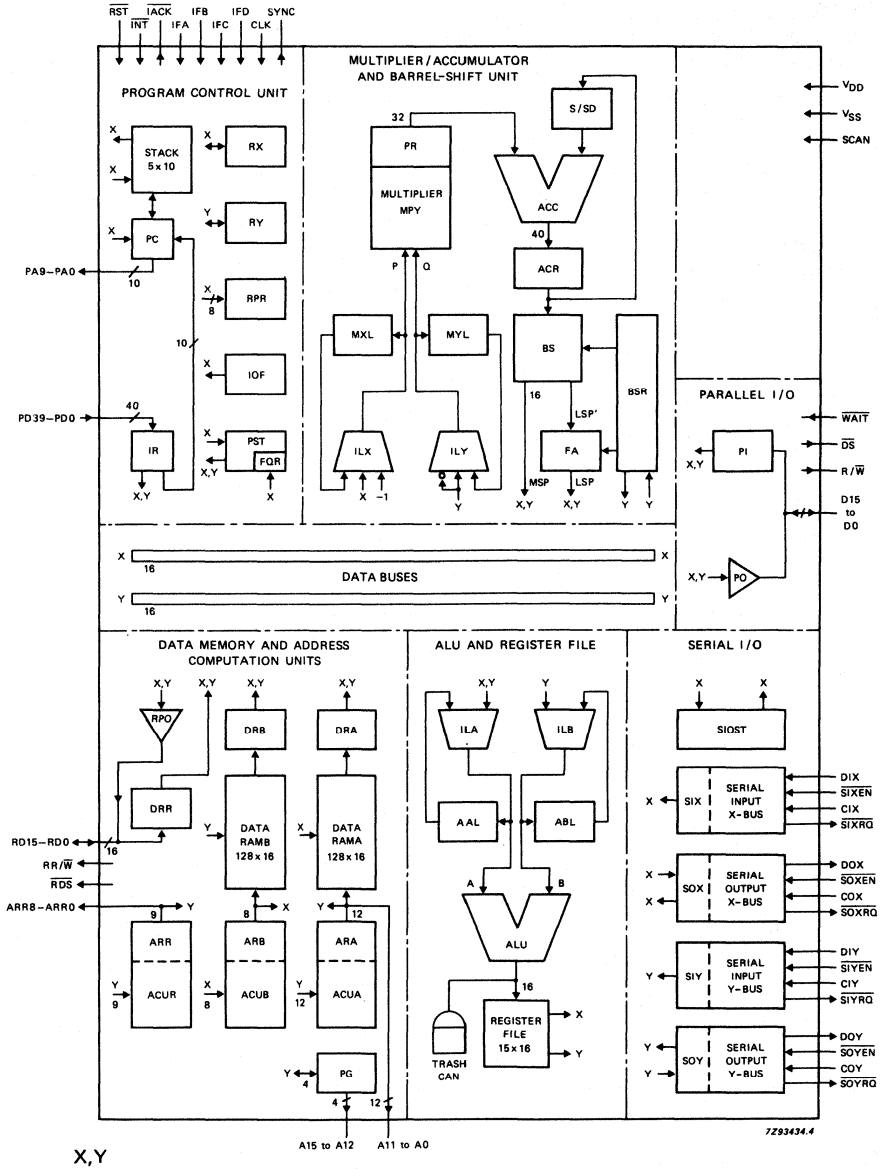


X,Y

Note 1: ↑ means connected to the X-bus/Y-bus.

Note 2: all data paths are 16 bits wide unless indicated otherwise.

Fig. 2.1-1 Detailed block diagram of the PCB5010.



Note 1: ↑ means connected to the X-bus/Y-bus.
Note 2: all data paths are 16 bits wide unless indicated otherwise.

Fig. 2.1-2 Detailed block diagram of the PCB5011.

2.2 PROGRAM CONTROL UNIT

2.2.1 Program memory

The PCB5011 has no on-chip program memory but you can connect external program memory. To access the external program memory, there are 40 program data pins (PD39-PD0) and 10 program address pins (PA9-PA0). The on-chip 10-bit program counter contents are available via these address pins.

The PCB5010 has 1K x 40-bit on-chip program memory:

- 987 x 40-bit mask programmable ROM (address 0-986)
- 32 x 40-bit static RAM (address 992-1023)
- 5 x 40-bit "load RAM" program in ROM (address 987-991)

The memory is addressed by the 10-bit on-chip program counter. The static RAM of the program memory can be loaded via the X-bus by MOVE or LOAD IMMEDIATE operations, following the procedure described in the section 2.2.2 "Load program RAM circuitry".

The "load RAM" program stored in the ROM can be used to load the RAM instructions from an external data memory. This program's code, and its equivalent expressed in the PCB5010/11 assembly language is given in Fig. 2.2.1-1.

Instruction code (hex)

```
987: CFFFE14140
988: 4014120040
989: 4014160040
990: 40140A0040
991: 4000000000
```

Code per instruction field (hex)

```
OP=3 DATA=0FFFF                    DX=0  DY=A  R=0  ACA=5 ACR=0 ACB=0
OP=1     MI=000    SX=05 SY=00     DX=9  DY=0  R=0  ACA=1 ACR=0 ACB=0
OP=1     MI=000    SX=05 SY=00     DX=7  DY=0  R=0  ACA=1 ACR=0 ACB=0
OP=1     MI=000    SX=05 SY=00     DX=5  DY=0  R=0  ACA=1 ACR=0 ACB=0
OP=1     MI=000    SX=00 SY=00     DX=0  DY=0  R=0  ACA=0 ACR=0 ACB=0
```

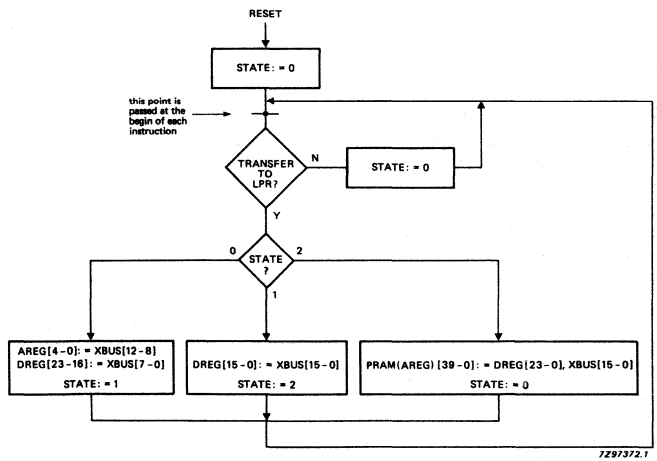
Assembler program

```
ACU (RAMA, M) : = –1                    ;
          RPR : = PI      AC (RAMA, INCA);
         PRAM : = PI      AC (RAMA, INCA);
           PC : = PI      AC (RAMA, INCA);
```

Fig. 2.2.1-1 "Load RAM" program.

2.2.2 Load program RAM circuitry (LPR)

LPR enables the programmer to load the 32 x 40-bit program RAM. To load each 40-bit instruction, three 16-bit words must be transferred to LPR via the X-bus, using MOVE or LOAD IMMEDIATE operations. LPR contains a 5-bit address register (AREG) in which the load address (range 0-31) is loaded and it contains a 24-bit data register (DREG) in which the instruction word is assembled. The loading procedure is shown in Fig. 2.2.2-1.



AREG = address register
DREG = data register
PRAM(i) = position i in the program RAM
[m – n]= bit m to bit n

Fig. 2.2.2-1 Program RAM loading procedure.

2.2.3 Program counter (PC) and mode circuitry (P and NP-mode)

The 10-bit program counter in the PCB5010 and PCB5011 is automatically incremented every instruction cycle during sequential program flow.

There are however, certain situations when the program counter is not incremented but updated differently:
- reset (see section 2.2.10)
- interrupt (see section 2.2.9)
- instruction repetition (see section 2.2.6)
- branch operations (see section 2.2.7)
- loading PC via the X-bus by means of a MOVE or LOAD IMMEDIATE operation (the 10 least significant bits of the X-bus data are loaded)

The processors work in two different modes:
1. Pipelined mode (P):
   instruction cycle = one clock cycle
2. Non-pipelined mode (NP):
   instruction cycle = two clock cycles

When the processor works in the P-mode, the result of a basic operation (see section 3.1 on instruction set) is not always available after the first instruction cycle but sometimes one clock cycle later. Since the processor uses pipelining, a new operation can start before the result of the previous operation is available. When the processor operates in NP-mode, the result of a basic operation is always available at the end of an instruction cycle. On reset, the processor is placed in the P-mode. Mode switching is possible under program control by setting and resetting the FQR bit in the PST register using a MOVE or LOAD IMMEDIATE operation. The instruction after the one that caused the change in the FQR bit is executed in the new mode. Return from interrupt and return from subroutine should be done in the mode in which it was entered.

2.2.4 Instruction register (IR)

In every instruction cycle (i.e. every clock cycle when working in the P-mode and every two clock cycles when working in the NP-mode) an instruction word is fetched from the program memory. The program memory access and storing of the result in the instruction register (IR) takes one clock cycle. During the next clock cycle, the new contents of the IR is decoded and the processor controlled accordingly.

2.2.5 Stack

When an interrupt or subroutine call occurs, the value of PC (in the P-mode) or the value of PC+1 (in the NP-mode) is placed on the stack. The stack is a 5 x 10-bit LIFO register file that allows automatic nesting up to five levels of subroutines and/or interrupts. The top of the stack containing the most recent PC value can be accessed via the data buses. This enables the programmer to extend the stack in the data memory.

2.2.6 Instruction repeat circuitry (RPR)

RPR is an 8-bit register that can be loaded via the X-bus by a MOVE or LOAD IMMEDIATE operation. Only the 8 LSBs on the bus (representing a number N between 0 and 255) are loaded. The instruction after the one in which these 8 bits are loaded is then executed N times as long as $2 \leqslant N \leqslant 255$. The execution count is undefined when $0 \leqslant N < 2$. The execution count is also undefined when the instruction to be repeated is to load RPR or the PC, or is to change the FQR bit in the PST register.

2.2.7 Branch circuitry

The PCB5010 and PCB5011 make it possible to depart from the sequential program flow under software control. There are 4 branch types, and each branch can depend on any one of 50 different conditions.

The 4 branch types are:

- go to
- subroutine call
- return from subroutine
- return from interrupt.

The 50 branch conditions are the true and false status of the following flags or combination of flags:
- ALU flags: Z, N, C, $\overline{\text{C.OR.Z}}$, V, VL, {N.XOR.V}.OR.Z, $\overline{\text{N.XOR.V}}$
- Accumulator flags: SGNM, OVFL
- Barrel-shifter flags: OOR, OORL
- ALU and barrel-shifter flags: OORL.OR.VL
- ACU flags: ACA, ACB, ACR
- User flags: IFA, IFB, IFC, IFD, IFA.AND.IFB.AND.IFC.AND.IFD
- Serial I/O flags: SIXACK, SIYACK, SOXACK, SOYACK

2.2.8 The PST and IOF registers (PST, IOF, IFA – IFD pins)

PST and IOF are 16-bit registers that contain all the flags. Furthermore, PST also contains a bit (EI) that indicates whether the interrupt is enabled or not (enabled = 1; disabled = 0), a bit (FQR) indicating which mode (P = 0 or NP = 1) the processor is working in, and two bits (PIO1 and PIO2) determining the input criteria for the parallel input. The meaning of each bit of PST and IOF is given below:

bit	PST register		IOF register	
00	OVFL	(accumulator flag)	SIXACK	(serial I/O flag)
01	OORL	(barrel-shifter flag)	SOXACK	(serial I/O flag)
02	VL	(ALU flag)	SIYACK	(serial I/O flag)
03	V	(ALU flag)	SOYACK	(serial I/O flag)
04	C	(ALU flag)	IFA	(user flag)
05	Z	(ALU flag)	IFB	(user flag)
06	N	(ALU flag)	IFC	(user flag)
07	OOR	(barrel-shifter flag)	IFD	(user flag)
08	SGNM	(accumulator flag)	reserved	
09	ACA	(ACU flag)	reserved	
10	ACB	(ACU flag)	reserved	
11	ACR	(ACU flag)	reserved	
12	PIO2	(parallel I/O flag)	reserved	
13	PIO1	(parallel I/O flag)	reserved	
14	EI	(interrupt enable/disable)	reserved	
15	FQR	(operation mode)	reserved	

The flags in PST and IOF reflect the status of the functional units to which they belong and they are updated during each relevant instruction. The flags IFA, IFB, IFC and IFD reflect the signal level on their respective input pins. "Lock" type flags (OVFL, OORL and VL) can only be changed from 0 to 1 by the functional units to which they belong. The programmer can overrule the functional units updating the flags in the PST register: the PST register can be overwritten using a MOVE or LOAD IMMEDIATE operation. These operations are also used for loading the EI, FQR, PIO1 and PIO2 bits. Furthermore, the programmer can load the FQR bit using a MOVE or LOAD IMMEDIATE operation without changing the other bits in the PST register.

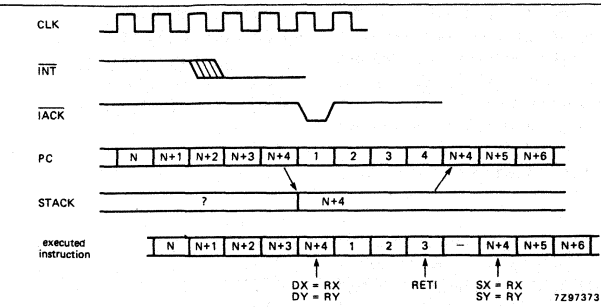
The PST and IOF register can be read using a MOVE operation. The flags can also be used as conditions in BRANCH operations (see section 2.2.7 on BRANCH circuitry). "Lock" type flags will automatically be reset to 0 when they are tested in a BRANCH operation.

2.2.9 Interrupt circuitry ($\overline{INT}$ and $\overline{IACK}$ pins, RX and RY)

The processor has an interrupt facility that the user can access via the $\overline{INT}$ and $\overline{IACK}$ pins. When an interrupt is accepted by the processor the program counter is loaded with address 1. The interrupt procedure is described below and the logic timing diagrams are given in Figures 2.2.9-1 and 2.2.9-2.

An interrupt is initiated by a LOW on the $\overline{INT}$ pin. The first positive going edge of CLK after a HIGH to LOW transition on $\overline{INT}$, the interrupt is clocked in by the processor. Two or three clock pulses later (see timing diagrams), the processor decides to accept the interrupt or postpone it. An interrupt is postponed:

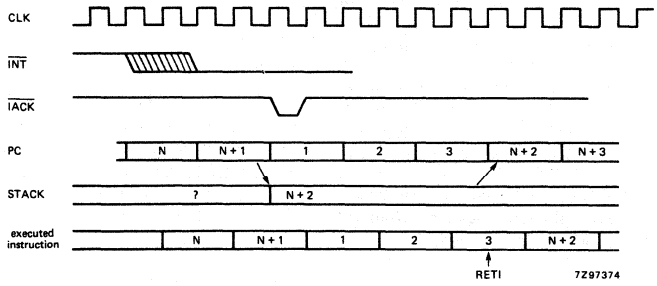
- while the PC is being loaded (as part of a BRANCH, MOVE or LOAD IMMEDIATE operation)
- while the RPR register is loaded
- during instruction repetition
- when the stack is the source or destination to the X-bus
- when the interrupt is disabled by software (EI bit in PST register is 0).



Note 1: The interrupt is postponed when one of the following conditions is true during instruction N + 3:
- loading of PC (as part of BRANCH or MOVE operation)
- loading of RPR
- stack source or destination to X-bus
- repetition mechanism on
- interrupt disabled by EI = 0

Note 2: Instruction N + 4 is executed only after the interrupt routine; before the interrupt routine only the bus sources are stored in RX and RY

Fig. 2.2.9-1 Interrupt logic timing in P-mode.



Note: The interrupt is postponed when one of the following conditions is true during instruction N + 1:
- loading of PC (as part of BRANCH or MOVE operation)
- loading of RPR
- stack source or destination to X-bus
- repetition mechanism on
- interrupt disabled by EI = 0

Fig. 2.2.9-2 Interrupt logic timing in NP-mode.

As soon as the above situations are completed, the postponed interrupt is accepted and thereafter handled in the same way as an interrupt that was accepted directly.

Accepting the interrupt means pushing the value of the PC (in P-mode) or PC+1 (NP-mode) on to the stack and loading the PC with address 1. When the PC contains address 1, the $\overline{IACK}$ pin goes LOW for one clock cycle to indicate to the outside world that the interrupt has been acknowledged.

In the P-mode, the instruction in the pipeline that should have been executed is not executed while the PC contains address 1 even though the expected X and Y-bus sources put their data on the buses. This data is stored in the bus-save register, RX and RY, that are automatically assigned as the destinations for the buses.

An interrupt routine is completed under program control using an RETI conditional BRANCH operation (see instruction set section 3.0). When the condition is true, PC is loaded with the address that was pushed onto the stack, and then the instruction at that address is executed. In the P-mode, however, RX and RY are used instead of the indicated X and Y-bus sources. Nested interrupts are permitted, but in the P-mode they are latched so long as the programmer has not stored the data in RX and RY elsewhere (i.e. so long as RX and RY have not been used as sources for the X and Y-buses). After returning from a nested interrupt in the P-mode, the old contents of RX and RY must be restored by the programmer.

Note: A new interrupt can only be generated after the $\overline{INT}$ signal has been HIGH for at least one positive going edge on CLK.

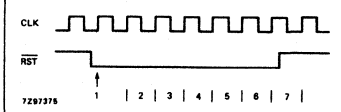
RX and RY can be used as general purpose registers when the interrupt is not used.

2.2.10 Reset circuitry ($\overline{RST}$ pin)

The processor is reset to an initial state when RST is LOW over at least 7 rising edges of CLK. A shorter reset may lead to an undefined situation.
The initial state is characterized by:

- PC : all zeros
- PST : all zeros
- IOF : SIXACK = SIYACK = 0 and SOXACK = SOYACK = 1
- RX, RY : all zeros
- STACK : all zeros (5 x 10)
- RPR : instruction repeat mechanism off
- LPR : STATE = 0
- MXL, MYL : all zeros
- RAMA(0) : all zeros
- RAMB(0) : all zeros
- PR : all zeros
- ACR : all zeros
- BSR : all zeros
- AAL, ABL : all zeros
- ARA, AA, SA : all zeros
- ARB, AB, SB : all zeros
- ARR, AR, SR : all zeros
- MA, MB, MR : all zeros
- PG : all zeros
- SIOST : all zeros
- SOX, SOY : all zeros
- $\overline{SIXRQ}$ = $\overline{SIYRQ}$ = 0
- $\overline{SOXRQ}$ = $\overline{SOYRQ}$ = 1

The logic timing of the reset is shown in Fig. 2.2.10-1.



1 – reset detection
2 – reset of all registers and latches mentioned above (excluding ACR), and "top of stack", serial I/O request signals, and PR
3 – reset of ACR and 2nd stack position
4 – reset of 3rd stack position
5 – reset of 4th stack position
6 – reset of 5th stack position
7 – reset of 6th stack position (note: this stack position must not be used, otherwise it may lead to an undefined state).

Fig. 2.2.10-1
The complete reset action.

2.2.11 Synchronization circuitry (SYNC pin)

The processor indicates where execution of a new instruction starts with a HIGH at the SYNC pin for half a clock cycle. This occurs once every two clock cycles in the NP-mode, and once every clock cycle in the P-mode. However, in the P-mode it will not occur when the program counter is loaded with a new address during the execution of a BRANCH operation, a MOVE operation, an interrupt, or a reset.

2.3 DATA MEMORIES AND ACU'S

2.3.1 Data memories

The processor contains 3 on-chip data memories:

- RAMA: 128 x 16 bits, static
- RAMB: 128 x 16 bits, static
- ROM : 512 x 16 bits (only on PCB5010, external for PCB5011)

It is also possible to connect up to 64K of external data memory via the parallel I/O.

Memory outputs are connected to the data registers (DRA, DRB and DRR) and the parallel data input register PI. DRA, DRB and DRR are updated every instruction cycle, but in the P-mode, DRA and DRB are not updated when in that instruction cycle, data is moved (from one of the buses) into RAMA or RAMB. Updating PI is described in the section 2.6 on the parallel I/O. Data written into the data registers and PI can be transferred via the X or Y-bus during a subsequent instruction.

RAMA can be written-to via the X-bus, RAMB can be written-to via the Y-bus and, external RAM can be written-to via either bus.

With the PCB5011, it is not only possible to read from an external ROM, but in place of the read, it is also possible to write-to an external 512 x 16-bit memory because the port is bidirectional, and therefore can be used as a second parallel I/O port.

2.3.2 ACUs and PG register

The 3 address computation units, ACUA, ACUB and ACUR, function identically but, their address widths differ: 12, 8 and 9 bits respectively. ACUs calculate the addresses for the on-chip RAMs (only the 7 least significant address bits are used for this addressing) and data ROM. ACUA not only generates the address for RAMA but also the part of the address for external data memory that defines the position within a page of 4096 x 16 words. It is possible to have 16 pages of external data memory. Pages are selected using the address pins A12 to A15 that reflect the contents of the page register PG that is loaded using a MOVE or LOAD IMMEDIATE operation.

Fig. 2.3.2-1 illustrates the memory addressing.

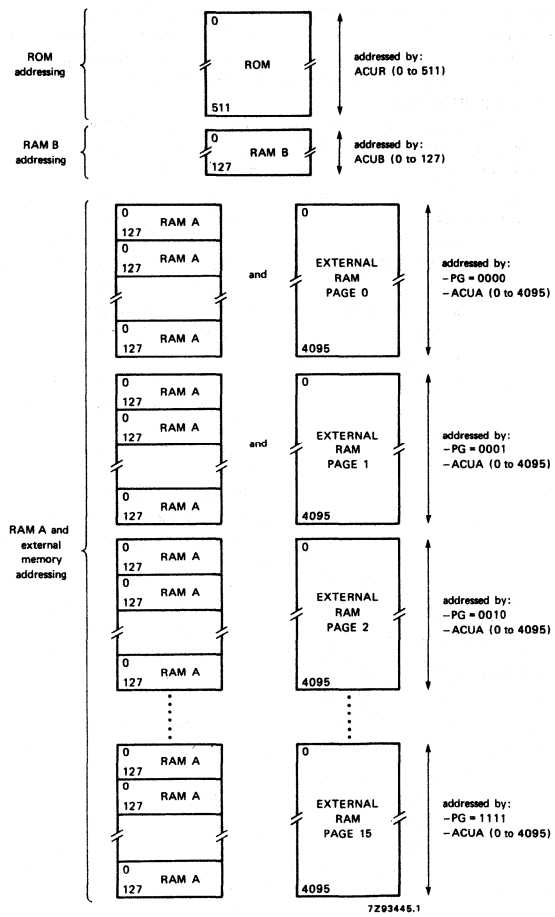


Fig. 2.3.2-1 Memory addressing.

Note:

RAMA and the external RAM are always simultaneously accessed by ACUA. A read-access results in loading of DRA and (under certain conditions determined by the PI01 and PI02 bits) simultaneous loading of PI. A next instruction specifies which of the two words (or both) are transferred to other places within the DSP via the data buses. A write-access results in an update of RAMA and/or the external RAM, depending on the specified destinations.

An ACU contains:
- an address register AR (which addresses the ROM respectively RAM's)
- a base address register A
- an offset register S
- an address masking register M
- a dedicated arithmetic unit

Only the AR registers (ARR, ARB and ARA) are shown in Figs 2.1-1 and 2.1-2. The A, S and M registers of RAMA, RAMB and the ROM (AA/BA/RA, AS/BS/RS and AM/BM/RM) are not shown.
The A, S, M and AR registers can be loaded directly (for initialization) via one of the data buses (X-bus for ACUB registers and Y-bus for ACUA and ACUR registers) using a MOVE or LOAD IMMEDIATE operation or they can be modified during address computation operations. Direct loading and address computation cannot take place simultaneously (see the section 3.0 on the instruction set).

Direct loading offers the following options:
- Load AR with value on the bus
- Load AR and A with value on the bus
- Load AR and S with value on the bus
- Load A with value on the bus
- Load S with value on the bus
- Load M with value on the bus
- Load AR, A and S with value on the bus
- Load AR with (value on the bus) !M

The notation !M means that, depending on the contents of the M register, all bits are not necessarily updated as the expression indicates:
- the bits whose corresponding bits in the M register are 1 are updated as specified in the expression
- the bits whose corresponding bits in the M register are 0 will retain their value (for AR) or will receive the previous value of their AR bit (for A and S).

The notation br(. . .) means that the bits are reversed in order.

Three flags in the PST register indicate the status of the 3 ACU's:
- ACA – ACUA flag
  is 1 when AR contains 0000 0000 0000;
  is 0 when AR does not contain 0000 0000 0000
- ACB – ACUB flag
  is 1 when AR contains 0000 0000;
  is 0 when AR does not contain 0000 0000
- ACR – ACUR flag
  is 1 when AR contains 0 0000 0000;
  is 0 when AR does not contain 0 0000 0000

Address computation offers the following options:

• AR:=AR	A:=A	S:=S	M:=M
• AR:=(A+1)!M	A:=(A+1)!M	S:=S	M:=M
• AR:=(A−1)!M	A:=(A−1)!M	S:=S	M:=M
• AR:=(A+S)!M	A:=(A+S)!M	S:=S	M:=M
• AR:=(S+1)!M	A:=A	S:=(S+1)!M	M:=M
• AR:=(A)!M	A:=A	S:=S	M:=M
• AR:=(S)!M	A:=A	S:=S	M:=M
• AR:=br(A+S)	A:=A+S	S:=S	M:=M

2.4 MULTIPLIER, ACCUMULATOR, BARREL-SHIFTER AND FORMAT-ADJUSTER UNIT

2.4.1 Multiplier

The multiplier performs a multiplication of two signed 16 bits operands P and Q presented in 2's complement notation. The result is presented by 32 bits in 2's complement notation and stored in the product result latch PR.

One of the following values can be chosen as P-operand:
- The value present on the X-bus
- The previous value which was automatically latched in the MXL latch
- The number −1

One of the following values can be chosen as Q-operand:
- The value present on the Y-bus
- The previous value which was automatically latched in the MYL latch
- The negated Y-bus value
  Note: when the Y-bus contains the highest negative value, -2^{15} (1000 0000 0000 0000 in binary) then the operand will be the highest positive value plus one, $+2^{15}$ (1 0000 0000 0000 0000 in binary). This number is stored in MYL which has a width of 17 bits for this particular situation.

The contents of MXL, MYL and PR are not changed when no MULTIPLY operation or a multiply HOLD operation is executed.

2.4.2 Accumulator

The accumulator unit consists of a 40 bit adder ACC, a 40 bit multiplication/accumulation register ACR and a sign and scale down block S/SD. The adder adds the in PR stored result of the multiplication to a second operand (provided by the S/SD block) which can be chosen from the following set:

- + or − the contents of ACR
- + or − the contents of ACR divided by 2^{15} (which allows multiprecision multiplication and addition)
- the number 0

The result of the addition is stored in ACR and is fed simultaneously to the barrel-shifter. The contents of the ACR register are not changed when no MULTIPLY operation is performed or a multiply HOLD operation is executed.

The 40-bit width of the accumulator allows the programmer to accumulate a number of multiplier results (at least 256) without the risk of overflow. Two flags in the PST register indicate the status of the accumulator:

- OVFL − overflow lock flag; this flag is set when overflow occurs in the adder (result outside the range -2^{39} to $+2^{39}-1$). For reset conditions see description of PST register (section 2.2.8).
- SGNM − sign flag; indicates the sign of the result of the addition (is identical to bit ACR(39)).

2.4.3 Barrel-shifter

From the 40-bit ACR contents, the barrel-shifter extracts 32 contiguous bits. The programmer determines which group of 32 bits is extracted by a value placed in the BSR register (bits BSR3 to BSR0).
Sixteen different sets are possible:

BSR contents BSR3 - BSR0	32-bit word, E31 - E0, extracted by the barrel-shifter
0000	ACR30, ... ,ACR0,0
0001	ACR31, ... ,ACR0
0010	ACR32, ... ,ACR1
0011	ACR33, ... ,ACR2
0100	ACR34, ... ,ACR3
0101	ACR35, ... ,ACR4
0110	ACR36, ... ,ACR5
0111	ACR37, ... ,ACR6
1000	ACR38, ... ,ACR7
1001	ACR39, ... ,ACR8
1010	ACR39,ACR39, ... ,ACR9
1011	ACR39,ACR39,ACR39, ... ,ACR10
1100	ACR39,ACR39,ACR39,ACR39, ... ,ACR11
1101	ACR39,ACR39,ACR39,ACR39,ACR39, ... ,ACR12
1110	ACR39,ACR39,ACR39,ACR39,ACR39,ACR39, ... ,ACR13
1111	ACR39,ACR39,ACR39,ACR39,ACR39,ACR39,ACR39,. . . . ,ACR14

Two flags in the PST register indicate the status of the barrel-shifter:

- OOR − Out of range flag. It is set when the sign bit of the extracted word E31-E0 has no significance. This occurs when one or more bits of ACR to the left of the extracted word differs from E31.
- OORL − Out of range lock flag. The conditions for setting are identical to those of OOR. The conditions for resetting are given in the section describing the PST register.

2.4.4 Format adjuster

The output E31-E0 of the barrel-shifter is split into a 16-bit most significant part MSP and a 16-bit least significant part LSP'. MSP can be connected directly to the X and/or Y bus. LSP' passes through a format adjuster (FA) before it reaches the X or Y bus. The output of FA is called LSP. Under software control, three FA options can be selected by placing a value in the BSR register (bits BSR5 to BSR4). The options are:

BSR contents BSR5 - BSR4	output LSP of format adjuster
00	E15-E0 (no change)
01	E0-E15 (bits reversed in order, used to speed-up certain serial outputs)
10	0, E15-E1 (bits shifted right over 1 position, left adjusted with zero; used for multi-precision multiplications)
11	reserved/undefined

2.4.5 Barrel-shifter register (BSR)

BSR is a 6-bit register. Its contents control the barrel-shifter (bit 0-3) and the format adjuster (bit 4-5) as explained in the previous sections. BSR can be loaded by means of a MOVE or LOAD IMMEDIATE operation. Loading has to be done at least one instruction before LSP or MSP is read to the X or Y-bus.

2.5 ALU AND REGISTER FILE

2.5.1 ALU

The PCB5010/11 has an ALU totally independent from the multiplier/accumulator unit. It is a 16-bit, 2-operand unit capable of executing 31 distinct operations. There are arithmetic, logic and some special purpose operations. The arithmetic operations defined as "extended" (mnemonic starts with X) are included to facilitate multi-precision operations. Extended operands are represented by 16-bit multiples.

An ALU operation produces a result R that may be stored in the register file or may be ignored (dumped in the trash can).

Several flags in the PST register give the status of the ALU. The flags are:
Z — Zero flag
N — Negative flag
C — Carry flag
V — Overflow flag
VL — Overflow lock flag (same as V but locked; see PST register description, section 2.2.8).

One of the following values can be chosen as A-operand:
- the value on the X-bus
- the value on the Y-bus
- the previous value which was automatically latched in the AAL-latch (this is not the case with the "byte swap" instruction).

One of the following values can be chosen as B-operand:
- the value on the Y-bus
- the previous value which was automatically latched in the ABL-latch

Dyadic operations require an A and B-operand, while monadic operations require only an A-operand. Some operations do not require an operand at all.

The ALU operations and their result R and flag settings are summed up in the following three tables:
A: Arithmetic operations
B: Logic operations
C: Other operations

The following notation is used:

- ZERO(R) — 0 (when not all 16 bits of R are 0)
  — 1 (when all 16 bits of R are 0)
- CARRY(F) — 0 (when a function F does not lead to a carry)
  — 1 (when a function F leads to a carry)
  Note: For this calculation, the operands are unsigned 16-bit numbers from 0 to 65535. The carry is 1 when the result of the addition is greater than 0. In all other cases the carry is 0.
- BORROW(F) — 0 (when a function F does not lead to a borrow)
  — 1 (when a function F leads to a borrow)
  Note: For this calculation, the operands are unsigned 16-bit numbers from 0 to 65535. The borrow is 1 when the result of the subtraction is below 0. In all other cases the borrow is 0.
- OVERFLOW(F) — 0 (when a function F does not lead to an overflow)
  — 1 (when a function F leads to an overflow)
  Note: For this calculation, the operands are signed 16-bit numbers between -2^{15} and $2^{15}-1$. The overflow is 1 when the result of the calculation is outside this range. In all other cases the overflow is 0.
- R(i) — Bit i of the 16-bit word R.

A: Arithmetic operations (see table on next page)

For the calculation of result R, the operands A and B are considered to be binary numbers in 2's complement notation (between -2^{15} and $+2^{15}-1$). R is also a binary number in 2's complement notation. However, with the DIV operation, the operands and the result are unsigned numbers (between 0 and 65535).

DEVELOPMENT DATA

A: Arithmetic operations

function	mnemonic	result (R)	flags				condition
			Z	N	C	V	
addition	ADD	A+B	ZERO(R)	R(15)	CARRY(A+B)	OVERFLOW(A+B)	no overflow
		$A+B-2^{16}$	ZERO(R)	R(15)	CARRY(A+B)	OVERFLOW(A+B)	positive overflow
		$A+B+2^{16}$	ZERO(R)	R(15)	CARRY(A+B)	OVERFLOW(A+B)	negative overflow
extended addition	XADD	A+B+C	ZERO(R).AND.Z	R(15)	CARRY(A+B+C)	OVERFLOW(A+B+C)	no overflow
		A+B+C−2(16)	ZERO(R).AND.Z	R(15)	CARRY(A+B+C)	OVERFLOW(A+B+C)	positive overflow
		A+B+C+2(16)	ZERO(R).AND.Z	R(15)	CARRY(A+B+C)	OVERFLOW(A+B+C)	negative overflow
subtraction	SUB	A−B	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	no overflow
		$A-B-2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	positive overflow
		$A-B+2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	negative overflow
extended subtraction	XSUB	A−B−C	ZERO(R).AND.Z	R(15)	BORROW(A−B−C)	OVERFLOW(A−B−C)	no overflow
		$A-B-C-2^{16}$	ZERO(R).AND.Z	R(15)	BORROW(A−B−C)	OVERFLOW(A−B−C)	positive overflow
		$A-B-C+2^{16}$	ZERO(R).AND.Z	R(15)	BORROW(A−B−C)	OVERFLOW(A−B−C)	negative overflow
conditional subtraction	CSUB	A	ZERO(R)	R(15)	0	0	N=0
		A−B	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	no overflow
		$A-B-2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	positive overflow } N=1
		$A-B+2^{16}$	ZERO(R)	R(15)	BORROW(A−B)	OVERFLOW(A−B)	negative overflow
negate	NEG	0−A	ZERO(R)	R(15)	BORROW(0−A)	OVERFLOW(0−A)	$A \neq -2^{15}$
		A	ZERO(R)	R(15)	BORROW(0−A)	OVERFLOW(0−A)	$A = -2^{15}$
extended negate	XNEG	0−A−C	ZERO(R).AND.Z	R(15)	BORROW(0−A−C)	OVERFLOW(0−A−C)	$A \neq -2^{15}$.OR.C = 1
		A	ZERO(R).AND.Z	R(15)	BORROW(0−A−C)	OVERFLOW(0−A−C)	$A = -2^{15}$.AND.C = 0
conditional negate	CNEG	A	ZERO(R)	R(15)	0	0	
decrement	DEC	A−1	ZERO(R)	R(15)	BORROW(A−1)	OVERFLOW(A−1)	$A \neq -2^{15}$
		$2^{15}-1$	ZERO(R)	R(15)	BORROW(A−1)	OVERFLOW(A−1)	$A = -2^{15}$
extended decrement	XDEC	A−C	ZERO(R).AND.Z	R(15)	BORROW(A−C)	OVERFLOW(A−C)	$A \neq -2^{15}$.OR.C = 0
		$2^{15}-1$	ZERO(R).AND.Z	R(15)	BORROW(A−C)	OVERFLOW(A−C)	$A = -2^{15}$.AND.C = 1
increment	INC	A+1	ZERO(R)	R(15)	CARRY(A+1)	OVERFLOW(A+1)	$A \neq 2^{15}-1$
		-2^{15}	ZERO(R)	R(15)	CARRY(A+1)	OVERFLOW(A+1)	$A = 2^{15}-1$
extended increment	XINC	A+C	ZERO(R).AND.Z	R(15)	CARRY(A+C)	OVERFLOW(A+C)	$A \neq 2^{15}-1$.OR.C = 0
		-2^{15}	ZERO(R).AND.Z	R(15)	CARRY(A+C)	OVERFLOW(A+C)	$A = 2^{15}-1$.AND.C = 1
arithmetic shift left	ASL	2*A	ZERO(R)	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$-2^{14} < A < 2^{14}$
		$2*A-2^{16}$	ZERO(R)	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A \geqslant 2^{14}$
		$2*A+2^{16}$	ZERO(R)	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A < -2^{14}$
extended arithmetic shift left	XASL	2*A+C	ZERO(R).AND.Z	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$-2^{14} < A < 2^{14}$
		$2*A+C-2^{16}$	ZERO(R).AND.Z	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A \geqslant 2^{14}$
		$2*A+C+2^{16}$	ZERO(R).AND.Z	R(15)	CARRY(A+A)	OVERFLOW(A+A)	$A < -2^{14}$
arithmetic shift right	ASR	A/2-fraction	ZERO(R)	R(15)	1(0)	0	
extended arithmetic shift right	XASR	A/2-fraction	ZERO(R).AND.Z	N	A(0)	0	MSB of A = C
		$A/2\text{-fraction}-2^{15}$	ZERO(R).AND.Z	N	A(0)	0	MSB of A = 0.AND.C = 1
		$A/2\text{-fraction}+2^{15}$	ZERO(R).AND.Z	N	A(0)	0	MSB of A = 1.AND.C = 0

A: Arithmetic operations (Cont'd)

function	mnemonic	result (R)	flags				condition
			Z	N	C	V	
add MSB of B to A	ADDM	A+B(15) A+B(15)−2^{16}	ZERO(R) ZERO(R)	R(15) R(15)	CARRY(A+B(15)) CARRY(A+B(15))	OVERFLOW(A+B(15)) OVERFLOW(A+B(15))	A+B(15) < 2^{15} A+B(15) = 2^{15}
unsigned division	DIV	2*(A−B) 2*A	ZERO(R) ZERO(R)	R(15) R(15)	$\overline{\text{BORROW(A−B)}}$ $\overline{\text{BORROW(A−B)}}$	0 0	0 ⩽ A−B < 2^{15} A−B < 0 or A−B > 2^{15}
sign extension	XSGN	NN . . . . N	Z.AND.NOT.N	N	N	V	

B: Logic operations

For the calculation of result R, the operands A and B are considered to be 16-bit binary words. R is also a 16-bit binary word.

function	mnemonic	result (R)	flags				condition
			Z	N	C	V	
complement	COM	.NOT.A(i)		R(15)	0	0	for i=0 . . . 15
logic AND	AND	A(i).AND.B(i)	ZERO(R)	R(15)	0	0	for i=0 . . . 15
logic OR	OR	A(i).OR.B(i)	ZERO(R)	R(15)	0	0	for i=0 . . . 15
exclusive OR	EXOR	A(i).EXOR.B(i)	ZERO(R)	R(15)	0	0	for i=0 . . . 15
byte swap	SWAP	A(i+8) A(i−8)	ZERO(R) ZERO(R)	R(15) R(15)	0 0	0 0	for i=0 . . . 7 for i=8 . . . 15
logic shift left	LSL	A(i−1) 0	ZERO(R) ZERO(R)	A(14) A(14)	A(15) A(15)	0 0	for i=1 . . . 15 for i=0
logic rotate left	LROL	A(i−1) C	ZERO(R) ZERO(R)	A(14) A(14)	A(15) A(15)	0 0	for i=1 . . . 15 for i=0
logic shift right	LSR	A(i+1) 0	ZERO(R) ZERO(R)	0 0	A(0) A(0)	0 0	for i=0 . . . 14 for i=15
logic rotate right	LROR	A(i+1) C	ZERO(R) ZERO(R)	0 0	A(0) A(0)	0 0	for i=0 . . . 14 for i=15

C: Other operations

function	mnemonic	result (R)	flags				condition
			Z	N	C	V	
pass and flag update	PASS	A	ZERO(A)	A(15)	0	0	
generate 0	NULL	0	1	0	0	0	
no operation	–	–	Z	N	C	V	

2.5.2 Register file

The output of the ALU is connected to the register file. This register file contains fifteen 16-bit registers. The programmer can choose to which register the ALU result is written and also has the option of discarding the result by writing it to the trash can.

The contents of any register may be read to either or both of the buses. Moreover, the register file is implemented as a 3-port memory, so that in the same instruction cycle three registers can be accessed: two accesses to read the present contents of register(s) and one to write in a new value.

The register file can be filled directly from the buses by a MOVE or LOAD IMMEDIATE operation. This does not affect the ALU flags but the AAL-latch will be updated. ALU operations cannot be specified simultaneously with the aforementioned MOVE operation.

2.6 PARALLEL I/O

Via the D15 – D0 pins, the PCB5010/11 permits parallel communication between the X or Y-bus and the outside world. An input or output can take place during each instruction cycle. Output occurs when data is transferred via the X or Y-bus with destination PO. The output is direct, there is no latching. Inputs are loaded into the parallel input latch PI, whose contents can be transferred via the X or Y-bus during a subsequent instruction. The programmer can select one of three input criteria by writing specified values into PST bits, PIO1 and PIO2;

The following control signals are associated with the parallel I/O (see timing in section 4):

- R/$\overline{W}$: indicates a read or write action (output)
- $\overline{DS}$: data strobe (output)
- $\overline{WAIT}$: signals for synchronization of the parallel I/O (input). This signal delays the internal clock, so that "slow" peripheral devices may be connected. Note: that $\overline{WAIT}$ signal can also be used with the second parallel I/O port in the PCB5011 (see section 2.3.1).

A block diagram of the parallel I/O circuitry is shown in Fig. 2.6-1.

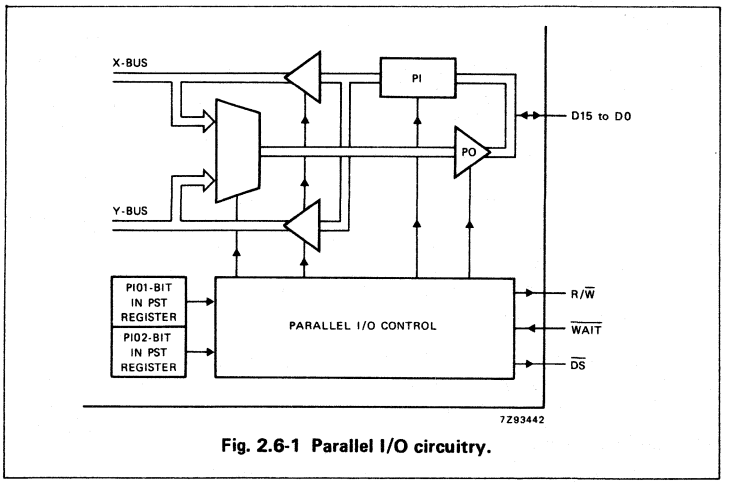


Fig. 2.6-1 Parallel I/O circuitry.

PIO1	PIO2	
0	0	A read action is performed each instruction cycle
0	1	A read action is performed only when: – ACUA is not executing a "no operation", or when – PI latch is source to X or Y-bus
1	0	A read action is performed only when: – PI latch is source to X or Y-bus
1	1	Reserved

Note: a read is only performed when there is no write (MOVE or LOAD IMMEDIATE operation to PO).

2.7 SERIAL I/O

The PCB5010/11 has 2 independent serial inputs DIX and DIY and 2 independent serial outputs DOX and DOY (destinations and sources for X and Y-bus respectively). Actual transfer occurs, with a maximum speed of 4 million bits/s, under the control of clocks CIX, COX, CIY, and COY from external devices.

The following handshake signals, described in more detail in the following sections, are associated with the serial I/O:
- input/output enable $\overline{\text{SIXEN}}$, $\overline{\text{SOXEN}}$, $\overline{\text{SIYEN}}$ and $\overline{\text{SOYEN}}$ (input signals)
- input/output request $\overline{\text{SIXRQ}}$, $\overline{\text{SOXRQ}}$, $\overline{\text{SIYRQ}}$ and $\overline{\text{SOYRQ}}$ (output signals)

The following flags, whose functions are also described in the following sections, are associated with the serial I/O:
- serial I/O acknowledge flags SIXACK, SOXACK, SIYACK and SOYACK.

The programmer may control the length of the words to be transferred (between 1 and 16 bits) by writing the applicable values in the SIOST register fields:

bit: 15 14 13 12	11 10 09 08	07 06 05 04	03 02 01 00
SOLY	SILY	SILX	SOLX

SILX = length of serial input word with destination X-bus
SOLX = length of serial output word with source X-bus
SILY = length of serial input word with destination Y-bus
SOLY = length of serial output word with source Y-bus

The binary number in each field specifies the length; the code 0000 indicates a length of 16 bits.

2.7.1 Serial input procedure

The serial input procedure, as illustrated in the flow diagram in Fig. 2.7.1-1, is described below. A detailed block diagram of the serial input circuitry (Fig. 2.7.1-2) is needed to understand the procedure.

Note: Only the serial input via the DIX pin is described since the serial input via the DIY pin operates in the same way.

1. At reset, the SIXACK flag is reset to '0' indicating that no word has been received in the SIX latch awaiting transfer via the X-bus.

2. The $\overline{\text{SIXRQ}}$ signal is reset to '0', indicating to external devices that they are allowed to send new data.

3. Nothing happens until the external device enables the serial input by setting the input signal $\overline{\text{SIXEN}}$ to '0'. This is checked only on the rising edge of the incoming clock signal CIX.

   $\overline{\text{SIXEN}}$ equal to '0', results in the shifting in of the first bit (LSB) available via the DIX pin. Then an internal counter COUNT is set to one less than the word-length. The word-length information is taken from the SILX field of the SIOST register.

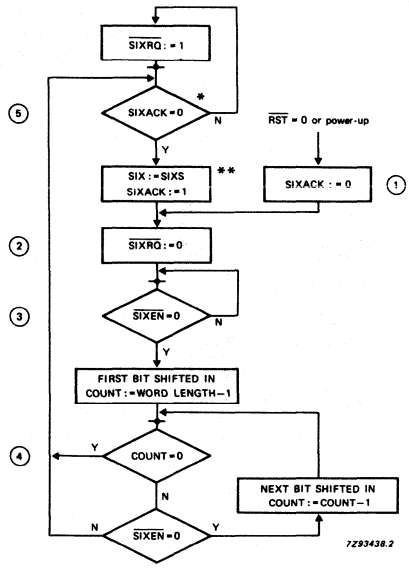
4. At the next rising edge of the incoming clock signal CIX, the contents of COUNT is tested. When the contents of the counter is zero, data input is finished (continue at step 5). If it does not contain zero the data input continues as long as the $\overline{\text{SIXEN}}$ signal is '0': COUNT is decremented and a bit is shifted in via the DIX pin. Step 4 is then repeated. When the $\overline{\text{SIXEN}}$ signal is one, the data input is finished (aborted) and the procedure continues with step 5.

5. After finishing data input, the content of the shift register SIXS is copied to latch SIX. When less than 16 bits have been received the word is placed in the most significant part of SIX and the remaining bits are set to '0'. Also, the SIXACK flag is set to 1 indicating that a word has been received and is awaiting transfer via the X-bus.

   This copying and flag setting however does not occur when the SIXACK flag is not '0' (indicating that the previous input has not been transferred via the X-bus; note that the first time after reset or power up SIXACK is always 0). The $\overline{\text{SIXRQ}}$ signal is set to one, indicating to external devices that they are not allowed to send new data.

   After SIXACK has become '0' (this is tested only at rising edges of the CIX clock signal) the copying and flag setting finally takes place. The procedure continues with step 2.

Note: After changing the contents of the SILX and SILY fields of the SIOST register (which means: changing the word-length) the contents of SIX and SIY are undefined.



* SIXACK goes to 0 when SIX is the source on the X-bus.
** When less than 16-bits have been received, the word is placed in the most significant part of SIX and the remaining bits are set to 0.
◆ This point is only passed when a rising edge on CIX occurs.

Fig. 2.7.1-1 Serial input procedure.

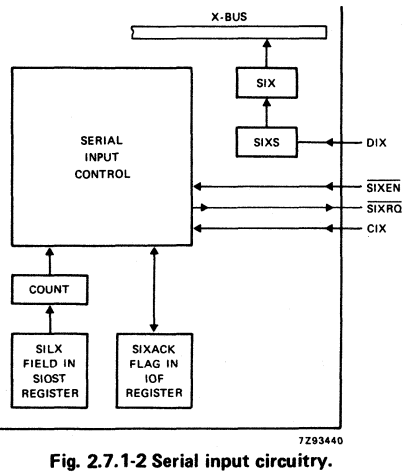


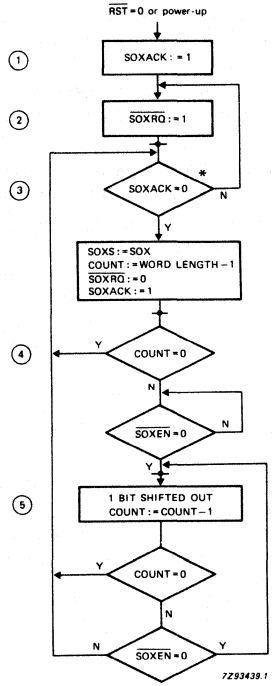
Fig. 2.7.1-2 Serial input circuitry.

2.7.2 Serial output procedures

The serial output procedure, as illustrated in the flow diagram in Fig. 2.7.2-1 is described below. A detailed block diagram of the serial output circuitry (Fig. 2.7.2-2) is needed to understand the procedure.

Note: Only the serial output via the DOX pin is described; the serial output via the DOY pin operates in the same way.

1. At reset, the SOXACK flag is set to '1', indicating that a word may be transferred via the X-bus to the SOX latch.
2. The $\overline{\text{SOXRQ}}$ output signal is set to '1' indicating to the external devices that there is no data available to be clocked out. The procedure is suspended until the first falling edge of incoming clock signal COX.
3. When the SOXACK flag is not '0' (then no data has been transferred via the X-bus to the SOX latch), step 2 is repeated. When SOXACK is '0' (data has been transferred via the X-bus to the SOX latch), the data in the SOX latch is copied to the SOXS output shift register. The first bit (LSB) of the word that must be shifted out is placed in front of the output 3-state driver.
   Then the $\overline{\text{SOXRQ}}$ output signal is set to '0' indicating to the external devices that data is available to be clocked out.
   Also, the SOXACK flag is set to one to indicate that a new data word may be transferred via the X-bus to the SOX latch. Finally, an internal counter is loaded with a value one less than the word-length. The word-length information is taken from the SOXL field of the SIOST register.
   The procedure is now suspended until the next falling edge of the incoming clock signal COX.
4. When the word-length is 1 (then the count is 0), the output procedure is finished. One bit words can be read by external devices that set the $\overline{\text{SOXEN}}$ signal to '0' which enables the 3-state output buffer. In this case, the procedure continues with step 3. It is important to note that SOXS can be overwritten before the bit has been read by the external devices.
   When the word-length is greater than 1 (then count is not equal to zero) the output procedure is not finished.
   The procedure is suspended until one of the external devices enables the serial output by setting the input signal $\overline{\text{SOXEN}}$ to '0'. The first bit is available on the DOX pin immediately after the serial output is enabled.
5. Nothing happens until a falling edge on the clock input COX is generated. At that moment another bit in the SOXS shift-register is shifted out via DOX. In addition, the contents of the counter is decremented. The output is finished when the counter contents has been decremented to zero (continue at step 3).
   If after decrementing, the counter value is not zero, the output continues by repeating step 5 unless $\overline{\text{SOXEN}}$ is now '1'. When $\overline{\text{SOXEN}}$ = 1, the output is finished (aborted) and the procedure continues at step 3.



* SOXACK goes to 0 when SOX is the destination on the X-bus.

◆ This point is only passed when a falling edge on COX occurs.

Note: DOX is not enabled (in the 3-state mode) while $\overline{SOXEN}$ = 1.

Fig. 2.7.2-1 Serial output procedure.

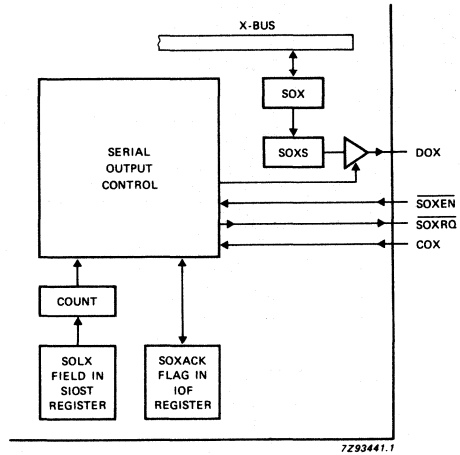


Fig. 2.7.2-2 Serial output circuitry.

2.8 DATA BUSES X AND Y

The data buses have a width of 16-bits and are used for transferring data between the functional units connected to them. Bus transfers are always part of MOVE and LOAD IMMEDIATE operations and can be part of MPY and ALU operations. The possible sources and destinations of the bus are given in the table below.

source on X	destination on X	source on Y	destination on Y
STACK	STACK		
RX	RX	RY	RY
	PC		
	RPR		
IOF			
IR(DATA field)		IR(DATA field)	
PST	PST	PST	
	FQR		
DRA DRB DRR		DRA DRB DRR	
	RAMA		RAMB
ARB		ARA ARR	
	ACUB		ACUA ACUR
		PG	PG
	ILX		ILY
LSP MSP		LSP MSP	
		BSR	BSR
RFILE	RFILE	RFILE	RFILE
	ILA		ILA ILB
PI	PO	PI	PO
SIOST	SIOST		
SIX SOX	SOX	SIY SOY	SOY

Note 1: FQR is loaded by putting the required value (0 or 1) in bit 15 of the 16-bit word that is sent. The other bits are 'don't cares'.

Note 2: When the source or destination has a width of less than 16 bits, only the least significant bits on the bus (same width) contain information. For a source, the MSBs are set to zero.

Note 3: ILX and ILY select the operands for the multiplier; ILA and ILB select the operands for the ALU.

3.0 INSTRUCTION SET

The behaviour of the processor is controlled by the instructions stored in on-chip ROM (PCB5010) or external program memory (PCB5011). Each instruction leads to the execution of one or more (up to 6) basic operations. The basic operations, the instruction format and the instruction fields are described in the following sections.

3.1 BASIC OPERATIONS

The execution of a basic operation can take either 1 or 2 clock cycles. This means that:

- for 2 cycle basic operations pipelining is used in the P-mode
- a 1 cycle operation is extended by a second "no action" cycle when the processor is operating in the NP-mode.

Basic operation sequencing is shown in Fig. 3.1-1 for the P-mode, and Fig. 3.1-2 for the NP-mode. There are 6 different basic operations which are described below.

- **ALU operation** (1 clock cycle)

  One of 31 different ALU operations is executed. The operations need 2, 1 or 0 operands. The operation's result is stored in the register file or thrown away (into the trash can). In addition, a number of flags are updated.

- **MOVE operation** (1 clock cycle)

  Data from an X-bus (Y-bus) source is transferred via the X-bus (Y-bus) to an X-bus (Y-bus) destination. In the case that both buses have the same destination no transfer takes place.

- **ACU (address computation and memory access) operation** (2 clock cycles)

  Clock cycle 1:
  An address is calculated by the ACU and written into an address register (ARA, ARB, or ARR).

  Clock cycle 2:
  RAMA, RAMB, ROM or external memory is accessed at the location given by the address register (ARA, ARB, or ARR). This access is normally a read which updates one of the data registers (DRA, DRB, DRR, or PI). If in the P-mode, however, the relevant RAM (RAMA, RAMB or external RAM) is assigned as a destination during a MOVE executed in parallel, the access will be a write. The result in this case is that the RAM is updated.

- **MPY (multiply/accumulate) operation** (2 clock cycles)

  Clock cycle 1:
  Two operands are multiplied together and the result stored in the PR latch.

  Clock cycle 2:
  The content of PR is added to the output of S/SD and stored in the ACR.

  Note 1: The content of the ACR is accessed via the barrel-shifter and format-adjuster so that it can be transferred on the X or Y-bus during the clock cycle following ACR loading. The buses are selected by specifying LSP and/or MSP as the source for the X or Y-bus.

  Note 2: The explanation of the MPY operation is a simplified presentation of what really happens. In fact, clock cycle 1 is not just used for multiplication, but part of the accumulation as well: i.e. accumulation of the lower part of the multiplier result and the contents of the accumulator. Therefore, in the P-mode, an MPY with +ACRS or −ACRS in the MPY field (see section 3.3 on description of MPY field) that directly follows another MPY operation leads to an undefined situation where the higher part of the first multiplication/accumulation result is already required at the end of clock cycle 1, but is only ready after clock cycle 2. If it is necessary to have an MPY operation with +ACRS or −ACRS directly after a previous MPY operation (for multiprecision multiplication), then there has to be a no operation cycle (or at least no MPY operation) between them.

- **BRANCH operation** (1 or 2 clock cycles)

  Clock cycle 1:
  The branch condition is checked, the result of which can be true or false. When the result is false, the BRANCH operation is terminated. When the result is true, the program counter is loaded with the branch address.

  Clock cylce 2: (only when condition is true)
  The new instruction is fetched to the instruction register IR.

  Note: during this fetch no new operation is started.

- **LOAD IMMEDIATE operation** (1 clock cycle)

  The 16-bit data word specified in the instruction is put on the X-bus and the Y-bus and transferred to one or two specified destinations. In the case that two identical destinations are specified no transfer takes place.

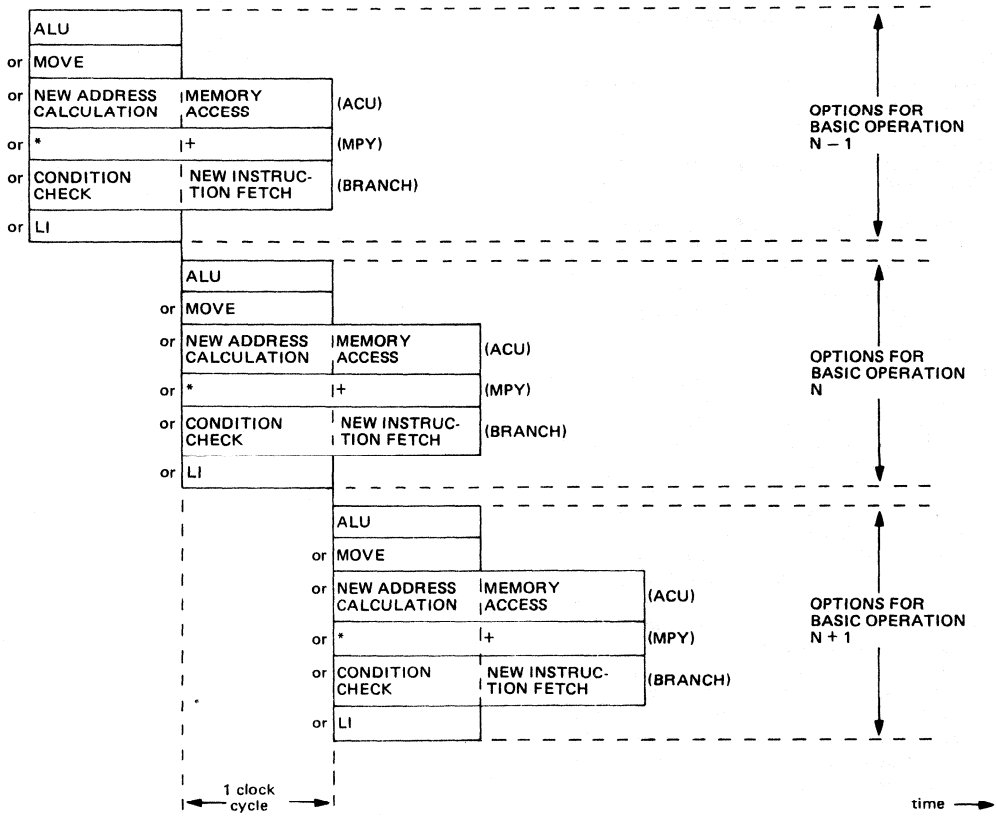


Fig. 3.1-1 Basic operation sequencing in P-mode.

Notes to Fig. 3.1-1

NOTE 1: Each instruction may contain several simultaneous basic operations (see section 3.2 on instruction formats).

NOTE 2: "New instruction fetch" (BRANCH) takes place only when the condition is true.

NOTE 3: During "New instruction fetch" (BRANCH) no new operation is started.

NOTE 4: Memory access is normally a data register (DRA, DRB, DRR, or PI) read. This read doesn't take place when there is a simultaneous MOVE to a RAM (during a RAM access).

NOTE 5: An MPY operation with +ACRS or –ACRS in the MPY field directly following another MPY operation leads to an undefined situation (see description of MPY operation).

NOTE 6: After instruction N which specifies a MOVE or LOAD IMMEDIATE operation to PC first instruction N + 1 is executed.

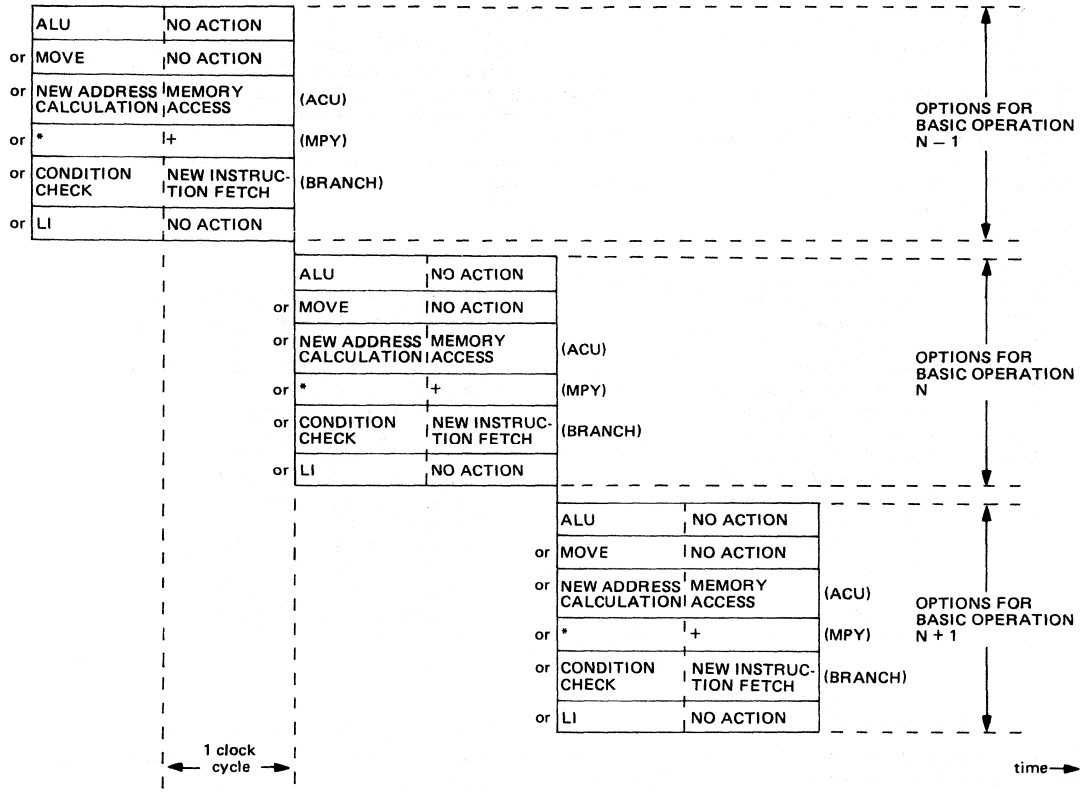


Fig. 3.1-2 Basic operation sequencing in NP-mode.

Notes to Fig. 3.1-2

NOTE 1: Each instruction may contain several simultaneous basic operations (see section 3.2 on instruction format).

NOTE 2: "New instruction fetch" (BRANCH) takes place only when the condition is true. If the condition is false, there is no action during the second clock cycle.

NOTE 3: Memory access is a data register read.

DEVELOPMENT DATA

3.2 INSTRUCTION FORMAT

All instruction words are 40-bits wide.

4 types of instructions are defined, each with their own set of basic operations:

Type 0: ALU operation + 2 MOVE operations + 3 ACU operations

Type 1: MULTIPLY operation + 2 MOVE operations + 3 ACU operations

Type 2: BRANCH operation + 3 ACU operations

Type 3: LOAD IMMEDIATE operation + 3 ACU operations.

Each basic operation is specified by the contents of one or more instruction fields (see Fig. 3.2-1).

The field at the far left of each instruction indicates the instruction type. The other fields are defined in the following table.

ALU	= Type of ALU operation	dedicated for ALU operations
AOPS	= ALU operands	dedicated for ALU operations
SX	= Source on X-bus	These fields are for ALU and/or MOVE operations,
SY	= Source on Y-bus	or for MPY and/or MOVE operations
DX	= Destination on X-bus	for MOVE or LI operations
DY	= Destination on Y-bus	for MOVE or LI operations
RFILE	= Destination in Register file	for ALU, MOVE or LI operations
ACUA	= Type of ACUA operation	dedicated for ACU operations
ACUB	= Type of ACUB operation	dedicated for ACU operations
ACUR	= Type of ACUR operation	dedicated for ACU operations
MPY	= Type of accumulator operation	dedicated for MPY operations
MOPS	= Multiply operands	dedicated for MPY operations
NAP	= Address of next instruction when condition is true	dedicated for BRANCH operations
BR	= Type of branch operation	dedicated for BRANCH operations
COND	= Branch condition	dedicated for BRANCH operations
DATA	= 16 bits data word that is transmitted on X and Y-bus	dedicated for LI operations

3.3 INSTRUCTION FIELDS

For each instruction field, the valid codes and their function are specified. For most fields, not only the function is specified but also a mnemonic. The PCB5010/11 assembly language, using the mnemonics in this data sheet, is described in a separate document.

Instruction type 0:

39	38	37 36 35 34 33	32 31	30 29 28 27 26	25 24 23 22 21	20 19 18 17	16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
0	0	ALU	AOPS	SX	SY	DX	DY	RFILE	ACUA	ACUR	ACUB

Instruction type 1:

39	38	37 36 35	34 33 32 31	30 29 28 27 26	25 24 23 22 21	20 19 18 17	16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
0	1	MPY	MOPS	SX	SY	DX	DY	RFILE	ACUA	ACUR	ACUB

Instruction type 2:

39	38	37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22	21 20 19	18 17 16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
1	0	NAP*	BR	CONDITION	0 0 0 0	ACUA	ACUR	ACUB

Instruction type 3:

39	38	37	36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21	20 19 18 17	16 15 14 13	12 11 10 9	8 7 6	5 4 3	2 1 0
1	1	0	DATA	DX	DY	RFILE	ACUA	ACUR	ACUB

* Only bits 22 to 31 are used.

Fig. 3.2-1 The four instruction types and their fields.

ALU

mnemonic	code binary	code hex	type	function
Arithmetic operations:				
ADD	10100	14	dyadic	addition
XADD	10101	15	dyadic	extended addition
SUB	10110	16	dyadic	subtraction
XSUB	10111	17	dyadic	extended subtraction
CSUB	11000	18	dyadic	conditional subtraction
NEG	01100	0C	monadic	negate
XNEG	01101	0D	monadic	extended negate
CNEG	01110	0E	monadic	conditional negate
DEC	01010	0A	monadic	decrement
XDEC	01011	0B	monadic	extended decrement
INC	01000	08	monadic	increment
XINC	01001	09	monadic	extended increment
ASL	00111	07	monadic	arithmetic shift left
XASL	00110	06	monadic	extended arithmetic shift left
ASR	00011	03	monadic	arithmetic shift right
XASR	00000	00	monadic	extended arithmetic shift right
ADDM	11010	1A	dyadic	add MSB of B to A
DIV	11001	19	dyadic	unsigned division step
XSGN	11110	1E	no operand	extended N flag
Logic operations:				
COM	10000	10	monadic	logic complement
AND	10001	11	dyadic	logic AND
OR	10010	12	dyadic	logic OR
EXOR	10011	13	dyadic	logic exclusive OR
SWAP	11100	1D	monadic	byte swap
LSL	00101	05	monadic	logic shift left
LROL	00100	04	monadic	logic rotate left
LSR	00001	01	monadic	logic shift right
LROR	00010	02	monadic	logic rotate right
Other operations:				
PASS	01111	0F	monadic	pass with flag update
NULL	11101	1D	no operand	generate 0
–	11111	1F	–	reserved
–	11011	1B	–	reserved

AOPS

mnemonic	code binary	code hex	ALU-type	A-operand	B-operand
*, *	00	0	dyadic	source on X-bus	source on Y-bus
AAL, *	01	1	dyadic	AAL	source on Y-bus
*, ABL	10	2	dyadic	source on X-bus	ABL
AAL, ABL	11	3	dyadic	AAL	ABL
AAL	00	0	monadic	AAL	–
(the operation is undefined when this operand is selected with a SWAP operation)					
*	01	1	monadic	source on X-bus	–
*	10	2	monadic	source on Y-bus	–
–	11	3	–	reserved	–

Note: the AOPS field has no meaning when a no operand operation is specified in the ALU field and as there is no operation, AAL and ABL retain their values.

* The mnemonic of the particular source is used (see SX and SY fields).

SX

mnemonic	code binary	code hex	full name of source
–	00000	00	no source
ROM	00001	01	data register DRR
–	00010	02	reserved
TOS	00011	03	top of stack (Note 1)
RX	00100	04	bussave register X
PI	00101	05	parallel data input register
IOF	00110	06	input/output status and user flag register
SOX	00111	07	serial output register connected to X-bus
SIX	01000	08	serial input register connected to X-bus
SIOST	01001	09	serial I/O control register
–	01010	0A	reserved
RAMB	01011	0B	data register DRB
PST	01100	0C	processor status register
RAMA	01101	0D	data register DRA
ACU(RAMB)	01110	0E	address register ARB
LSP	01111	0F	least significant 16 bits of multiply/shift/adjust result
MSP	10000	10	most significant 16 bits of multiply/shift/adjust result
R1	10001	11	register 1
R2	10010	12	register 2
R3	10011	13	register 3
R4	10100	14	register 4
R5	10101	15	register 5
R6	10110	16	register 6
R7	10111	17	register 7
R8	11000	18	register 8
R9	11001	19	register 9
R10	11010	1A	register 10
R11	11011	1B	register 11
R12	11100	1C	register 12
R13	11101	1D	register 13
R14	11110	1E	register 14
R15	11111	1F	register 15

Note 1: When TOS is used as a source, the stack is popped one level.

SY

mnemonic	code binary	code hex	full name of source
–	00000	00	no source
RAMB	00001	01	data register DRB
–	00010	02	reserved
RAMA	00011	03	data register DRA
RY	00100	04	bussave register Y
ROM	00101	05	data register DRR
SIY	00110	06	serial input register connected to Y-bus
–	00111	07	reserved
PG	01000	08	page register
BSR	01001	09	barrel-shifter/format adjuster control register
ACU(ROM)	01010	0A	address register ARR
ACU(RAMA)	01011	0B	address register ARA
PST	01100	0C	processor status register
PI	01101	0D	parallel data input register
SOY	01110	0E	serial output register connected to Y-bus
LSP	01111	0F	least significant 16 bits of multiply/shift/adjust result
MSP	10000	10	most significant 16 bits of multiply/shift/adjsut result
R1	10001	11	register 1
R2	10010	12	register 2
R3	10011	13	register 3
R4	10100	14	register 4
R5	10101	15	register 5
R6	10110	16	register 6
R7	10111	17	register 7
R8	11000	18	register 8
R9	11001	19	register 9
R10	11010	1A	register 10
R11	11011	1B	register 11
R12	11110	1C	register 12
R13	11101	1D	register 13
R14	11110	1E	register 14
R15	11111	1F	register 15

DX

mnemonic	code binary	code hex	full name of destination
–	0000	0	no destination
FQR	0001	1	FQR bit in PST; the required value for FQR must be present in bit 15 on the bus; the other bits are don't cares
SIOST	0010	2	serial I/O control register
RPO	0011	3	second parallel data output buffer (PCB5011 only)
RX	0100	4	bussave register X
PC	0101	5	program counter
SOX	0110	6	serial output register connected to X-bus
PRAM	0111	7	program RAM (PCB5010 only)
–	1000	8	reserved
RPR	1001	9	instruction repeat register
PO	1010	A	parallel data output buffer
RAMA	1011	B	RAMA
PST	1100	C	processor status register
TOS	1101	D	top of stack (Note 1)
ACU(RAMB,*)	1110	E	ACUB
**	1111	F	register file

* fill in a mnemonic of the ACU-initialization field.
** fill in a mnemonic of the RFILE field.

Note 1: When TOS is used as a destination, the stack is pushed one level.

DY

mnemonic	code binary	code hex	full name of destination
–	0000	0	no destination
BSR	0001	1	barrel-shifter/format adjuster control register
–	0010	2	reserved
RAMB	0011	3	RAMB
–	0100	4	reserved
RY	0101	5	bussave register Y
–	0110	6	reserved
–	0111	7	reserved
–	1000	8	reserved
PG	1001	9	page register
ACU(RAMA,*)	1010	A	ACUA
PO	1011	B	parallel data output buffer
RPO	1100	C	second parallel data output buffer (PCB5011 only)
SOY	1101	D	serial output register connected to Y-bus
ACU(ROM,*)	1110	E	ACUR
**	1111	F	register file

* fill in a mnemonic of the ACU-initialization field.
** fill in a mnemonic of the RFILE field.

RFILE

mnemonic	code binary	code hex	full name of destination
–	0000	0	no destination
R1	0001	1	register 1
R2	0010	2	register 2
R3	0011	3	register 3
R4	0100	4	register 4
R5	0101	5	register 5
R6	0110	6	register 6
R7	0111	7	register 7
R8	1000	8	register 8
R9	1001	9	register 9
R10	1010	A	register 10
R11	1011	B	register 11
R12	1100	C	register 12
R13	1101	D	register 13
R14	1110	E	register 14
R15	1111	F	register 15

ACU

The ACU fields for RAMA, RAMB and ROM are identical. The content of the field has a different meaning if it is for ACU initialization or address computation.

ACU INITIALIZATION

mnemonic	code binary	code hex	New values for: AR	A	S	M
AR	000	0	source	A	S	M
AAR	001	1	source	source	S	M
SAR	010	2	source	A	source	M
A	011	3	AR	source	S	M
S	100	4	AR	A	source	M
M	101	5	AR	A	S	source
ASAR	110	6	source	source	source	M
AR1M	111	7	(source)!M	A	S	M

ADDRESS COMPUTATION

mnemonic	code binary	code hex	New values for: AR	A	S	M
	000	0	AR	A	S	M
INCA	001	1	(A+1)!M	(A+1)!M	S	M
DECA	010	2	(A–1)!M	(A–1)!M	S	M
STEP	011	3	(A+S)!M	(A+S)!M	S	M
INCS	100	4	(S+1)!M	A	(S+1)!M	M
A	101	5	(A)!M	A	S	M
S	110	6	(S)!M	A	S	M
REV	111	7	br(A+S)	A+S	S	M

Note: see section 2.3.2 on ACUs and PG register for explanation of !M and br(. . . .).

MPY

mnemonic	code binary	code hex	new ACR-value
–	000	0	ACR (HOLD)
0	001	1	P*Q
+ACR	010	2	P*Q + ACR
–ACR	011	3	P*Q – ACR
+ACRS	100	4	P*Q + ACR x 2^{-15}
–ACRS	101	5	P*Q – ACR x 2^{-15}
	other		reserved

MOPS

mnemonic	code binary	code hex	P-input of multiplier	Q-input of multiplier
*, *	0000	0	source on X-bus	source on Y-bus
, –	0001	1	source on X-bus	–(source on Y-bus)
MXL,*	0010	2	MXL	source on Y-bus
MXL, –*	0011	3	MXL	–(source on Y-bus)
*, MYL	0100	4	source on X-bus	MYL
MXL, MYL	0101	5	MXL	MYL
–1, –*	0110	6	–1	–(source on Y-bus)
–1, *	0111	7	–1	source on Y-bus
–1, MYL	1000	8	–1	MYL
	other		reserved	reserved

Note: When the MPY-field contains 000, then independent of the MOPS-code the following is true:

mnemonic	code	P-input of multiplier	Q-input of multiplier
–	XXXX	MXL	MYL

* Fill in the mnemonic of the particular source (see SX and SY fields).

NAP

The NAP field contains the address of the next instruction to be executed if a branch condition is true.

BR

mnemonic	code binary	code hex	function
GOTO	000	0	goto
CALL	001	1	subroutine call
RET	010	2	return from subroutine
RETI	100	4	return $\overline{\text{INT}}$ interrupt
	other		reserved

DEVELOPMENT DATA

COND

mnemonic	code binary	code hex(X=0)	condition	mnemonic explanation
–	00000X	00	always true	
AN	00001X	02	SGNM = 1	accumulator negative
XO	00010X	04	OOR = 1	
–	00011X	06	reserved	
GE or NOT LT	00100X	08	$\overline{\text{N.EXOR.V}}$ = 1	greater or equal to/not less than
NOT GT or LE	00101X	0A	(N.EXOR.V).OR.Z = 1	not greater than/less than or equal to
IFX	00110X	0C	IFA.AND.IFB.AND.IFC.AND.IFD = 1	
HI or NOT LS	00111X	0E	$\overline{\text{C.OR.Z}}$ = 1	higher/not less than or equal to
OFL	01000X	10	OORL.OR.VL = 1	system overflow
XOL	01001X	12	OORL = 1	extractor overflow
AOL	01010X	14	OVFL = 1	accumulator overflow
VL	01011X	16	VL = 1	
Z or EQ	01100X	18	Z = 1	
N	01101X	1A	N = 1	
C	01110X	1C	C = 1	
V	01111X	1E	V = 1	
SIX	10000X	20	SIXACK = 1	
SOX	10001X	22	SOXACK = 1	
SIY	10010X	24	SIYACK = 1	
SOY	10011X	26	SOYACK = 1	
ACU(RAMA)	10100X	28	ACA = 1	
ACU(RAMB)	10101X	2A	ACB = 1	
ACU(ROM)	10110X	2C	ACR = 1	
–	10111X	2E	reserved	
IFA	11000X	30	IFA = 1	
IFB	11001X	32	IFB = 1	
IFC	11010X	34	IFC = 1	
IFD	11011X	36	IFD = 1	
–	11100X	38	reserved	
–	11101X	3A	reserved	
–	11110X	3C	reserved	
–	11111X	3E	reserved	

X = 0: branch takes place when condition = true
X = 1: branch takes place when condition = false

Note: the mnemonic names GE, LT, GT, LE, HI, and LS refer to situations where the flag setting is a result of a subtraction (SUB) of operands A and B. For example, GE means that A is greater than or equal to B.

DATA

Data is a 16 bit data word which is transmitted on the X and Y-bus.

4.0 ELECTRICAL SPECIFICATION

4.1 ABSOLUTE MAXMIMUM RATINGS

symbol	parameter	condition	min.	max.	unit
V_{DD}	supply voltage		−0.3	+7	V
V_I	voltage at any input		−0.3	+7	V
T_{amb}	operating ambient temperature range	PCB5010/11 PCF5010/11	0 −40	+70 +85	°C °C
T_{stg}	storage temperature range		−55	+150	°C

4.2 DC CHARACTERISTICS

T_{amb} = 0 to +70 °C; V_{DD} = 5 V

symbol	parameter	condition	min.	typ.	max.	unit
V_{DD}	supply voltage		4.75	5.0	5.25	V
V_{IH}	HIGH level input voltage		2	–	V_{DD}+0.3	V
V_{IL}	LOW level input voltage		−0.3	–	+0.8	V
V_{OH}	HIGH level output voltage	V_{DD} = 4.75 V I_{OH} = 100 µA	2.4	–	–	V
V_{OL}	LOW level output voltage	V_{DD} = 4.75 V I_{OL} = 2 mA	–	–	0.4	V
I_{IH}	HIGH level input current		–	–	10	µA
$-I_{IL}$	LOW level input current		–	–	100	µA
I_{OH}	HIGH level output current		–	–	100	µA
I_{OL}	LOW level output current		–	–	2	mA
C_I	input pin capacitance		–	–	tbf	pF
C_O	output pin capacitance		–	–	tbf	pF
P	power dissipation		–	–	tbf	mW

Note: All inputs not connected are pulled up to HIGH level.

DEVELOPMENT DATA

4.3 AC CHARACTERISTICS

no.	parameter	min.	max.	unit	note
1	CLK width HIGH	62,5	1000	ns	
2	CLK width LOW	62,5	1000	ns	
3	CLK HIGH to SYNC HIGH	20	50	ns	
4	CLK HIGH to Ax valid	20	60	ns	x = 0 . . . 15
5	CLK HIGH to R/$\overline{W}$ LOW	20	85	ns	
6	R/$\overline{W}$ width LOW	120		ns	
7	CLK LOW to $\overline{DS}$ LOW	20	50	ns	
8	CLK HIGH to $\overline{DS}$ HIGH	20	50	ns	
9	Dx set-up time	15		ns	x = 0 . . . 15
10	Dx hold time	0		ns	x = 0 . . . 15
11	Dx valid to $\overline{DS}$ LOW	0		ns	x = 0 . . . 15
12	$\overline{DS}$ HIGH to Dx invalid	15		ns	x = 0 . . . 15
13	$\overline{WAIT}$ set-up time	10		ns	
14	$\overline{WAIT}$ hold time	30		ns	
15	$\overline{INT}$ set-up time	5		ns	
16	$\overline{INT}$ hold time	30		ns	
17	CLK HIGH to $\overline{IACK}$ LOW		60	ns	
18	CLK HIGH to $\overline{IACK}$ HIGH		60	ns	
19	IFA, IFB, IFC, IFD set-up time	5		ns	
20	IFA, IFB, IFC, IFD hold time	30		ns	
21	$\overline{RST}$ set-up time	10		ns	
22	$\overline{RST}$ hold time	30		ns	
24	CLK HIGH to PAx or ARRx valid	20	60	ns	x = 0 . . 9 or . . 8
25	CLK HIGH to RR/$\overline{W}$ LOW	20	85	ns	
26	RR/$\overline{W}$ width LOW	120		ns	
27	CLK LOW to $\overline{RDS}$ LOW	20	50	ns	
28	CLK HIGH to $\overline{RDS}$ HIGH	20	50	ns	
29	RDx set-up time	15		ns	x = 0 . . . 15
30	RDx hold time	0		ns	x = 0 . . . 15
31	RDx valid to $\overline{RDS}$ LOW	0		ns	x = 0 . . . 15
32	$\overline{RDS}$ HIGH to RDx invalid	15		ns	x = 0 . . . 15
41	COX, CIX, COY, CIY width HIGH	125		ns	
42	COX, CIX, COY, CIY width LOW	125		ns	
43	COX(Y) LOW to $\overline{SOX(Y)RQ}$ LOW		40	ns	
44	COX(Y) LOW to $\overline{SOX(Y)RQ}$ HIGH		40	ns	
45	$\overline{SOX(Y)EN}$ set-up time	40		ns	
46	$\overline{SOX(Y)EN}$ hold time	40		ns	
47	COX(Y) LOW to next DOX(Y) valid		40	ns	
48	$\overline{SOX(Y)EN}$ LOW to DOX(Y) valid	10		ns	
49	$\overline{SOX(Y)EN}$ HIGH to DOX(Y) 3-state		40	ns	
53	CIX(Y) LOW to $\overline{SIX(Y)RQ}$ LOW		40	ns	
54	CIX(Y) LOW to $\overline{SIX(Y)RQ}$ HIGH		40	ns	
55	$\overline{SIX(Y)EN}$ set-up time	30		ns	
56	$\overline{SIX(Y)EN}$ hold time	10		ns	
57	DIX, DIY set-up time	10		ns	
58	DIX, DIY hold time	40		ns	
59	PDx set-up time	5		ns	x = 0 . . . 39
60	PDx hold time	30		ns	x = 0 . . . 39

Note: For each device, values are all min. or all max. .

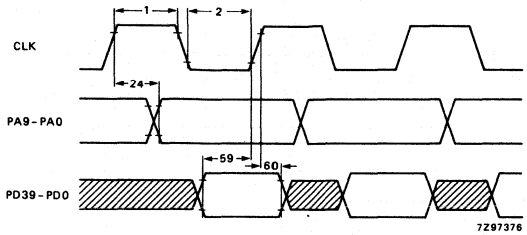


Fig. 4.3-1 Program memory access timing (for PCB5011 only).

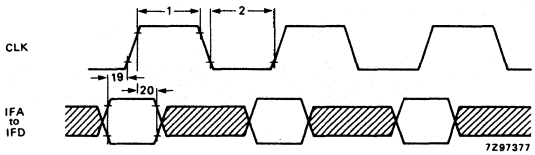


Fig. 4.3-2 User flag timing.

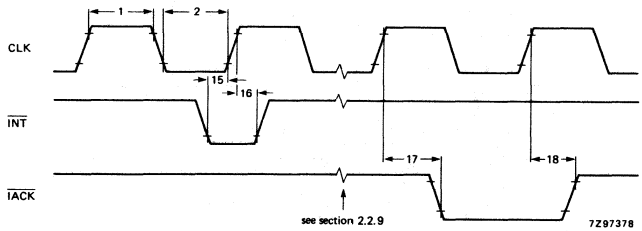


Fig. 4.3-3 Interrupt timing.

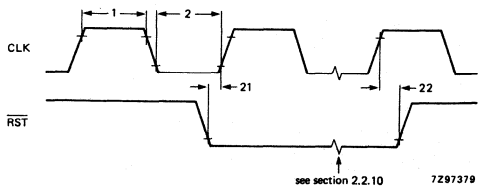


Fig. 4.3-4 Reset timing.

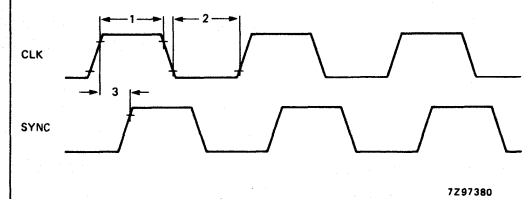


Fig. 4.3-5 Synchronization timing.

DEVELOPMENT DATA

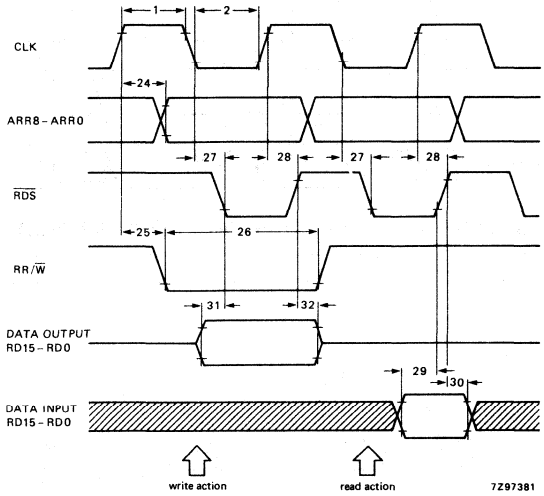
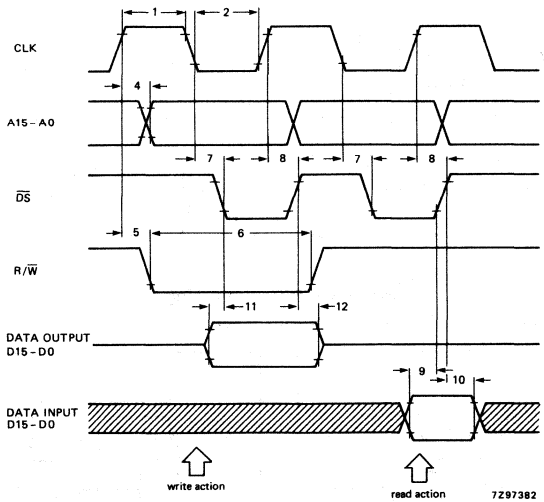
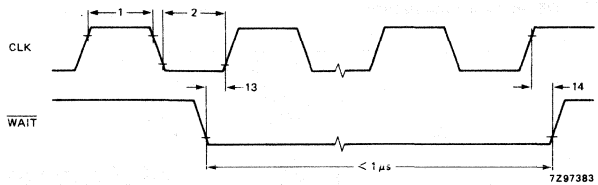


Fig. 4.3-6 Second parallel I/O timing (for PCB5011 only).



Note: (part of) the signals A15 – A0 can be used just as hardware controlling outputs if they are not needed for addressing external RAM.

Fig. 4.3-7 Parallel I/O timing ($\overline{\text{WAIT}}$ inactive).



Note: as long as $\overline{WAIT}$ = 0 all clocked (by CLK) processor actions are suspended i.e. the internal status and all signals remain unchanged.

Fig. 4.3-8 $\overline{WAIT}$ signal timing.

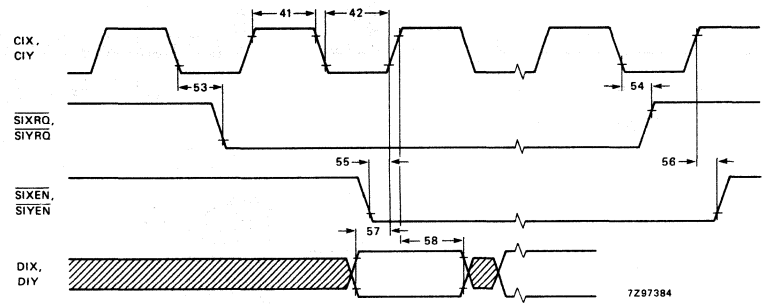


Fig. 4.3-9 Serial input timing.

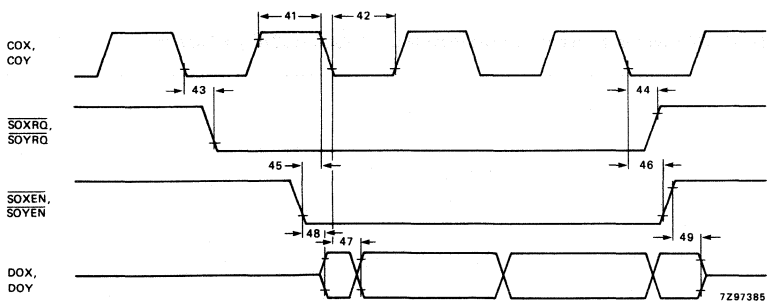


Fig. 4.3-10 Serial output timing.

5.0 PACKAGE OUTLINES

5.1 PCB5010 PACKAGE OUTLINE (dimensions in mm)

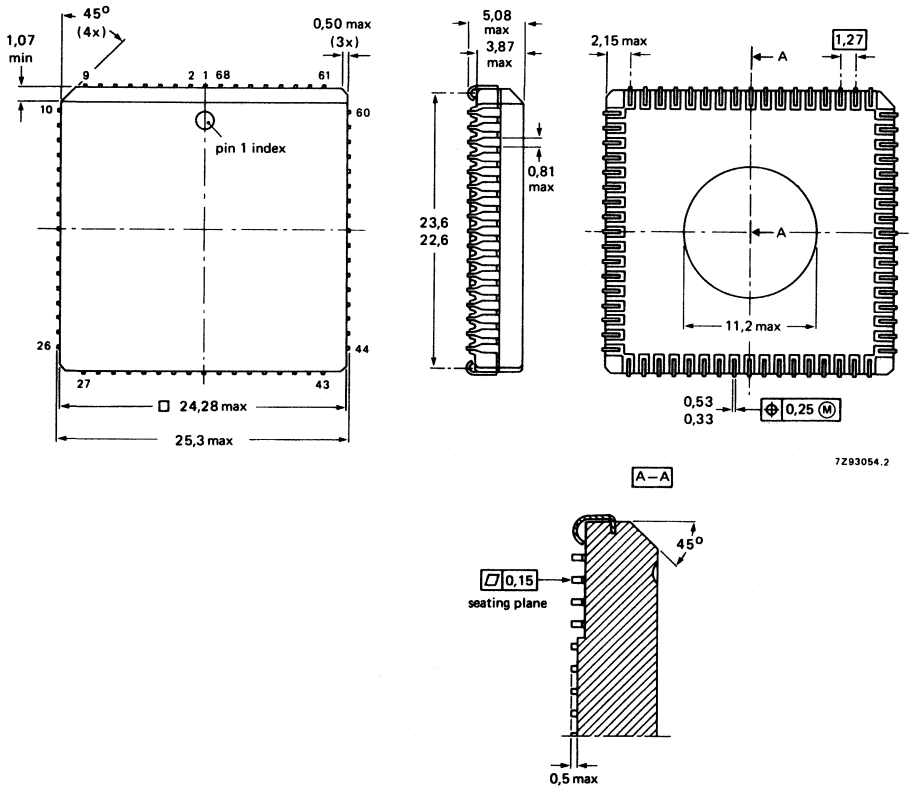


Fig. 5.1-1 68-lead plastic leaded-chip-carrier (PLCC) (SOT-188A) package for the PCB5010.

DEVELOPMENT DATA

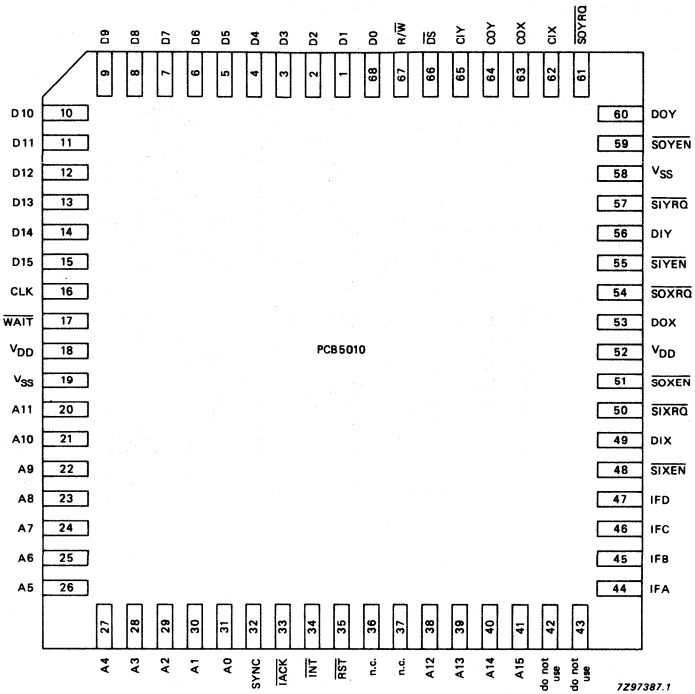


Fig. 5.1-2 Pinning for the PCB5010 (PLCC).

5.2 PCB5011 PACKAGE OUTLINE (dimensions in mm)

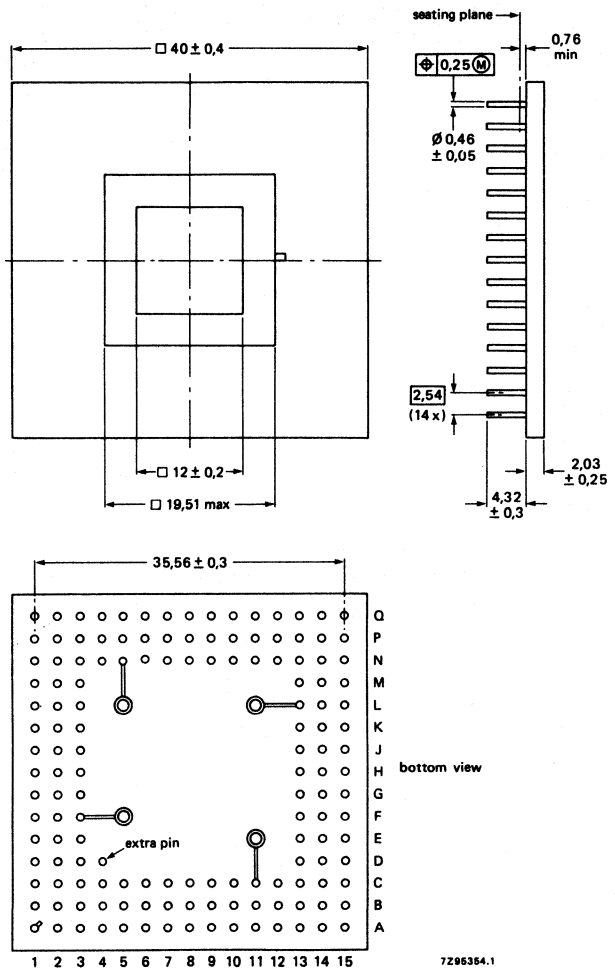


Fig. 5.2-1 144-pin grid array (PGA) package for the PCB5011.

DEVELOPMENT DATA

5.3 PIN ASSIGNMENT FOR Fig. 5.2-1

PCB5011 signal name	pin number
V_{DD}	N8, C8
V_{SS}	N9, A2
CLK	Q2
(do not use)	B3
$\overline{RST}$	L14
D15	P3
D14	N4
D13	Q1
D12	P2
D11	N3
D10	M3
D9	P1
D8	N2
D7	L3
D6	M2
D5	N1
D4	M1
D3	L2
D2	L1
D1	K3
D0	K2
A15	A1
A14	B2
A13	C3
A12	C4
A11	N5
A10	Q3
A9	P5
A8	Q4
A7	N6
A6	P6
A5	Q5
A4	P7
A3	N7
A2	Q6
A1	Q7
A0	P8
R/$\overline{W}$	J2
$\overline{DS}$	K1
$\overline{WAIT}$	P4
DIX	B1

PCB5011 signal name	pin number
$\overline{SIXEN}$	C2
$\overline{SIXRQ}$	D2
CIX	D3
DIY	H3
$\overline{SIYEN}$	J3
$\overline{SIYRQ}$	H1
CIY	J1
DOX	C1
$\overline{SOXEN}$	E2
$\overline{SOXRQ}$	E3
COX	D1
DOY	G1
$\overline{SOYEN}$	F1
$\overline{SOYRQ}$	H2
COY	G3
$\overline{INT}$	M15
$\overline{IACK}$	M14
SYNC	N14
IFA	F3
IFB	F2
IFC	E1
IFD	G2
PA9	Q13
PA8	P12
PA7	N11
PA6	P13
PA5	Q14
PA4	N12
PA3	N13
PA2	P14
PA1	Q15
PA0	M13

(continued on next page)

PCB5011 signal name	pin number
PD39	C5
PD38	B4
PD37	A3
PD36	A4
PD35	B5
PD34	A5
PD33	C6
PD32	B6
PD31	B7
PD30	A6
PD29	A7
PD28	C7
PD27	A8
PD26	B8
PD25	A9
PD24	A10
PD23	C9
PD22	B9
PD21	A11
PD20	B10
PD19	C10
PD18	A12
PD17	B11
PD16	A13
PD15	C11
PD14	B12
PD13	A14
PD12	B13
PD11	C12
PD10	G15
PD9	G13
PD8	K14
PD7	L15
PD6	J14
PD5	J13
PD4	K15
PD3	J15
PD2	H14
PD1	H15
PD0	H13
ARR8	Q8
ARR7	Q9
ARR6	Q10
ARR5	P9
ARR4	P10
ARR3	N10
ARR2	Q11
ARR1	P11
ARR0	Q12

PCB5011 signal name	pin number
RD15	F15
RD14	G14
RD13	F14
RD12	F13
RD11	E15
RD10	E14
RD9	D15
RD8	C15
RD7	D14
RD6	E13
RD5	C14
RD4	B15
RD3	D13
RD2	C13
RD1	B14
RD0	A15
RR/$\overline{W}$	L13
$\overline{RDS}$	N15

APPENDIX A

PCB5010/PCB5011 INSTRUCTION SUMMARY

Type 0 instructions: ALU/MOVE/ADDRESS COMPUTATION

TY	ALU			AOPS			SX		SY		DX		DY		RFILE		ACUA		ACUR		ACUB	
	mnemonic	m/d	hex code	mnemonic	m/d	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
	ADD	d	14	SX,SY	d	0	–	00	–	00	–	0	–	0	–	0	**DY=A**		**DY=E**		**DX=E**	
0	XADD	d	15	AAL,SY	d	1	ROM	01	RAMB	01	FQR	1	BSR	1	R1	1	AR	0	AR	0	AR	0
	SUB	d	16	SX,ABL	d	2	–	02	–	02	SIOST	2	–	2	R2	2	AAR	1	AAR	1	AAR	1
	XSUB	d	17	AAL,ABL	d	3	TOS	03	RAMA	03	RPO	3	RAMB	3	R3	3	SAR	2	SAR	2	SAR	2
	CSUB	d	18				RX	04	RY	04	–	4	–	4	R4	4	A	3	A	3	A	3
	NEG	m	0C	AAL	m	0	PI	05	ROM	05	PC	5	RY	5	R5	5	S	4	S	4	S	4
	XNEG	m	0D	(ext/SWAP)			IOF	06	SIY	06	SOX	6	–	6	R6	6	M	5	M	5	M	5
	CNEG	m	0E	SX	m	1	SOX	07	–	07	PRAM	7	–	7	R7	7	ASAR	6	ASAR	6	ASAR	6
	DEC	m	0A	SY	m	2	SIX	08	PG	08	–	8	–	8	R8	8	AR1M	7	AR1M	7	AR1M	7
	XDEC	m	0B	–	–	3	SIOST	09	BSR	09	RPR	9	PG	9	R9	9						
	INC	m	08				–	0A	ACU(ROM)	0A	P0	A	ACU(RAMA)	A	R10	A	**DY≠A**		**DY≠E**		**DX≠E**	
	XINC	m	09				RAMB	0B	ACU(RAMA)	0B	RAMA	B	P0	B	R11	B	–	0	–	0	–	0
	ASL	m	07				PST	0C	PST	0C	PST	C	RPO	C	R12	C	INCA	1	INCA	1	INCA	1
	XASL	m	06				RAMA	0D	PI	0D	TOS	D	SOY	D	R13	D	DECA	2	DECA	2	DECA	2
	ASR	m	03				ACU(RAMB)	0E	SOY	0E	ACU(RAMB)	E	ACU(ROM)	E	R14	E	STEP	3	STEP	3	STEP	3
	XASR	m	00				LSP	0F	LSP	0F	RFILE	F	RFILE	F	R15	F	INCS	4	INCS	4	INCS	4
	ADDM	d	1A				MSP	10	MSP	10							A	5	A	5	A	5
	DIV	d	19				R1	11	R1	11							S	6	S	6	S	6
	XSGN	–	1E				R2	12	R2	12							REV	7	REV	7	REV	7
	COM	m	10				R3	13	R3	13												
	AND	d	11				R4	14	R4	14												
	OR	d	12				R5	15	R5	15												
	EXOR	d	13				R6	16	R6	16												
	SWAP	m	1C				R7	17	R7	17												
	LSL	m	05				R8	18	R8	18												
	LROL	m	04				R9	19	R9	19												
	LSR	m	01				R10	1A	R10	1A												
	LROR	m	02				R11	1B	R11	1B												
	PASS	m	0F				R12	1C	R12	1C												
	NULL	–	1D				R13	1D	R13	1D												
	–	–	1B				R14	1E	R14	1E												
	–	–	1F				R15	1F	R15	1F												

Type 1 instructions: MPY/MOVE/ADDRESS COMPUTATION

TY	MPY		MOPS		SX		SY		DX		DY		RFILE		ACUA		ACUR		ACUB	
	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
	–	0	SX,SY	0																
1	0	1	SX,–SY	1																
	+ACR	2	MXL,SY	2																
	–ACR	3	MXL,–SY	3																
	+ACRS	4	SX,MYL	4	as above		as above		as above		as above		as above		as above		as above		as above	
	–ACRS	5	MXL,MYL	5																
			–1,–SY	6																
			–1,SY	7																
			–1,MYL	8																

Type 2 instructions: BRANCH/ADDRESS COMPUTATION

TY	NAP	BR		CONDITION		CONDITION		ACUA		ACUR		ACUB	
		mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
2	address of next instruction if condition matches	GOTO	0	–	00	–	01	as above		as above		as above	
		CALL	1	AN	02	NOT AN	03						
		RET	2	X0	04	NOT X0	05						
		RETI	4	–	06	–	07						
				GE	08	LT	09						
				LE	0A	GT	0B						
				IFX	0C	NOT IFX	0D						
				HI	0E	LS	0F						
				OFL	10	NOT OFL	11						
				XOL	12	NOT XOL	13						
				AOL	14	NOT AOL	15						
				VL	16	NOT VL	17						
				Z	18	NOT Z	19						
				N	1A	NOT N	1B						
				C	1C	NOT C	1D						
				V	1E	NOT V	1F						
				SIX	20	NOT SIX	21						
				SOX	22	NOT SOX	23						
				SIY	24	NOT SIY	25						
				SOY	26	NOT SOY	27						
				ACU(RAMA)	28	NOT ACU(RAMA)	29						
				ACU(RAMB)	2A	NOT ACU(RAMB)	2B						
				ACU(ROM)	2C	NOT ACU(ROM)	2D						
				–	2E	–	2F						
				IFA	30	NOT IFA	31						
				IFB	32	NOT IFB	33						
				IFC	34	NOT IFC	35						
				IFD	36	NOT IFD	37						

Type 3 instructions: LOAD IMMEDIATE/ADDRESS COMPUTATION

TY	DATA	DX		DY		RFILE		ACUA		ACUR		ACUB	
		mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code	mnemonic	hex code
3	16-bit data transferred to both X and Y buses	as above		as above		as above		as above		as above		as above	

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C552 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C552 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C552" is used to refer to both family members:

- PCB83C552: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C552: ROM-less version of the PCB83C552

This I/O intensive device provides architectural enhancements to function as a controller in the field of automotive electronics, specifically engine management and gear box control.

The PCB83C552 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, six 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), an additional 16-bit timer coupled to capture and compare latches, a fifteen-source, two-priority-level, nested interrupt structure, an 8-input ADC, a dual DAC pulse width modulated interface, two serial interfaces (UART and I^2C-bus), a 'watchdog' timer and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C552 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

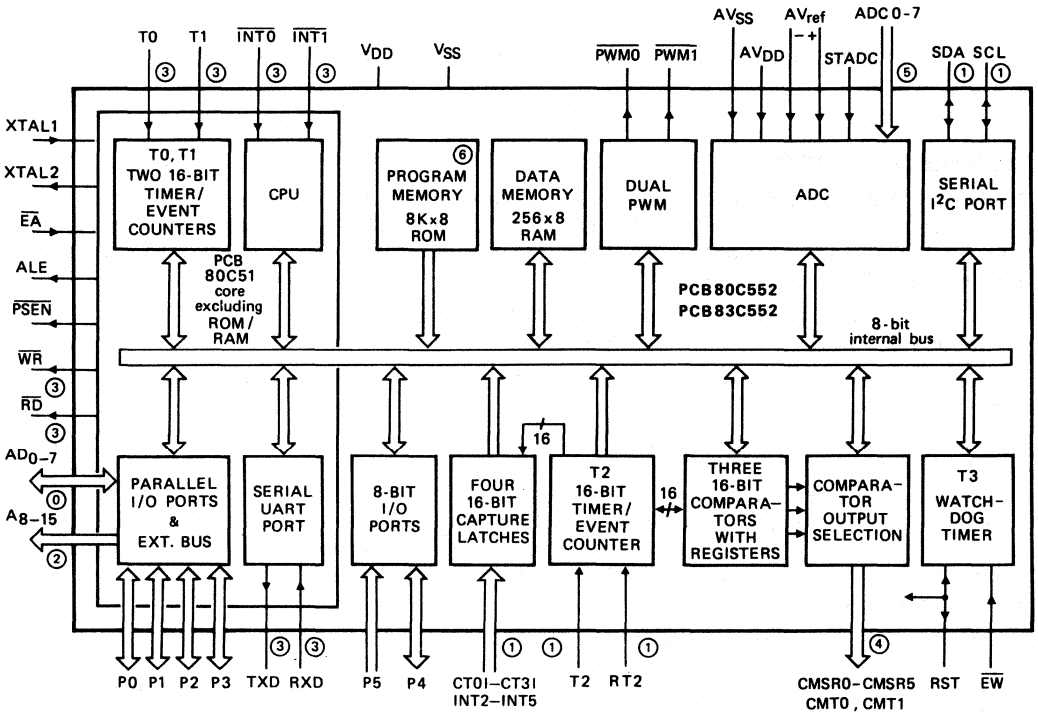
Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- An additional 16-bit timer/counter coupled to four capture registers and three compare registers
- A 10-bit ADC with 8 multiplexed analogue inputs
- Two 8-bit resolution, Pulse Width Modulated outputs
- Five 8-bit I/O ports plus one 8-bit input port shared with analogue inputs
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART compatible with the standard PCB80C51
- On-chip watchdog timer

- **A version for extended temperature range is in preparation**

PACKAGE OUTLINES

PCB83C552; PCB80C552: 68-lead plastic leaded-chip-carrier (PLCC) (SOT188 pedestal or SOT188AA pocket versions, these are interchangeable).



⓪ alternative function of port 0
① alternative functions of port 1
② alternative function of port 2
③ alternative function of port 3
④ alternative function of port 4
⑤ alternative function of port 5
⑥ not present in PCB80C552

7Z97647.5

POWER SUPPLY
V_{DD} + 5 V MAIN SUPPLY
V_{SS} GROUND

Fig. 1 Block diagram.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The PCB83C652 single-chip 8-bit microcontroller is manufactured in an advanced CMOS process and is a derivative of the PCB80C51 microcontroller family. The PCB83C652 has the same instruction set as the PCB80C51. Two versions of the derivative exist although the generic term "PCB83C652" is used to refer to both family members:

- PCB83C652: 8 K bytes mask-programmable ROM, 256 bytes RAM
- PCB80C652: ROM-less version of the PCB83C652

This device provides architectural enhancements that make it applicable in a variety of applications in general control systems.

The PCB83C652 contains a non-volatile 8 K x 8 read-only program memory, a volatile 256 x 8 read/write data memory, four 8-bit I/O ports, two 16-bit timer/event counters (identical to the timers of the 80C51), a multi-source, two-priority-level, nested interrupt structure, an I^2C interface, UART and on-chip oscillator and timing circuits. For systems that require extra capability, the PCB83C652 can be expanded using standard TTL compatible memories and logic.

The device also functions as an arithmetic processor having facilities for both binary and BCD arithmetic plus bit-handling capabilities. The instruction set consists of over 100 instructions: 49 one-byte, 45 two-byte and 17 three-byte. With a 12 MHz crystal, 58% of the instructions are executed in 1 μs and 40% in 2 μs. Multiply and divide instructions require 4 μs.

Features

- 80C51 central processing unit
- 8 K x 8 ROM, expandable externally to 64 K bytes
- 256 x 8 RAM, expandable externally to 64 K bytes
- Two standard 16-bit timer/counters
- Four 8-bit I/O ports
- I^2C-bus serial I/O port with byte orientated master and slave functions
- Full-duplex UART facilities
  Three temperature ranges available
  0 to + 70 °C; PCB83C652 versions
  −40 to + 85 °C; PCF83C652 versions
  −40 to + 110 °C; PCA83C652 versions
- Extended frequency range: 1.2 MHz to 12 MHz

PACKAGE OUTLINES

PCA/PCB/PCF83C652P; PCA/PCB/PCF80C652P: 40-lead DIL; plastic (SOT129).
PCA/PCB/PCF83C652WP; PCA/PCB/PCF80C652WP: 44-lead plastic leaded-chip-carrier (PLCC) (SOT187 pedestal or SOT187AA pocket versions, these are interchangeable).
PCA/PCB/PCF83C652H; PCA/PCB/PCF80C652H: 44-lead quad flat-pack (QFP). This is in preparation.

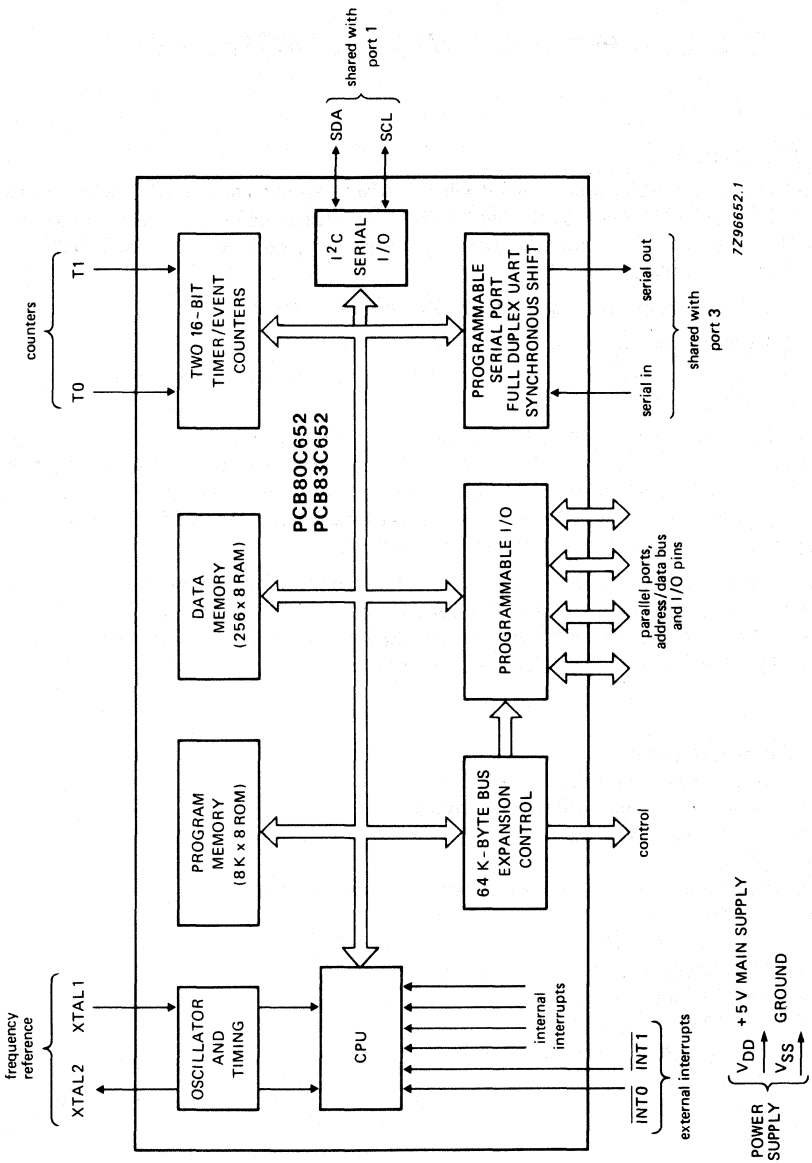


Fig. 1 Block diagram.

DTMF/MODEM/MUSICAL-TONE GENERATORS

GENERAL DESCRIPTION

The PCD3311 and PCD3312 are single-chip silicon gate CMOS integrated circuits. They are intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The devices can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With their on-chip voltage reference the PCD3311 and PCD3312 provide constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the devices provide 12 MODEM frequencies (300 to 1200 bits per second) used in simplex MODEM applications and two octaves of musical scale in steps of semitones.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)
- MODEM and melody tone generators

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	1,2	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	−25	–	dB
Operating ambient temperature range	T_{amb}	−25	–	+70	°C

PACKAGE OUTLINES

PCD3311P: 14-lead DIL; plastic (SOT27).
PCD3311T: 16-lead mini-pack; plastic (SO16L; SOT162A).
PCD3312P: 8-lead DIL; plastic (SOT97).
PCD3312T: 8-lead mini-pack; plastic (SO8L; SOT176).

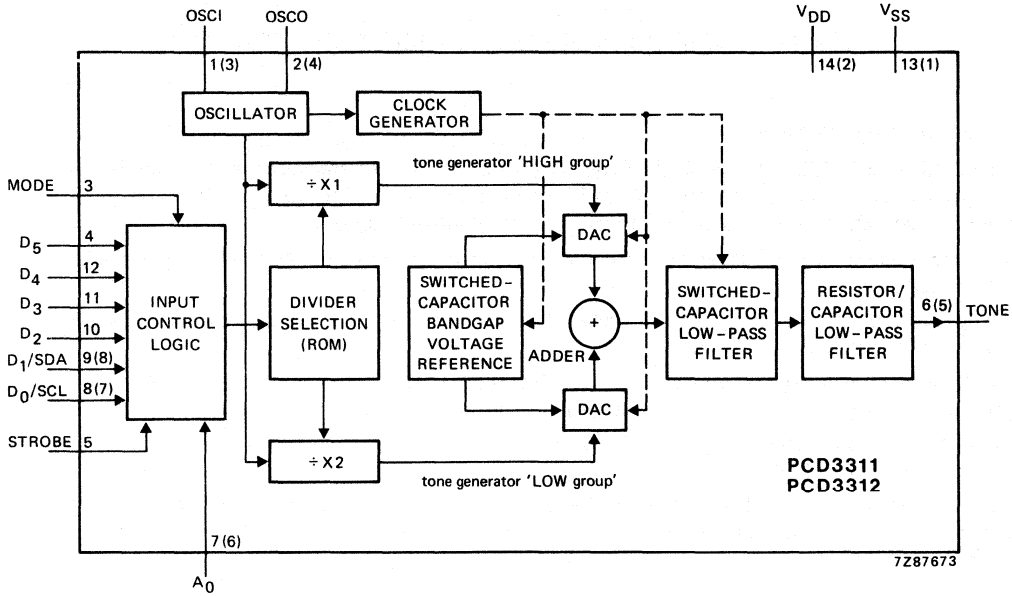


Fig. 1 Block diagram; the pin numbers in parenthesis refer to the PCD3312.

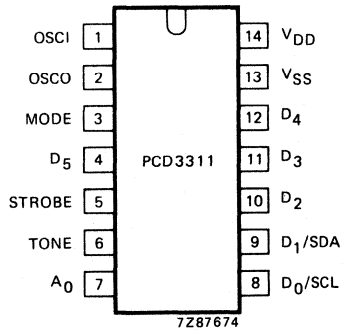


Fig. 2 Pinning diagram for the PCD3311.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D_5	parallel data input*
5	STROBE	strobe input; used for the loading of data in the parallel mode
6	TONE	frequency output for single or dual tones
7	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
8	D_0/SCL	parallel data input* or serial clock line (I^2C bus)
9	D_0/SDA	parallel data input* or serial data line (I^2C) bus)
10	D_2	parallel data inputs*
11	D_3	
12	D_4	
13	V_{SS}	negative supply
14	V_{DD}	positive supply

* MODE = HIGH.

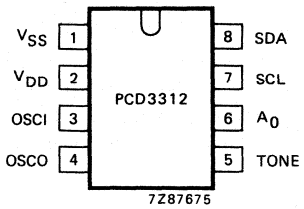


Fig. 3 Pinning diagram for the PCD3312.

PINNING

1	V_{SS}	negative supply
2	V_{DD}	positive supply
3	OSCI	oscillator input
4	OSCO	oscillator output
5	TONE	frequency output for single or dual tones
6	A_0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
7	SCL	serial clock line (I^2C bus)
8	SDA	serial data line (I^2C bus)

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311 and PCD3312 is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode (only for the PCD3311), or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus (for both PCD3311 and PCD3312).

Parallel mode can only be obtained for the PCD3311 by setting MODE input HIGH.

Data inputs (D_0, D_1, D_2, D_3, D_4 and D_5)

Inputs D_0 and D_1 have no internal pull-down or pull-up resistors and must not be left open in any application. Inputs D_2 to D_5 have internal pull-down. D_5 and D_4 are used to select between DTMF dual, DTMF single, MODEM and melody tones (see Table 1). D_3 to D_0 select the combination of the tones for DTMF or single-tone itself.

Table 1 D_5 and D_4 in accordance with the selected application

D_5	D_4	application
0	0	DTMF single tones; standby; melody tones
0	1	DTMF dual tones (all 16 combinations)
1	0	MODEM tones; standby; melody tones
1	1	melody tones

1 = H = HIGH voltage level
0 = L = LOW voltage level

Note: Tables 2, 3, 4 and 5 show all input codes and their corresponding output frequencies.

DEVELOPMENT DATA

FUNCTIONAL DESCRIPTION (continued)

Strobe input (STROBE, only for the PCD3311)

This input (with internal pull-down) allows the loading of parallel data into D_0 to D_5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained for the PCD3311 by setting MODE input LOW.

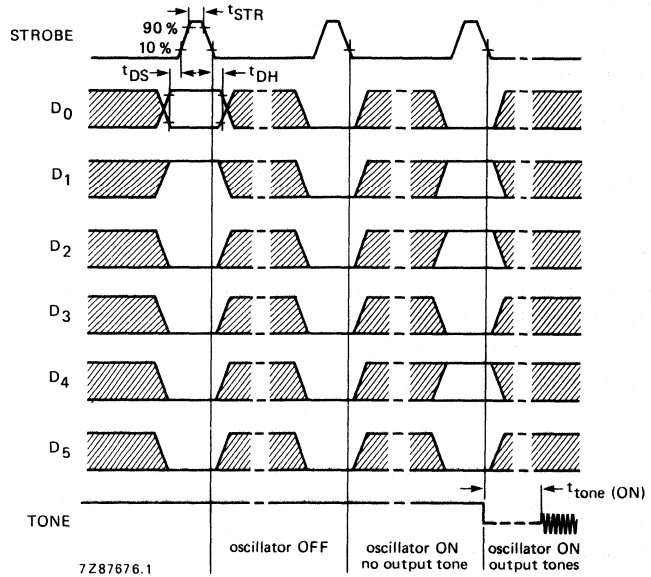


Fig. 4 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D_0 and D_1 respectively. For the PCD3311 the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A_0)

A_0 is the slave address input and it identifies the device when up to two PCD3311 or PCD3312 devices are connected to the same I^2C bus. In any case A_0 must be connected to V_{DD} or V_{SS}.

I²C bus data configuration (see Fig. 5)

The PCD3311 and PCD3312 are always slave receivers in the I²C bus configuration (R/$\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode for the PCD3311 as well as for the PCD3312, where the least significant bit is selectable by hardware on input A_0 and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 2, 3, 4, and 5). D_6 and D_7 are don't care (X) bits.

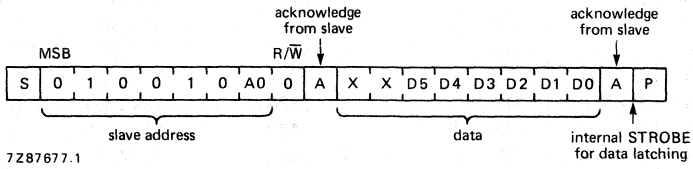


Fig. 5 I²C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 3 shows the frequency tolerance of the output tones for DTMF signalling; Tables 4 and 5 for the modem and melody tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

DEVELOPMENT DATA

Table 2 Input data for control (no output tone; TONE at V_{DD})

D_5	D_4	D_3	D_2	D_1	D_0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for DTMF

D_5	D_4	D_3	D_2	D_1	D_0	HEX	symbol	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

Table 4 Input data for MODEM frequencies

D_5	D_4	D_3	D_2	D_1	D_0	HEX	standard frequency Hz	tone output freq. Hz**	frequency deviation %	frequency deviation Hz	remarks
1	0	0	1	0	0	24	1300	1296,94	−0,24	−3,06	V.23
1	0	0	1	0	1	25	2100	2103,14	+ 0,15	+ 3,14	
1	0	0	1	1	0	26	1200	1197,17	−0,24	−2,83	Bell 202
1	0	0	1	1	1	27	2200	2192,01	−0,36	−7,99	
1	0	1	0	0	0	28	980	978,82	−0,12	−1,18	V.21
1	0	1	0	0	1	29	1180	1179,03	−0,08	−0,97	
1	0	1	0	1	0	2A	1070	1073,33	+ 0,31	+ 3,33	Bell 103
1	0	1	0	1	1	2B	1270	1265,30	−0,37	−4,70	
1	0	1	1	0	0	2C	1650	1655,66	+ 0,34	+ 5,66	V.21
1	0	1	1	0	1	2D	1850	1852,77	+ 0,15	+ 2,77	
1	0	1	1	1	0	2E	2025	2021,20	−0,19	−3,80	Bell 103
1	0	1	1	1	1	2F	2225	2223,32	−0,08	−1,68	

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

Table 5 Input data for melody tones

D_5	D_4	D_3	D_2	D_1	D_0	HEX	note	standard frequency Hz*	tone output frequency Hz**
1	1	0	0	0	0	30	D#5	622,3	622,5
1	1	0	0	0	1	31	E5	659,3	659,5
1	1	0	0	1	0	32	F5	698,5	697,9
1	1	0	0	1	1	33	F#5	740,0	741,1
1	1	0	1	0	0	34	G5	784,0	782,1
1	1	0	1	0	1	35	G#5	830,6	832,3
1	1	0	1	1	0	36	A5	880,0	879,3
1	1	0	1	1	1	37	A#5	932,3	931,9
1	1	1	0	0	0	38	B5	987,8	985,0
1	1	1	0	0	1	39	C6	1046,5	1044,5
1	1	1	0	1	0	3A	C#6	1108,7	1111,7
1	0	1	0	0	1	29	D6	1174,7	1179,0
1	1	1	0	1	1	3B	D#6	1244,5	1245,1
1	1	1	1	0	0	3C	E6	1318,5	1318,9
1	1	1	1	0	1	3D	F6	1396,9	1402,1
0	0	1	1	1	0	0E	F#6	1480,0	1482,2
1	1	1	1	1	0	3E	G6	1568,0	1572,0
1	0	1	1	0	0	2C	G#6	1661,2	1655,7
1	1	1	1	1	1	3F	A6	1760,0	1768,5
0	0	0	1	0	0	04	A#6	1864,7	1875,1
0	0	0	1	0	1	05	B6	1975,5	1970,0
1	0	0	1	0	1	25	C7	2093,0	2103,1
1	0	1	1	1	1	2F	C#7	2217,5	2223,3
0	0	0	1	1	0	06	D7	2349,3	2358,1
0	0	0	1	1	1	07	D#7	2489,0	2470,4

* Standard scale based on A4 = 440 Hz.

** Tone output frequency when using a 3,579 545 MHz crystal.

1 = H = HIGH voltage level
0 = L = LOW voltage level

DEVELOPMENT DATA

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

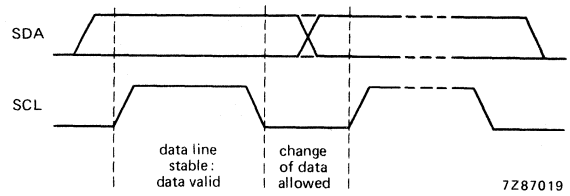


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

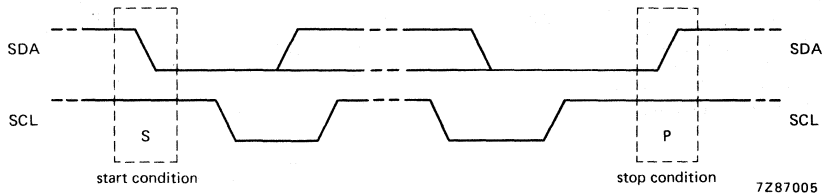


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

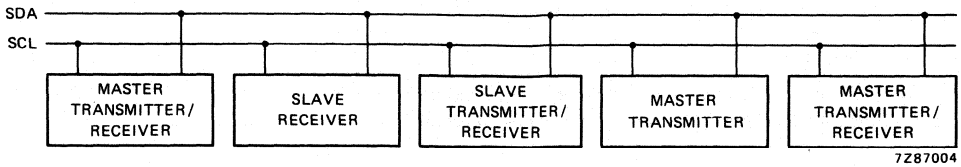


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

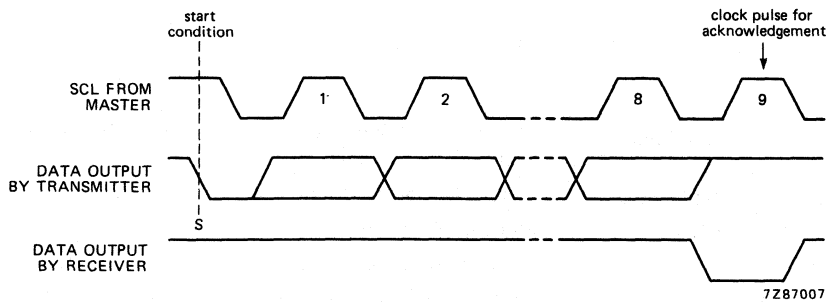


Fig. 9 Acknowledgement on the I^2C bus.

CHARACTERISTICS OF THE I²C BUS (continued)

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

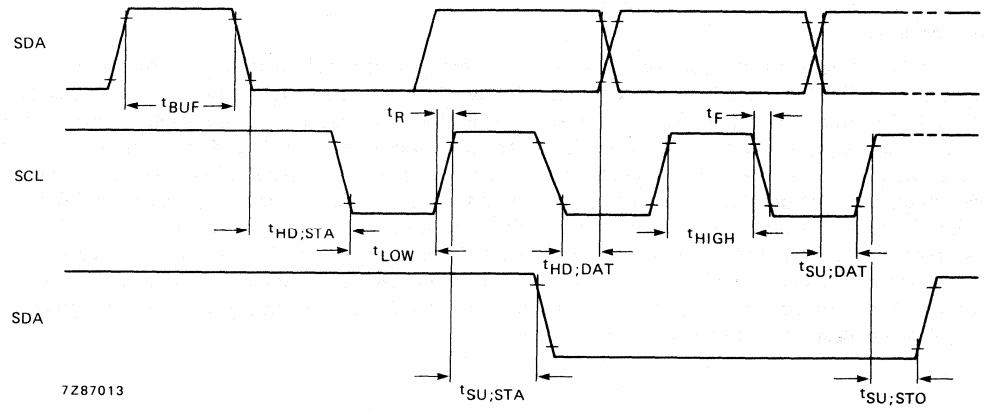


Fig. 10 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

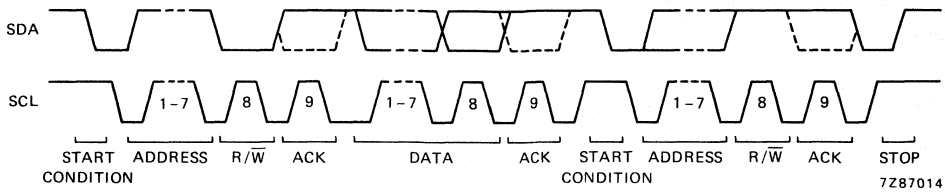


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

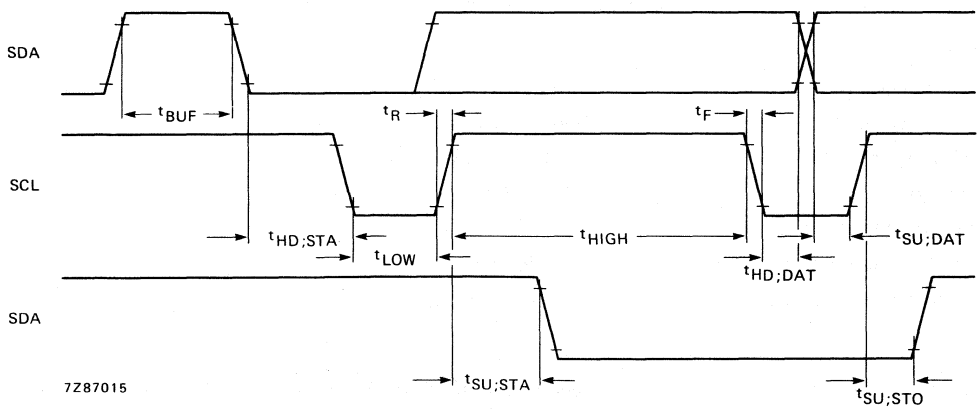


Fig. 12 Timing of the low-speed mode.

DEVELOPMENT DATA

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

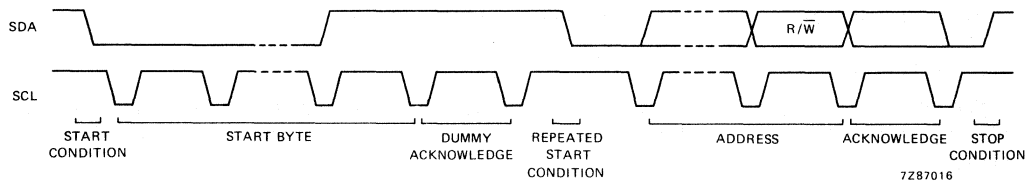


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
D.C. input current (any input)	$\pm I_I$	–	10	mA
D.C. output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 50 Ω;
T_{amb} = −25 to + 70 °C; unless otherwise specified

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	1,0	mA
dual output tone	I_{DD}	–	0,6	1,2	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D_0 to D_5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D_2 to D_5; MODE; STROBE; A_0					
Pull-down input current $V_I = V_{DD}$	$-I_{IL}$	30	150	300	nA
SCL (D_0); SDA (D_1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 10)	f_{SCL}	–	–	100	kHz
Input capacitance; $V_I = V_{SS}$	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 14)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
D.C. voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D_0/SCL and D_1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

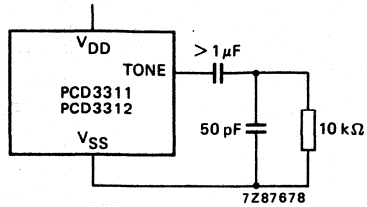


Fig. 14 TONE output test circuit.

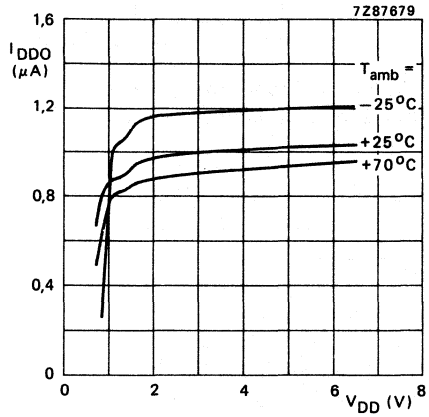


Fig. 15 Standby supply current as a function of supply voltage; oscillator OFF.

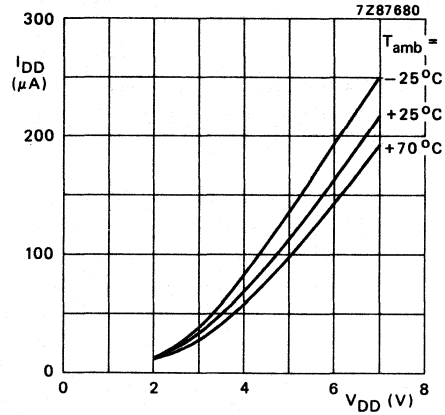


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

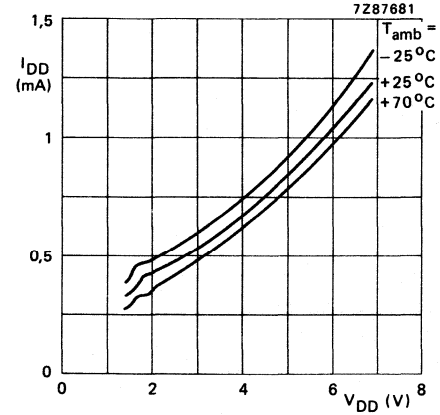


Fig. 17 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

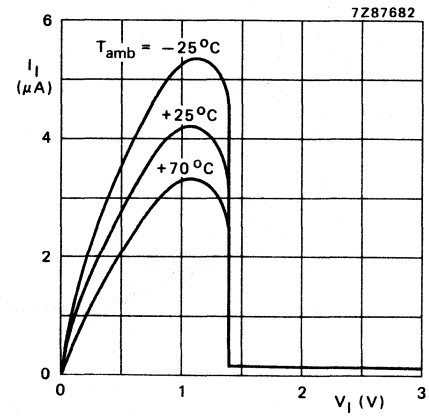


Fig. 18 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

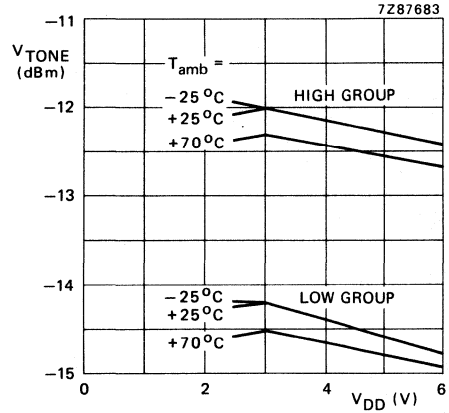


Fig. 19 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

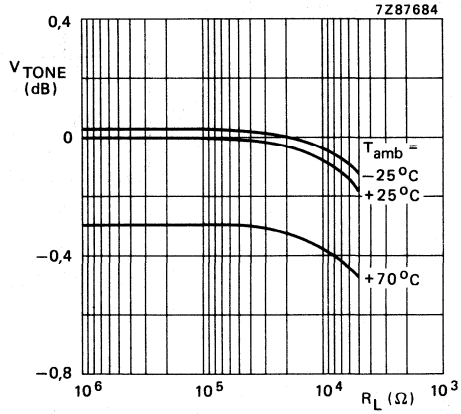


Fig. 20 Dual tone output voltage level as a function of output load resistance.

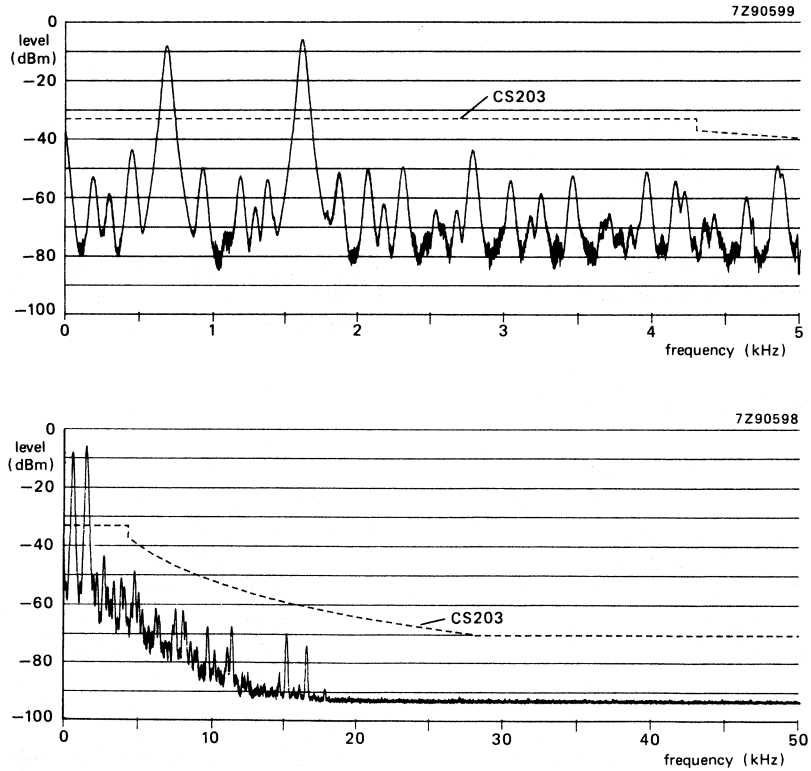


Fig. 21 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

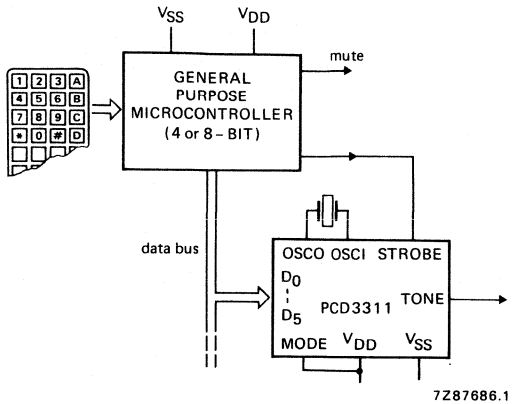


Fig. 22 PCD3311 driven by a microcontroller with parallel data-bus.

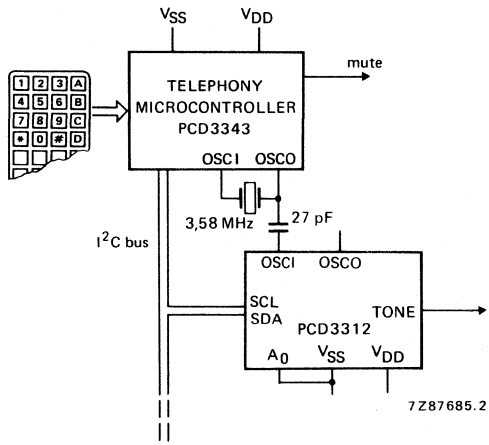


Fig. 23 PCD3312 driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus).
The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes. The same application is possible with the PCD3311 with MODE = V_{SS}.

DTMF / SINGLE -TONE GENERATOR

GENERAL DESCRIPTION

The PCD3311A is a single-chip silicon gate CMOS integrated circuit. It is intended to provide dual-tone multi-frequency (DTMF) combinations required for tone dialling systems in telephone sets which contain a microcontroller for the control functions.

The various audio output frequencies are generated from an on-chip 3,58 MHz quartz crystal-controlled oscillator.

The device can interface directly to all standard microcontrollers by accepting a binary-coded parallel input or serial data input (I^2C bus).

With its on-chip voltage reference the PCD3311A provides constant output amplitudes which are independent of the operating supply voltage and ambient temperature.

An on-chip filtering system assures a very low total harmonic distortion in accordance with the CEPT CS 203 recommendations.

In addition to the standard DTMF frequencies the device provides 32 single frequencies.

Features

- Stabilized output voltage level
- Low output distortion with on-chip filtering (CEPT CS 203 compatible)
- Latched inputs for data bus applications
- I^2C bus compatible
- Mode select input (selection of parallel or serial data input)

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current	I_{DD}	–	–	0,9	mA
Static standby current	I_{DDO}	–	–	3	μA
DTMF output voltage level (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion	THD	–	–25	–	dB
Operating ambient temperature range	T_{amb}	–25	–	+70	°C

PACKAGE OUTLINE

PCD3311AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

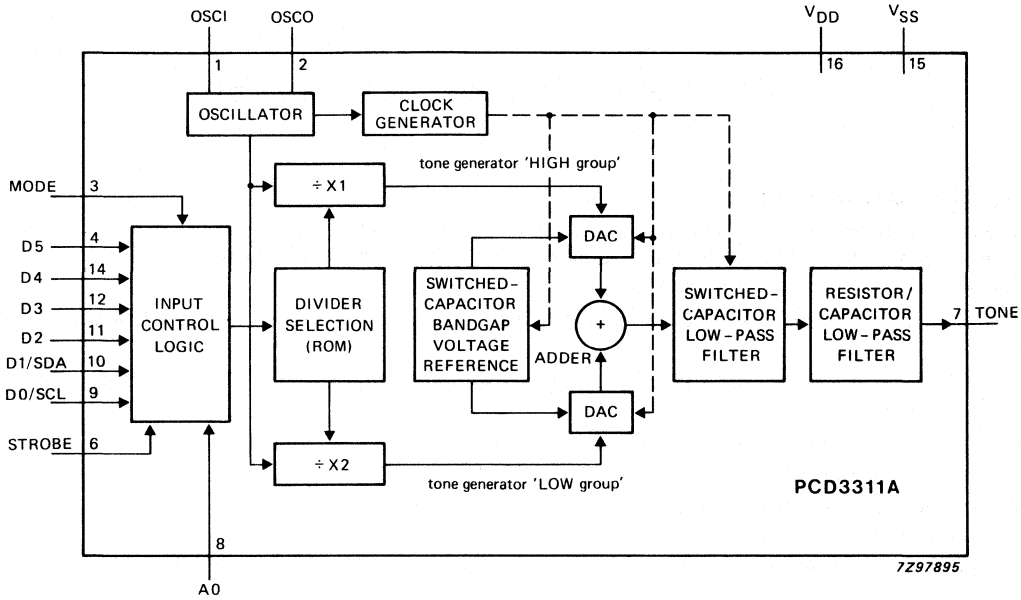


Fig. 1 Block diagram.

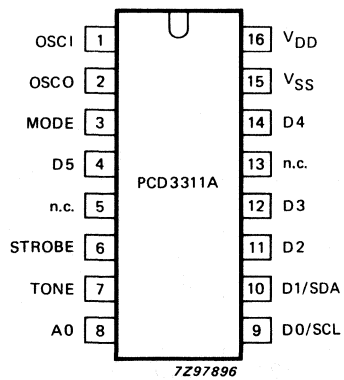


Fig. 2 Pinning diagram.

PINNING

1	OSCI	oscillator input
2	OSCO	oscillator output
3	MODE	mode select input; used for the selection between serial mode (MODE = LOW) and parallel mode (MODE = HIGH)
4	D5	parallel data input*
6	STROBE	strobe input; used for the loading of data in the parallel mode
7	TONE	frequency output for single or dual tones
8	A0	slave address input in the serial mode; must be connected to V_{DD} or V_{SS}
9	D0/SCL	parallel data input* or serial clock line (I^2C bus)
10	D1/SDA	parallel data input* or serial data line (I^2C bus)
11	D2	parallel data inputs*
12	D3	
14	D4	
15	V_{SS}	negative supply
16	V_{DD}	positive supply
5;13	n.c.	not connected

* MODE = HIGH.

FUNCTIONAL DESCRIPTION

Clock/oscillator (OSCI and OSCO)

The timebase for the PCD3311A is a crystal-controlled oscillator with a 3,58 MHz quartz crystal connected between OSCI and OSCO. Alternatively, the OSCI input can be driven from an external clock.

Mode select (MODE)

This input selects the data input mode. When connected to V_{DD}, data can be received in the parallel mode or, when connected to V_{SS} or left open, data can be received via the serial I^2C bus.

Parallel mode can only be obtained by setting MODE input HIGH.

Data inputs (D0, D1, D2, D3, D4 and D5)

Inputs D0 and D1 have no internal pulll-down or pull-up resistors and must not be left open in any application. Inputs D2 to D5 have internal pull-down.

Tables 1, 2 and 3 show all input codes and their corresponding output frequencies.

Strobe input (STROBE)

This input (with internal pull-down) allows the loading of parallel data into D0 to D5 when MODE is HIGH.

The data inputs must be stable preceeding the positive-going edge of the strobe pulse (active HIGH). Input data are loaded at the negative-going edge of the strobe pulse and then the corresponding tone (or standby mode) is provided at the TONE output. The output remains unchanged until the negative-going edge of the next STROBE pulse (for new data) is received.

Serial mode can only be obtained by setting MODE input LOW.

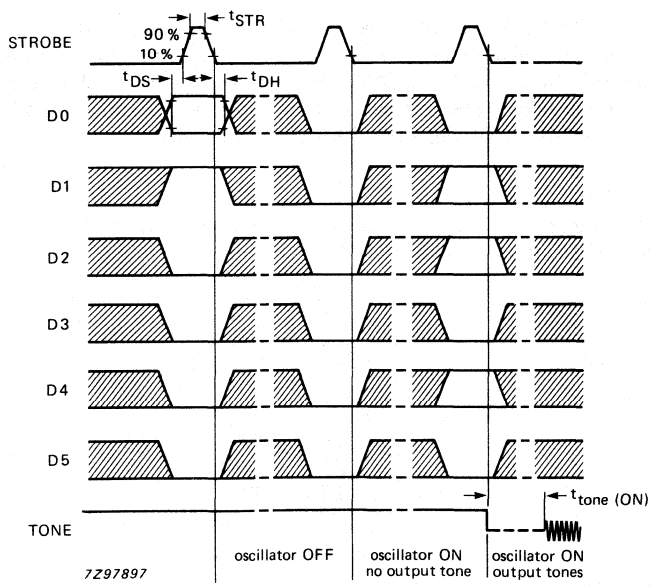


Fig. 3 Timing diagram showing control possibilities of the oscillator and the TONE output (e.g. 770 Hz + 1477 Hz) in the parallel mode (MODE = HIGH).

FUNCTIONAL DESCRIPTION (continued)

Serial clock and data inputs (SCL and SDA)

SCL and SDA are combined with D0 and D1 respectively. For the PCD3311A the selection of SCL and SDA is controlled by the MODE input. SCL and SDA are serial clock and data lines according to the I^2C bus specification (see "CHARACTERISTICS OF THE I^2C BUS"). Both inputs must be pulled-up externally to V_{DD}.

Address input (A0)

A0 is the slave address input and it identifies the device when up to two PCD3311 devices are connected to the same I^2C bus. However, A0 must be connected to V_{DD} or V_{SS}.

I^2C bus data configuration (see Fig. 4)

The PCD3311 is always a slave receiver in the I^2C bus configuration ($R/\overline{W}$ bit = 0).

The slave address consists of 7 bits in the serial mode where the least significant bit is selectable by hardware on input A0, and the other more significant bits are internally fixed. In the serial mode the same input codes are used as in the parallel mode (see Tables 1, 2 and 3). D6 and D7 are don't care (X) bits.

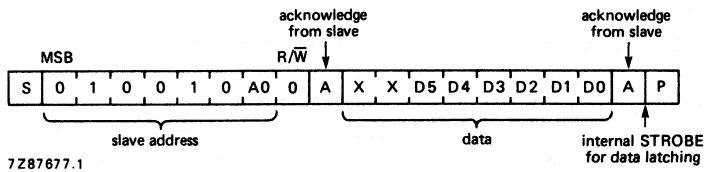


Fig. 4 I^2C bus data format.

Tone output (TONE)

The single and the dual tones which are provided at the TONE output are filtered by an on-chip switched-capacitor filter, followed by an active RC low-pass filter. Therefore, the total harmonic distortion of the DTMF tones fulfils the CEPT CS 203 recommendations. An on-chip reference voltage provides output-tone levels independent of the supply voltage. Table 2 shows the frequency tolerance of the output tones for DTMF signalling; Table 3 for the single tones.

Power-on reset

In order to avoid undefined states of the devices when the power is switched ON, an internal reset circuit sets them to the standby mode (oscillator OFF).

Table 1 Input data for control (no output tone; TONE at V_{DD})

D5	D4	D3	D2	D1	D0	HEX	oscillator
X	0	0	0	0	0	00/20	ON
X	0	0	0	0	1	01/21	OFF
X	0	0	0	1	0	02/22	OFF
X	0	0	0	1	1	03/23	OFF

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level
X = don't care.

Table 2 Input data for DTMF

D5	D4	D3	D2	D1	D0	HEX	symbol	standard frequency Hz	tone output freq. Hz*	frequency deviation %	frequency deviation Hz
0	0	1	0	0	0	08		697	697,90	+ 0,13	+ 0,90
0	0	1	0	0	1	09		770	770,46	+ 0,06	+ 0,46
0	0	1	0	1	0	0A		852	850,45	−0,18	−1,55
0	0	1	0	1	1	0B		941	943,23	+ 0,24	+ 2,23
0	0	1	1	0	0	0C		1209	1206,45	−0,21	−2,55
0	0	1	1	0	1	0D		1336	1341,66	+ 0,42	+ 5,66
0	0	1	1	1	0	0E		1477	1482,21	+ 0,35	+ 5,21
0	0	1	1	1	1	0F		1633	1638,24	+ 0,32	+ 5,24
0	1	0	0	0	0	10	0	941+1336			
0	1	0	0	0	1	11	1	697+1209			
0	1	0	0	1	0	12	2	697+1336			
0	1	0	0	1	1	13	3	697+1477			
0	1	0	1	0	0	14	4	770+1209			
0	1	0	1	0	1	15	5	770+1336			
0	1	0	1	1	0	16	6	770+1477			
0	1	0	1	1	1	17	7	852+1209			
0	1	1	0	0	0	18	8	852+1336			
0	1	1	0	0	1	19	9	852+1477			
0	1	1	0	1	0	1A	A	697+1633			
0	1	1	0	1	1	1B	B	770+1633			
0	1	1	1	0	0	1C	C	852+1633			
0	1	1	1	0	1	1D	D	941+1633			
0	1	1	1	1	0	1E	*	941+1209			
0	1	1	1	1	1	1F	#	941+1477			

DEVELOPMENT DATA

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

* Tone output frequency when using a 3,579 545 MHz crystal.

FUNCTIONAL DESCRIPTION (continued)

Table 3 Input data for single frequencies

D5	D4	D3	D2	D1	D0	HEX	standard frequency (Hz)	tone output (Hz)*	frequency deviation	
									%	Hz
0	0	0	1	0	0	04	680	679,62	−0,06	−0,38
0	0	0	1	0	1	05	740	741,11	+0,15	+1,11
0	0	0	1	1	0	06	810	810,59	+0,07	+0,59
0	0	0	1	1	1	07	873	874,34	+0,15	+1,34
1	0	0	1	0	0	24	886	884,28	−0,20	−1,73
1	0	0	1	0	1	25	930	931,93	+0,21	+1,93
1	0	0	1	1	0	26	970	972,70	+0,28	+2,70
1	0	0	1	1	1	27	991	991,29	+0,03	+0,29
1	0	1	0	0	0	28	1055	1051,57	−0,33	−3,43
1	0	1	0	0	0	28	1060	1051,57	−0,80	−8,43
1	0	1	0	0	1	29	1124	1127,77	+0,34	+3,77
1	0	1	0	1	0	2A	1160	1161,44	+0,12	+1,44
1	0	1	0	1	1	2B	1197	1197,17	+0,01	+0,17
1	0	1	1	0	0	2C	1270	1275,68	+0,45	+5,68
1	0	1	1	0	0	2C	1275	1275,68	+0,05	+0,68
1	0	1	1	0	1	2D	1358	1353,33	−0,34	−4,68
1	0	1	1	1	0	2E	1400	1402,09	+0,15	+2,09
1	0	1	1	1	1	2F	1446	1441,04	−0,34	−4,96
1	1	0	0	0	0	30	1520	1525,81	+0,38	+5,81
1	1	0	0	0	0	30	1530	1525,81	−0,27	−4,19
1	1	0	0	0	1	31	1540	1540,92	+0,06	+0,92
1	1	0	0	1	0	32	1640	1638,24	−0,11	−1,76
1	1	0	0	1	1	33	1670	1673,47	+0,21	+3,47
1	1	0	1	0	0	34	1747	1748,68	+0,10	+1,68
1	1	0	1	0	1	35	1830	1830,97	+0,05	+0,97
1	1	0	1	1	0	36	1860	1852,77	−0,39	−7,23
1	1	0	1	1	1	37	1960	1970,03	+0,51	+10,03
1	1	0	1	1	1	37	1981	1970,03	−0,55	−10,97
1	1	1	0	0	0	38	2000	2021,20	+1,06	+21,20
1	1	1	0	0	1	39	2110	2103,14	−0,33	−6,86
1	1	1	0	1	0	3A	2200	2192,01	−0,36	−7,99
1	1	1	0	1	1	3B	2247	2255,54	+0,38	+8,54
1	1	1	1	0	0	3C	2280	2288,71	+0,38	+8,71
1	1	1	1	0	1	3D	2400	2394,34	−0,24	−5,66
1	1	1	1	1	0	3E	2600	2593,87	−0,24	−6,13
1	1	1	1	1	1	3F	2800	2779,15	−0,75	−20,85

Where:

1 = H = HIGH voltage level
0 = L = LOW voltage level

* Tone output frequency when using a 3,579545 MHz crystal.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

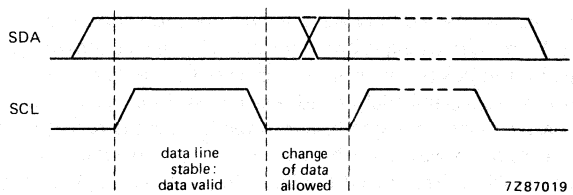


Fig. 5 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

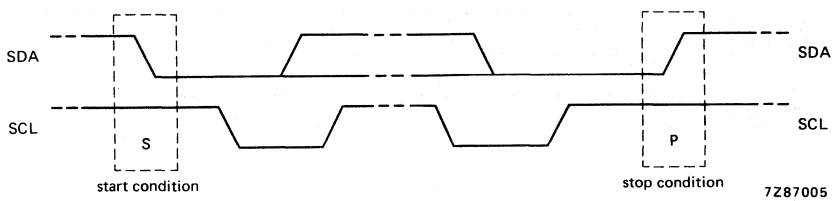


Fig. 6 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

CHARACTERISTICS OF THE I²C BUS (continued)

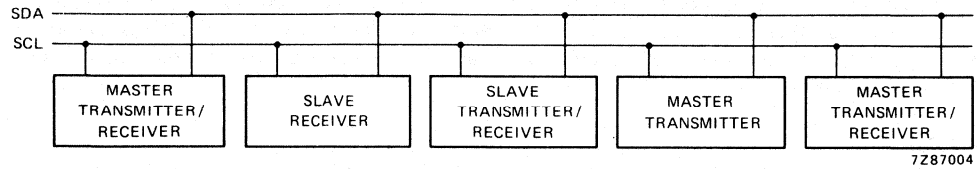


Fig. 7 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

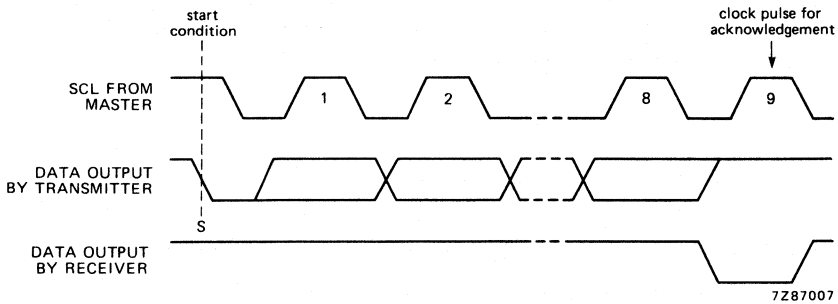


Fig. 8 Acknowledgement on the I²C bus.

DEVELOPMENT DATA

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The ICs operate in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 9.

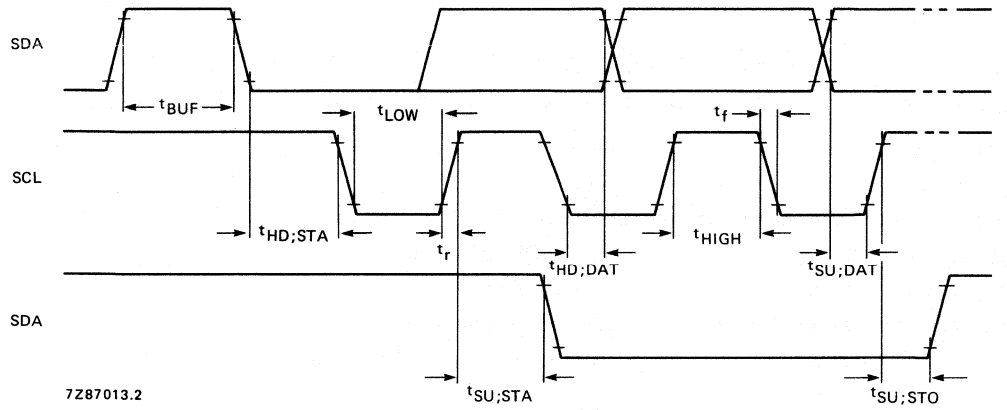


Fig. 9 Timing of the high-speed mode.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

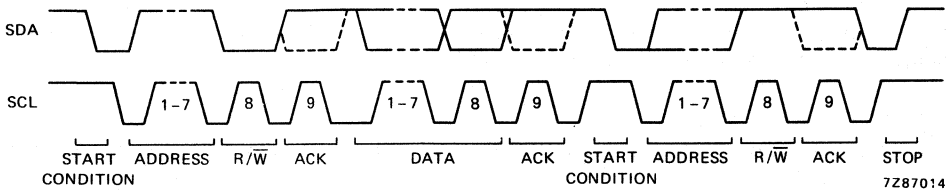


Fig. 10 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs

The dashed line is the acknowledgement of the receiver

Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 11.

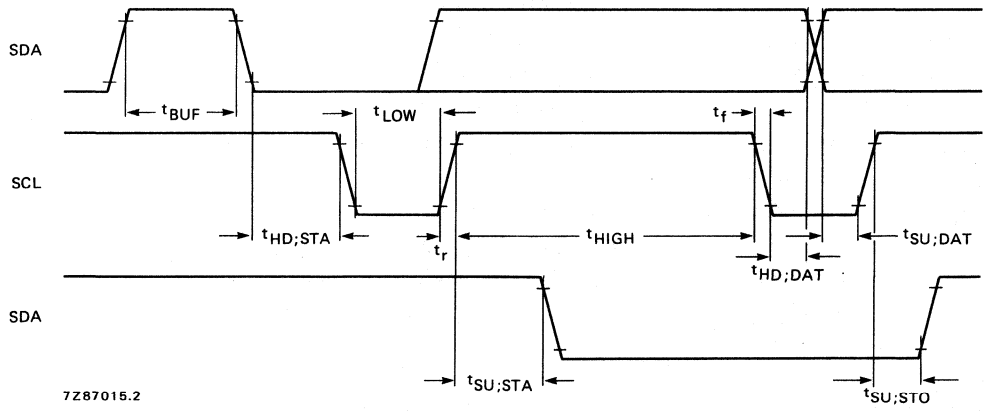


Fig. 11 Timing of the low-speed mode.

Timing specifications (continued)

Where:

t_{BUF}	$t \geqslant 105\ \mu s$ (t_{LOWmin})
$t_{HD;STA}$	$t \geqslant 365\ \mu s$ ($t_{HIGHmin}$)
t_{LOW}	$130\ \mu s \pm 25\ \mu s$
t_{HIGH}	$390\ \mu s \pm 25\ \mu s$
$t_{SU;STA}$	$130\ \mu s \pm 25\ \mu s$ *
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_r	$t \leqslant 1\ \mu s$
t_f	$t \leqslant 300$ ns
$t_{SU;STO}$	$130\ \mu s \pm 25\ \mu s$

Note

All the timing values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}. For definitions see high-speed mode.

DEVELOPMENT DATA

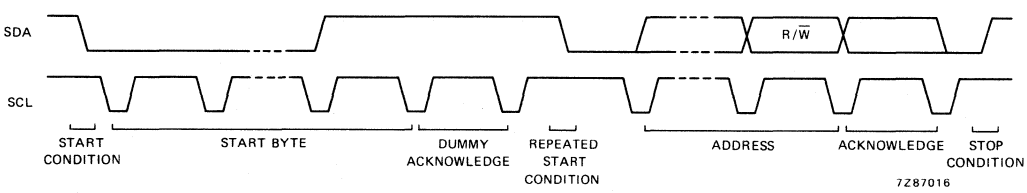


Fig. 12 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	$130\ \mu s \pm 25\ \mu s$
$t_{HIGHmin}$	$390\ \mu s \pm 25\ \mu s$
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Max. number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook "ICs for digital systems in radio, audio and video equipment".

* Only valid for repeated start code.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage range	V_{DD}	−0,8	+ 8,0	V
Input voltage range (any input)	V_I	−0,8	V_{DD}+0,8	V
DC input current (any input)	$\pm I_I$	–	10	mA
DC output current (any output)	$\pm I_O$	–	10	mA
Supply current	$\pm I_{DD}$; $\pm I_{SS}$	–	50	mA
Power dissipation per output	P_O	–	50	mW
Total power dissipation per package	P_{tot}	–	300	mW
Operating ambient temperature range	T_{amb}	−25	+ 70	°C
Storage temperature range	T_{stg}	−65	+ 150	°C

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; crystal parameters: f_{osc} = 3,579 545 MHz, R_{Smax} = 100 Ω; T_{amb} = −25 to + 70 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6,0	V
Operating supply current (note 1) oscillator ON; V_{DD} = 3 V					
no output tone	I_{DD}	–	50	100	μA
single output tone	I_{DD}	–	0,5	0,9	mA
dual output tone	I_{DD}	–	0,6	0,9	mA
Static standby current oscillator OFF; note 1	I_{DDO}	–	–	3	μA
Inputs/outputs (SDA)					
D0 to D5; MODE; STROBE					
Input voltage LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
D2 to D5; MODE; STROBE; A0					
Pull-down input current V_I = V_{DD}	$-I_{IL}$	30	150	300	nA
SCL (D0); SDA (D1)					
Output current LOW (SDA) V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Clock frequency (see Fig. 10)	f_{SCL}	–	–	100	kHz
Input capacitance; V_I = V_{SS}	C_I	–	–	7	pF
Allowable input spike pulse width	t_I	–	–	100	ns

parameter	symbol	min.	typ.	max.	unit
TONE output (see Fig. 13)					
DTMF output voltage levels (r.m.s. values)					
HIGH group	$V_{HG(rms)}$	158	192	205	mV
LOW group	$V_{LG(rms)}$	125	150	160	mV
DC voltage level	V_{DC}	–	½ V_{DD}	–	V
Pre-emphasis of group	ΔV_G	1,85	2,10	2,35	dB
Total harmonic distortion T_{amb} = 25 °C					
dual tone; note 2	THD	–	–25	–	dB
modem tone, note 3	THD	–	–29	–	dB
Output impedance	$\|Z_O\|$	–	0,1	0,5	kΩ
OSCI input					
Maximum allowable amplitude at OSCI	$V_{OSC(p-p)}$	–	–	$V_{DD}-V_{SS}$	V
Timing (V_{DD} = 3 V)					
Oscillator start-up time	$t_{OSC(ON)}$	–	3	–	ms
TONE start-up time; note 4	$t_{TONE(ON)}$	–	0,5	–	ms
STROBE pulse width; note 5	t_{STR}	400	–	–	ns
Data set-up time; note 5	t_{DS}	150	–	–	ns
Data hold time; note 5	t_{DH}	100	–	–	ns

DEVELOPMENT DATA

Notes to the characteristics

1. Crystal is connected between OSCI and OSCO; D0/SCL and D1/SDA via a resistance of 5,6 kΩ to V_{DD}; all other pins left open.
2. Related to the level of the LOW group frequency component (CEPT CS 203).
3. Related to the level of the fundamental frequency.
4. Oscillator must be running.
5. Values are referenced to the 10% and 90% levels of the relevant pulse amplitudes, with a total voltage swing from V_{SS} to V_{DD}.

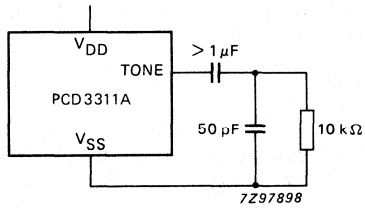


Fig. 13 TONE output test circuit.

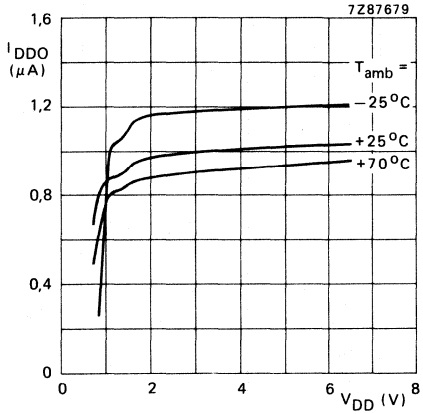


Fig. 14 Standby supply current as a function of supply voltage; oscillator OFF.

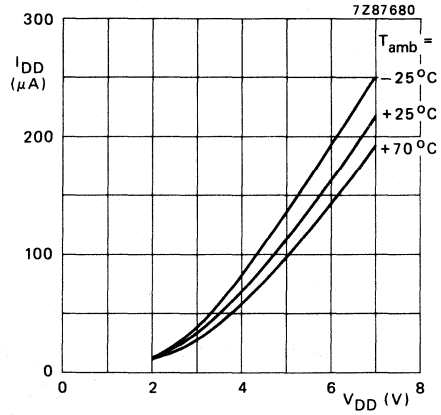


Fig. 15 Operating supply current as a function of supply voltage; oscillator ON; no output at TONE.

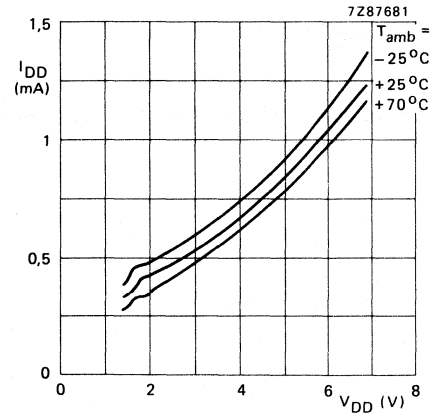


Fig. 16 Operating supply current as a function of supply voltage; oscillator ON; dual tone at TONE.

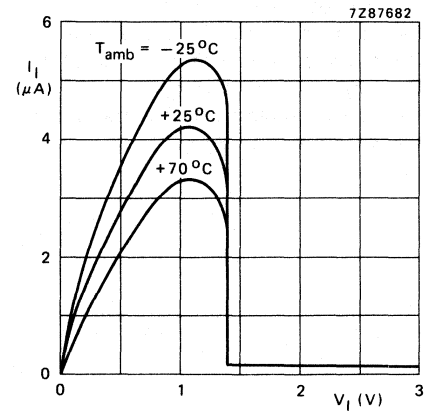


Fig. 17 Pull-down input current as a function of input voltage; V_{DD} = 3 V.

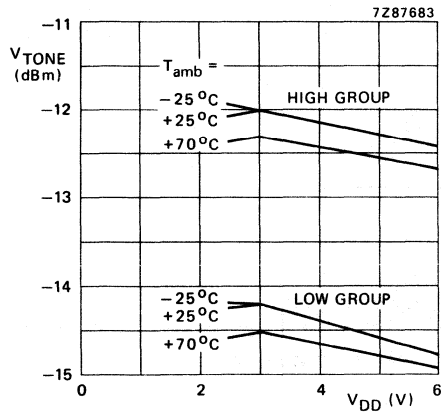


Fig. 18 DTMF output voltage levels as a function of operating supply voltage; R_L = 1 MΩ.

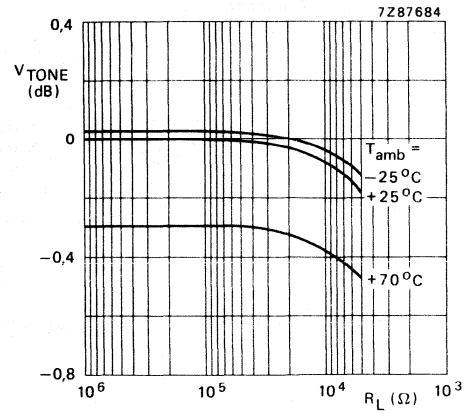


Fig. 19 Dual tone output voltage level as a function of output load resistance.

DEVELOPMENT DATA

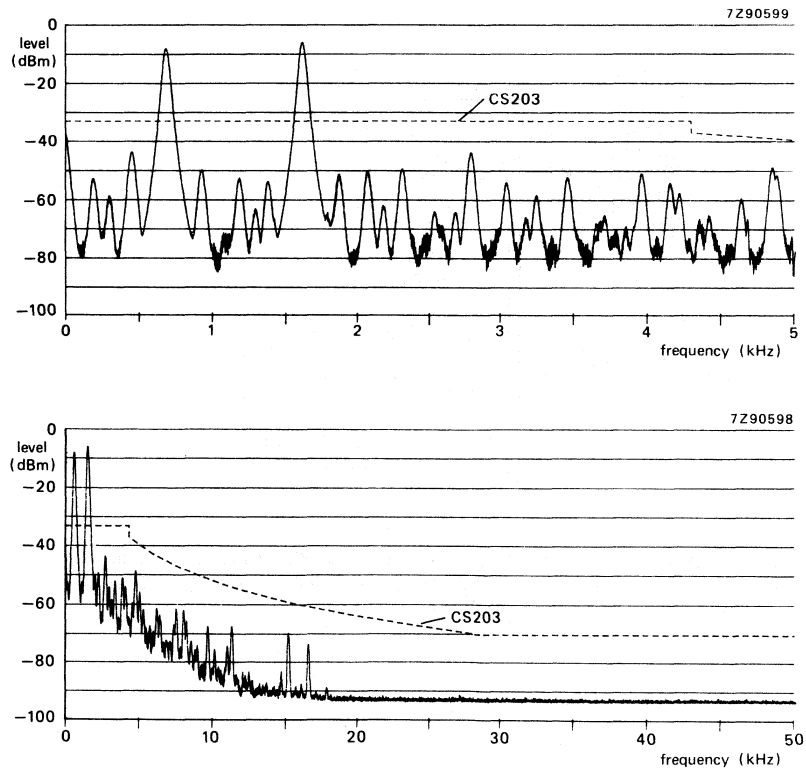


Fig. 20 Typical frequency spectrum of a dual tone signal after flat-band amplification of 6 dB.

APPLICATION INFORMATION

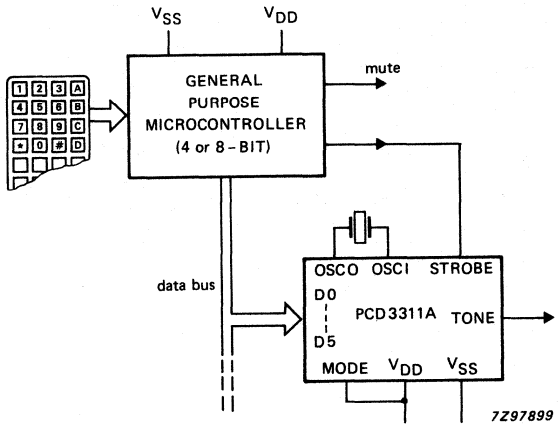


Fig. 21 PCD3311A driven by a microcontroller with parallel data-bus.

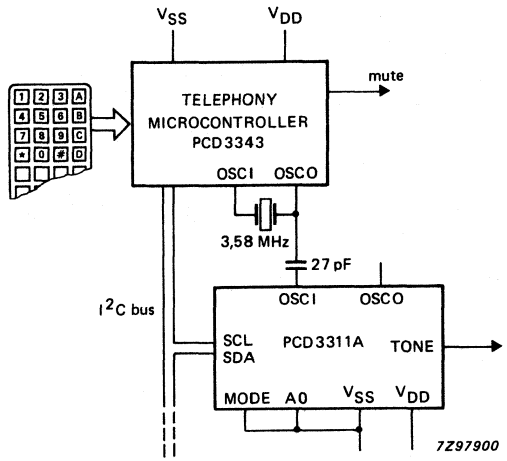


Fig. 22 PCD3311A driven by telephony microcontroller PCD3343 with serial I/O (I^2C bus). The PCD3343 is a single-chip 8-bit microcontroller with 3K ROM/224 RAM bytes.

LCD DRIVER

GENERAL DESCRIPTION

The members of the PCF21XX family are single chip, silicon gate CMOS circuits. A three-line bus (CBUS) structure enables serial data transfer with microcontrollers. All inputs are CMOS/NMOS compatible.

Features

- Supply voltage 2,25 to 6,5 V
- Low current consumption
- Serial data input
- CBUS control
- One-point built-in oscillator
- Expansion possibility
- Power-on reset clear

	PCF2100	PCF2110	PCF2111	PCF2112
• LCD segments	40	60	64	32
• LED segments	–	2	–	–
• Multiplex rate	1:2	1:2	1:2	1:1
• Word length	22 bit	34 bit	34 bit	34 bit

PACKAGE OUTLINES

PCF2100P: 28-lead DIL; plastic (SOT117).

PCF2110P:
PCF2111P: 40-lead DIL; plastic (SOT129).
PCF2112P:

PCF2100T: 28-lead mini-pack; plastic (SO28; SOT136A).

PCF2110T:
PCF2111T: 40-lead mini-pack; plastic (VSO40; SOT158A).
PCF2112T:

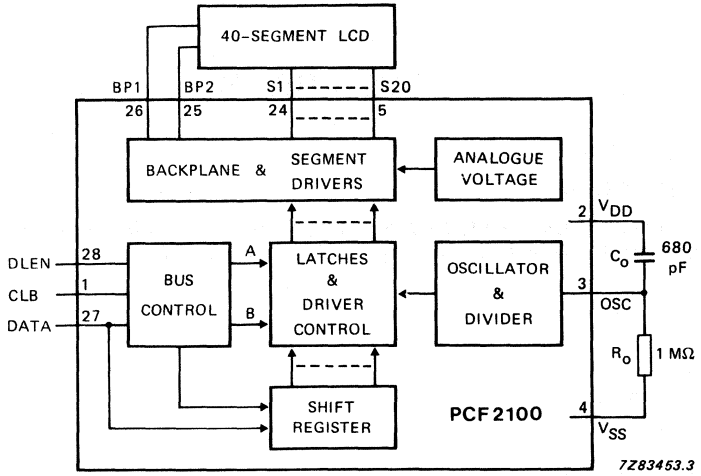


Fig. 1 Block diagram; PCF2100

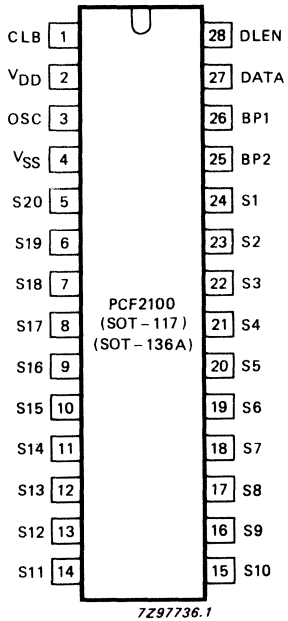


Fig. 2 Pinning diagram; PCF2100

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
27	DATA	data line	CBUS
28	DLEN	data line enable	CBUS

Outputs

5 to 24	S20 to S1	LCD driver outputs
25	BP2	backplane drivers (commons of LCD)
26	BP1	backplane drivers (commons of LCD)

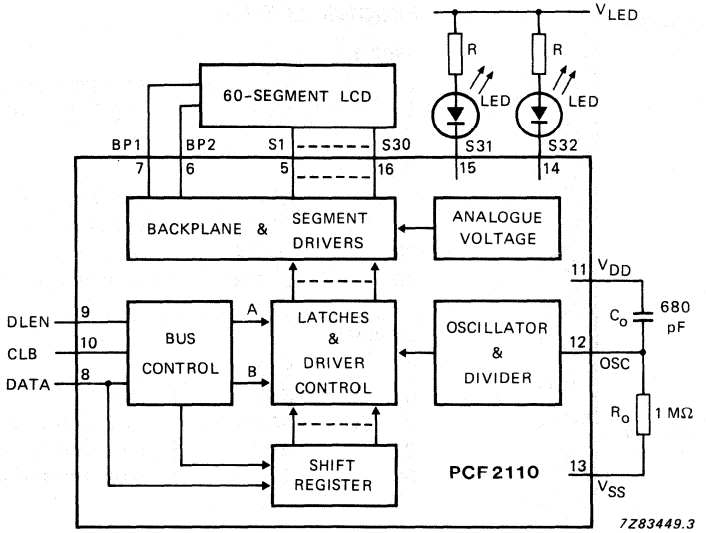


Fig. 3 Block diagram; PCF2110 (SOT-129).

DEVELOPMENT DATA

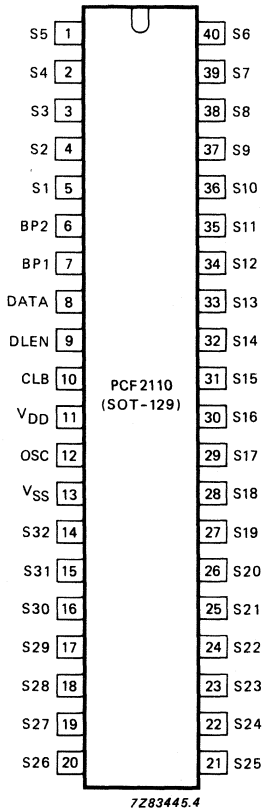


Fig. 4 Pinning diagram; PCF2110

PINNING (SOT-129)

Supply

11	V_{DD}	positive supply
13	V_{SS}	negative supply

Inputs

8	DATA	data line	CBUS
9	DLEN	data line enable	CBUS
10	CLB	clock burst	CBUS
12	OSC	oscillator input	

Outputs

1 to 5	S5 to S1	LCD driver outputs
6	BP2	backplane drivers (commons of LCD)
7	BP1	backplane drivers (commons of LCD)
14	S32	LED driver outputs
15	S31	LED driver outputs
16 to 40	S30 to S6	LCD driver outputs

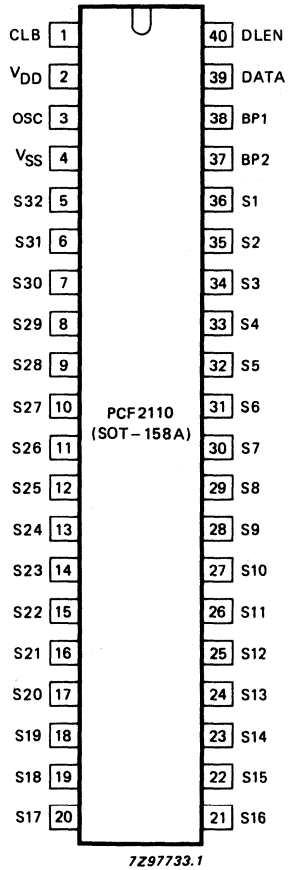


Fig. 5 Pinning diagram; PCF2110

PINNING (SOT-158A)

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)
3	OSC	oscillator input
39	DATA	data line (CBUS)
40	DLEN	data line enable (CBUS)

Outputs

5	S32	LED driver outputs
6	S31	LED driver outputs
7 to 36	S30 to S1	LCD driver outputs
37	BP2	backplane drivers (commons of LCD)
38	BP1	backplane drivers (commons of LCD)

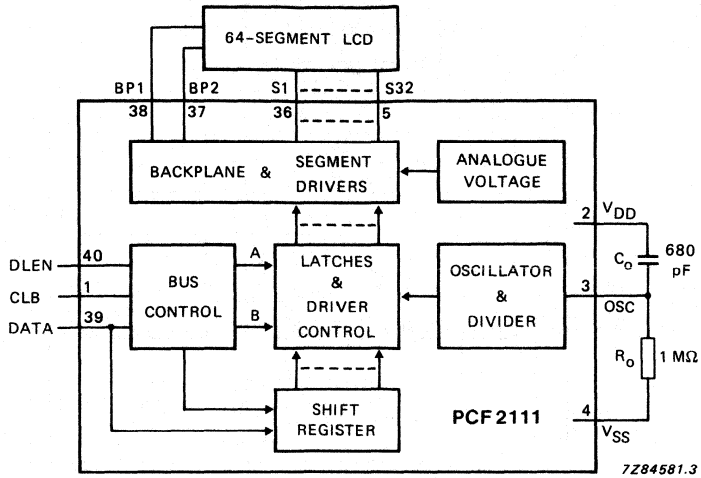


Fig. 6 Block diagram; PCF2111

DEVELOPMENT DATA

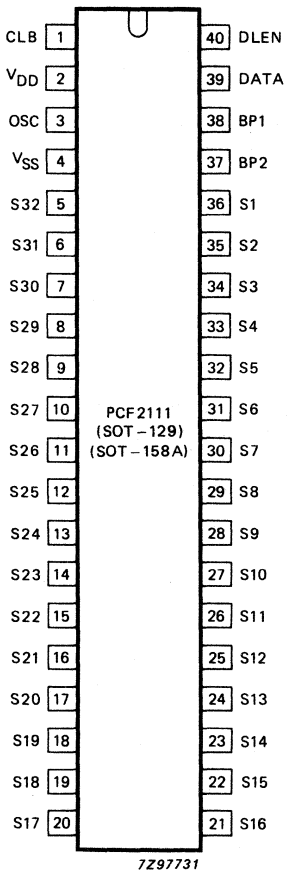


Fig. 7 Pinning diagram; PCF2111

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP1	backplane drivers (commons of LCD)
37	BP2	backplane drivers (commons of LCD)

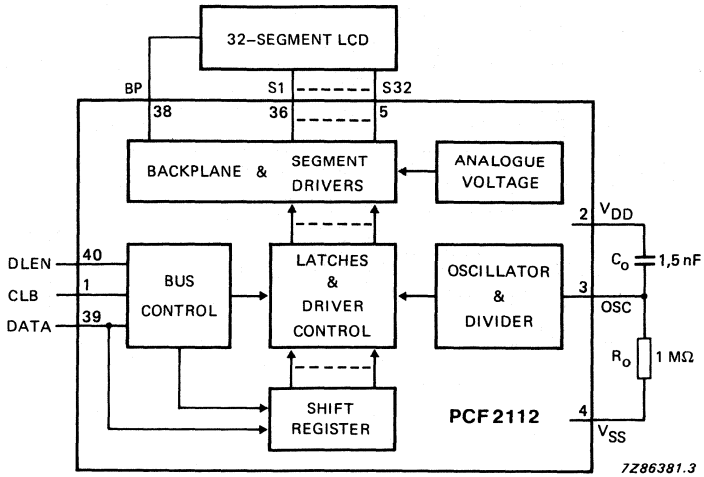


Fig. 8 Block diagram; PCF2112

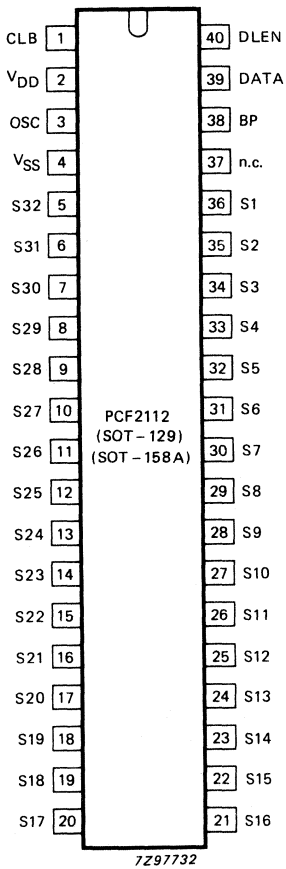


Fig. 9 Pinning diagram; PCF2112

PINNING

Supply

2	V_{DD}	positive supply
4	V_{SS}	negative supply

Inputs

1	CLB	clock burst (CBUS)	
3	OSC	oscillator input	
39	DATA	data line	CBUS
40	DLEN	data line enable	CBUS

Outputs

5 to 36	S32 to S1	LCD driver outputs
38	BP	backplane driver (common of LCD)
37	n.c.	not connected

FUNCTIONAL DESCRIPTION

An LCD segment or LED output is activated when the corresponding DATA-bit is HIGH.

PCF2100

When DATA-bit 21 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 21 LOW, the B-latches (BP2) are loaded. CLB-pulse 23 transfers data from the shift register to the selected latches.

PCF2110

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. Bits 31 and 32 contain the LED output information. With DATA-bit 33 LOW, the B-latches (BP2) are loaded and bits 31 and 32 are ignored. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2111

When DATA-bit 33 is HIGH, the A-latches (BP1) are loaded. With DATA-bit 33 LOW, the B-latches (BP2) are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

PCF2112

When DATA-bit 33 is HIGH, the latches are loaded. CLB-pulse 35 transfers data from the shift register to the selected latches.

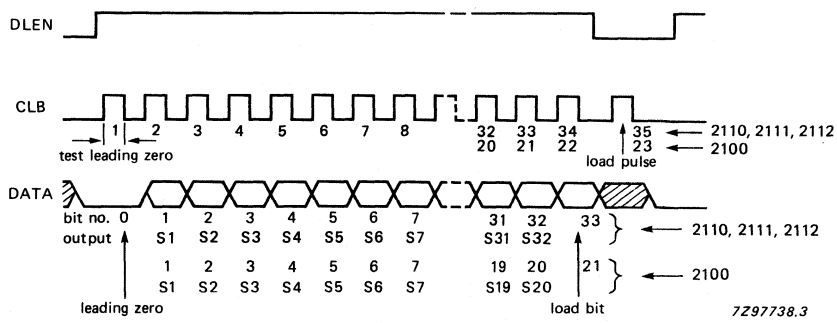


Fig. 10 CBUS data format.

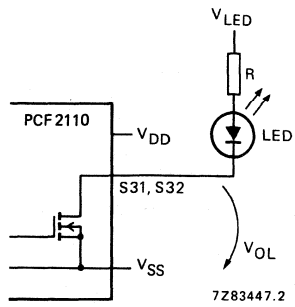


Fig. 11 LED driver circuitry.

The following tests are carried out by the bus control logic:

a. Test on leading zero.
b. Test on number of DATA-bits.
c. Test of disturbed DLEN and DATA signals during transmission.

If one of the test conditions is not fulfilled, no action follows the load condition (load pulse with DLEN LOW) and the driver is ready to receive new data.

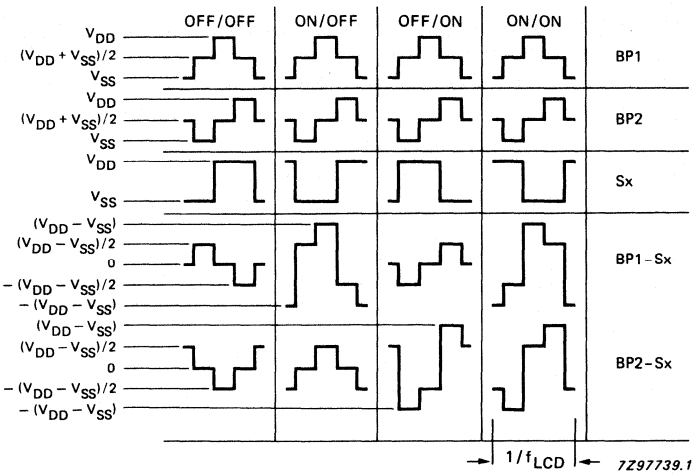


Fig. 12 Timing diagram (except PCF2112).

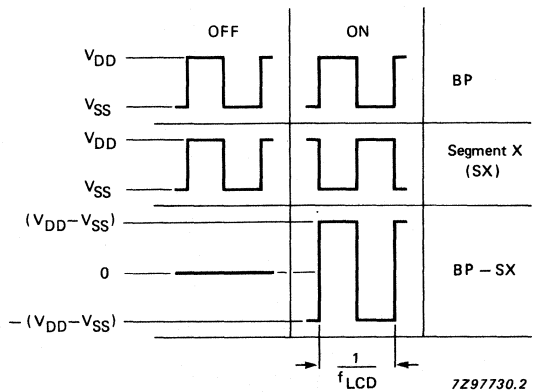


Fig. 13 Timing diagram for PCF2112.

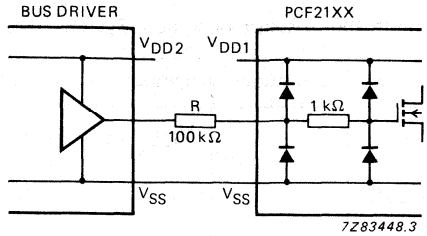
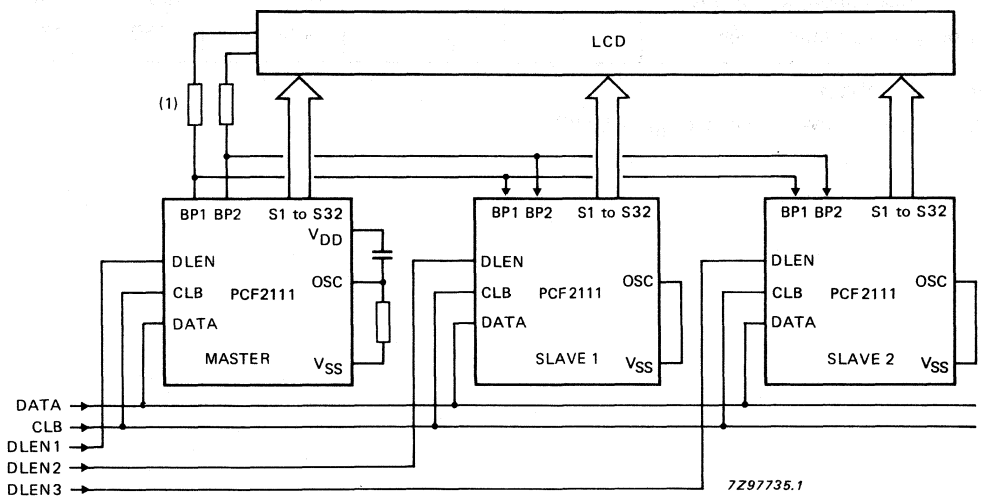


Fig. 14 Input circuitry.

Note to Fig. 14

V_{SS} line is common. In systems where it is expected that $V_{DD2} > V_{DD1} + 0{,}5$ V, a resistor should be inserted to reduce the current flowing through the input protection. Maximum input current $\leqslant 40\,\mu A$.



(1) In the slave mode, the serial resistors between BP1 and BP2 of the PCF2111 and the backplane of the LCD must be $> 2{,}7$ kΩ. In most applications the resistance of the interconnection to the LCD already has a higher value.

Fig. 15 Diagram showing expansion possibility (using PCF2111).

Note to Fig. 15

By connecting OSC to V_{SS} the BP-pins become inputs and generate signals synchronized to the single oscillator frequency, thus allowing expansion of several members of the PCF21XX family up to the BP drive capability of the master. The PCF2112 can only function as a master for other PCF2112s.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage range		V_{DD}	−0,5	9,0	V
Input voltage range DLEN, CLB, DATA and OSC		V_I	V_{SS}−0,5	V_{DD}+0,5	V
Output voltage range BP1, BP2 and S1 to S32		V_O	V_{SS}−0,5	V_{DD}+0,5	V
Supply current		$\pm I_{DD}$, $\pm I_{SS}$	−	50	mA
DC input current		$\pm I_I$	−	20	mA
DC output current		$\pm I_O$	−	25	mA
Total power dissipation per package	note 1	P_{tot}	−	500	mW
Power dissipation per output		P_O	−	100	mW
Storage temperature range		T_{stg}	−65	+150	°C

Note to the ratings

1. Derate by 7,7 mW/°C when $T_{amb} > 60$ °C.

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DEVELOPMENT DATA

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		V_{DD}	2,25	–	6,5	V
Supply current	note 1	I_{DD1}	–	20	50	μA
Supply current	note 1; T_{amb} = −25 to + 85 °C	I_{DD2}	–	20	30	μA
Power-on reset level	note 2	V_{POR}	–	1,0	1,4	V
Inputs CLB, DATA DLEN						
Input voltage						
LOW		V_{IL}	–	–	0,8	V
HIGH		V_{IH}	2,0	–	–	V
Leakage current	$V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	–	1	μA
Input capacitance	note 3	C_I	–	–	10	pF
Input OSC						
Oscillator start-up current	$V_I = V_{SS}$	I_{OSC}	0,5	1,2	5,0	μA
LCD outputs						
DC component of backplane drivers		$\pm V_{BP}$	–	20	–	mV
Backplane driver output impedance	note 4; V_{DD} = 5 V	R_{BP}	–	0,5	5	kΩ
Segment driver output impedance	note 4; V_{DD} = 5 V	R_S	–	1	7	kΩ
LED outputs (S31 and S32 in PCF2110)						
Output current LOW	V_{OL}=0,4 V; V_{DD}=5 V	I_{OL}	8	14	–	mA
Output leakage current	$V_O = V_{DD}$	$\pm I_O$	–	–	1	μA
Load current		I_{LED}	–	–	20	mA

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,25 to 6,5 V; T_{amb} = −40 to + 85 °C; R_O = 1 MΩ; C_O = 680 pF; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Inputs CLB, DATA DLEN						
Data set-up time		t_{SUDA}	3	–	–	μs
Data hold time		t_{HDDA}	3	–	–	μs
Leading zero set-up time		t_{SULZ}	3	–	–	μs
Enable set-up time		t_{SUEN}	1	–	–	μs
Disable set-up time		t_{SUDI}	2	–	–	μs
Load pulse set-up time		t_{SULD}	2,5	–	–	μs
Busy time		t_{BUSY}	3	–	–	μs
CLB HIGH time		t_{WH}	1	–	–	μs
CLB LOW time		t_{WL}	5	–	–	μs
CLB period		t_{CLB}	10	–	–	μs
Rise and fall times		t_r, t_f	–	–	10	μs
LCD timing						
LCD frame frequency		f_{LCD}	60	75	100	Hz
LCD frame frequency for PCF2112	C_O = 1,5 nF	f_{LCD}	30	35	50	Hz
Transfer time with test loads	V_{DD} = 5 V	t_{BS}	–	20	100	μs
Driver delay with test loads	V_{DD} = 5 V	t_{PLCD}	–	20	100	μs

Notes to the characteristics

1. Outputs open; CBUS inactive.
2. Resets all logic, when $V_{DD} < V_{POR}$.
3. Periodically sampled (not 100% tested).
4. Outputs measured one at a time.
5. All timing values are referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

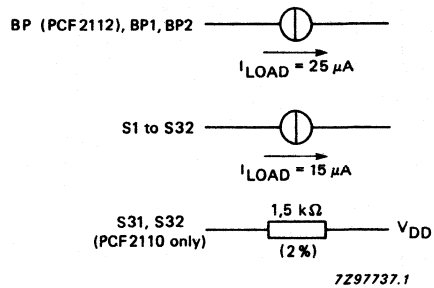
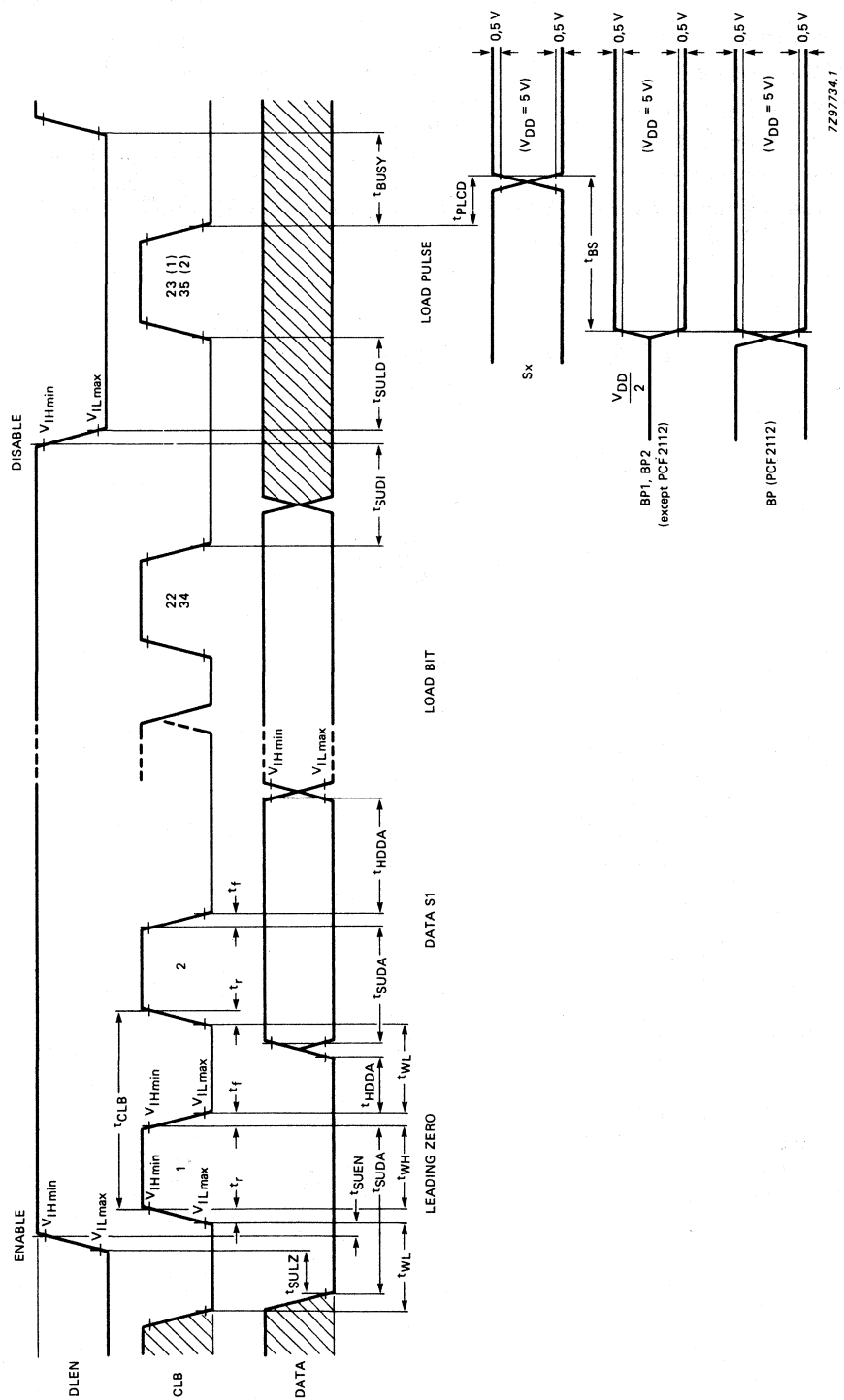


Fig. 16 Test loads.

DEVELOPMENT DATA



(1) Load pulse 23 (for PCF2100).
(2) Load pulse 35 (for PCF2110, PCD2111 and PCF2112; see Fig. 10).

Fig. 17 CBUS timing.

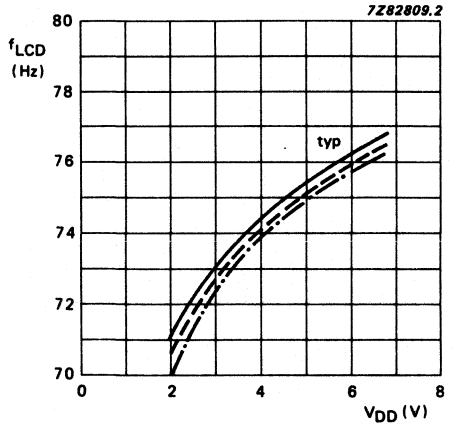


Fig. 18 Displays frequency as a function of supply voltage; C_O = 680 pF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

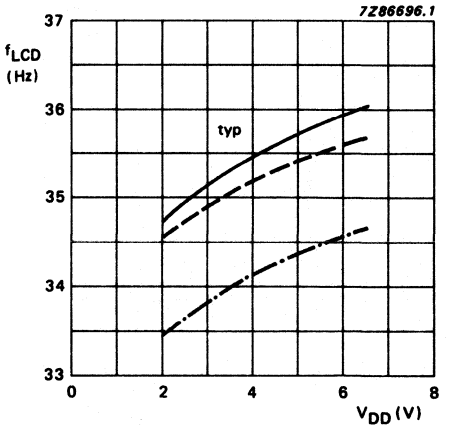


Fig. 19 Display frequency as a function of supply voltage; C_O = 1,5 nF (except PCF2112).
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

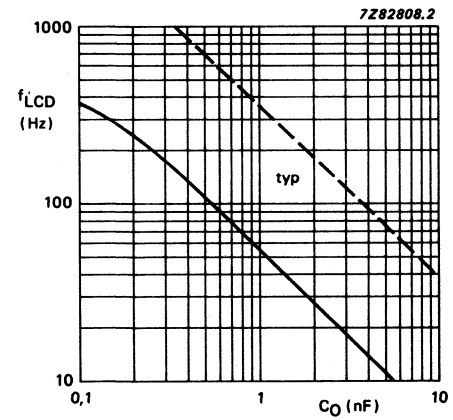


Fig. 20 Display frequency as a function of R_O and C_O; T_{amb} = + 25 °C; V_{DD} = 5 V.
——— R_O = 1 MΩ;
– – – – R_O = 100 kΩ.

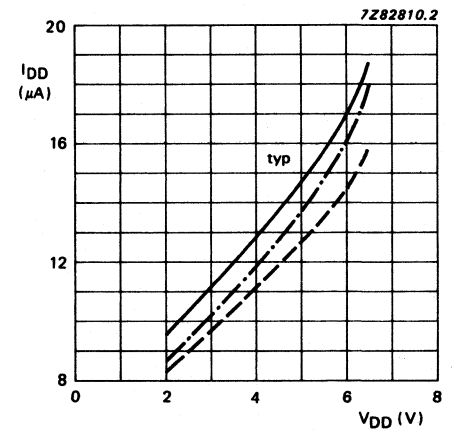


Fig. 21 Supply current as a function of supply voltage.
——— T_{amb} = –40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

DEVELOPMENT DATA

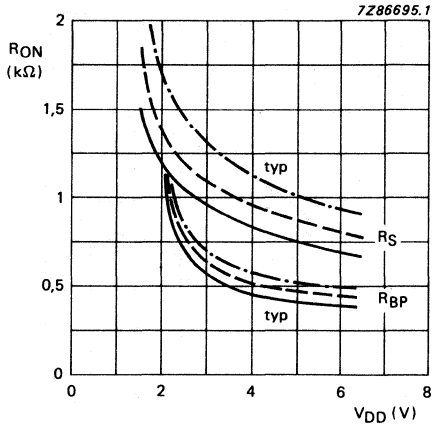


Fig. 22 Output resistance of backplane and segments.
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

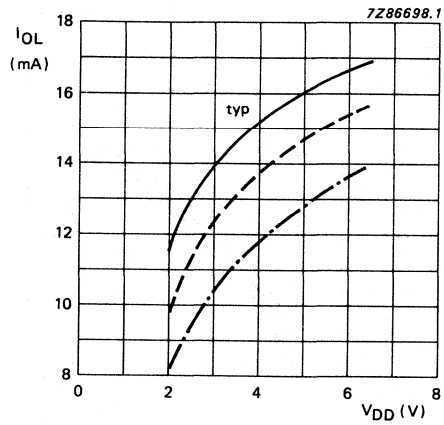


Fig. 23 Output current as a function of supply voltage (only PCF2112).
——— T_{amb} = −40 °C;
– – – – T_{amb} = + 25 °C;
– . – . – T_{amb} = + 85 °C.

VOICE SYNTHESIZER

GENERAL DESCRIPTION

The PCF8200 is a CMOS integrated circuit for generating good quality speech from digital code with a programmable bit rate. The circuit is primarily intended for applications in microprocessor controlled systems, where the speech code is stored separately.
Applications include automotive, telephony, personal computers, annunciators, aids for the handicapped, and general industrial devices.

Features

- Male and female speech with good quality
- Speech-band from 0 to 5 kHz
- Bit-rate between 455 bits/second and 4545 bits/second
- Programmable frame duration
- Programmable speaking speed
- CMOS technology
- Operating temperature range −40 to + 85 °C
- Single 5 V supply with low power consumption and power-down stand-by mode
- Interfaces easily with most popular microcomputers and microprocessors through 8 bit parallel bus or I^2C bus
- Software readable status word (parallel bus or I^2C bus)
- BUSY-signal and $\overline{REQ}$-signal hardware readable
- Internal low-pass filter and 11-bit D/A converter

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	–	5	–	V
Supply current	I_{DD}	–	12	#	mA
Supply current (stand-by)	$I_{DD(SB)}$	–	1	–	μA
Inputs					
Input voltage	V_{IH}	2,0	–	V_{DD}	V
Input voltage	V_{IL}	0	–	0,8	V
Input capacitance	C_I	–	7	–	pF
Outputs (D5 to D7)					
Output voltage high	V_{OH}	3,5	–	V_{DD}	V
Output voltage low	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Operating ambient temperature range	T_{amb}	−40	–	+ 85	°C

Value not yet available.

PACKAGE OUTLINE

24-lead DIL; plastic (SOT101A).

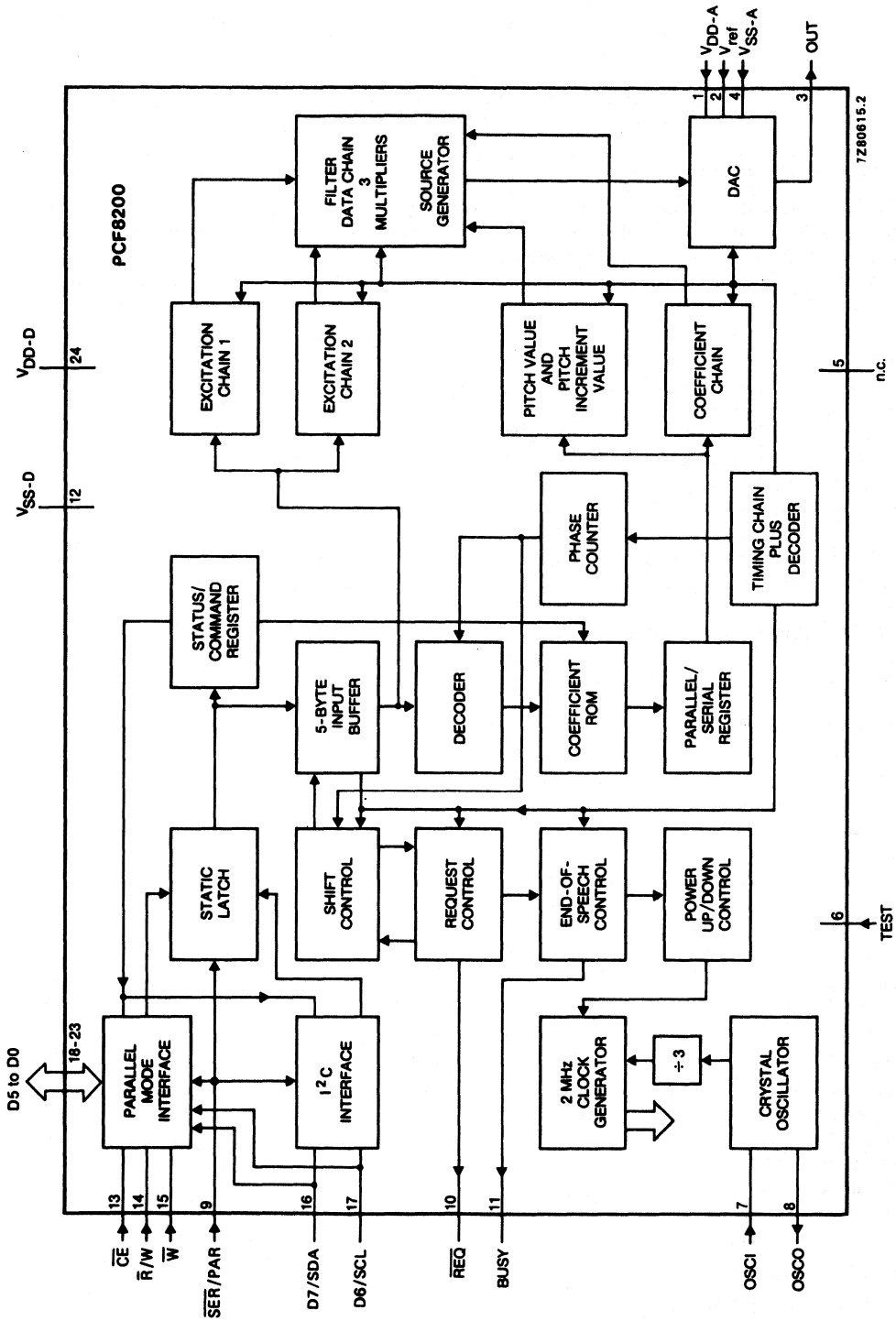


Fig. 1 Block diagram.

PINNING

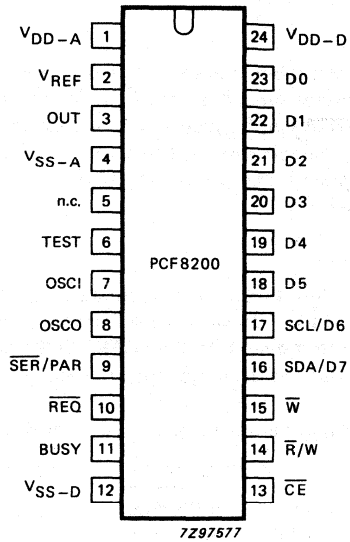


Fig. 2 Pinning diagram.

DEVELOPMENT DATA

1	V_{DD-A}	positive supply voltage for DAC output stage
2	V_{REF}	DAC reference voltage input
3	OUT	speech output
4	V_{SS-A}	negative supply voltage for DAC stage
5	n.c.	not connected
6	TEST	for normal operation this pin must be grounded (V_{SS})
7	OSCI	oscillator input
8	OSCO	oscillator output
9	$\overline{SER}$/PAR	for parallel data bus operation this pin is hard-wired to V_{DD}, or to V_{SS} to enable the I^2C bus
10	$\overline{REQ}$	status bit indicating request for data
11	BUSY	status indicating synthesizer busy
12	V_{SS-D}	negative supply voltage for digital circuits
13	$\overline{CE}$	chip-enable input
14	R/$\overline{W}$	read/write control input
15	$\overline{W}$	write input
16	SDA/D7	I^2C bus serial data input/output (serial mode) or parallel data input/output D7 (parallel mode)
17	SCL/D6	I^2C bus serial clock input/output (serial mode) or parallel data input/output D6 (parallel mode)
18	D5	parallel data input/outputs
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	V_{DD-D}	positive supply voltage for digital circuits

FUNCTIONAL DESCRIPTION

The synthesizer has been designed for a vocal tract modelling technique of voice synthesis. An excitation signal is fed to a series of resonators. Each resonator simulates one of the formants in the original speech. It is controlled by two parameters, one for the resonant frequency and one for the bandwidth. Five formants are needed for male speech and four for female speech. The output of this system is defined by the excitation signal, the amplitude values and the resonator settings. By periodic updating of all parameters very high quality speech can be produced.

OPERATION

Speech characteristics change quite slowly, therefore the control parameters for the speech synthesizer can be adequately updated every few tens of milliseconds with interpolation during the interval to ensure a smooth changeover from one parameter value to the next. In the PCF8200 the standard-frame duration can be set to 8,8 , 10,4, 12,8 or 17,6 milliseconds with the speed-option, speaking speed, in the command-register.
The duration of each individual speech frame is programmable to be 1, 2, 3 or 5 times the standard-frame duration.

FD1, FD0	10	01	00	11	FS0, FS1
00	8,8	10,4	12,8	17,6	ms
01	17,6	20,8	25,6	35,2	ms
10	26,4	31,2	38,4	52,8	ms
11	44,0	52,0	64,0	88,0	ms

Table 1. Frame duration as a function of speed-option (FS1, FS0) and frame-duration (FD1, FD0).

The excitation signal is a random noise source for unvoiced sounds and a programmable pulse generator for voiced sounds. Both sources have an amplitude modulator which is updated 8 times in one speech-frame by linear interpolation. The pitch is updated every 1/8 of a standard frame.

The excitation signal is filtered with a five formant filter for male speech and a four formant filter for female speech. The formant filter is a cascade of all second-order sections. The control parameters, formant-frequency and formant-bandwidth, are updated eight times per speech frame by linear interpolation.
A block diagram of the formant synthesizer is shown in Fig. 3.

The filter output is upsampled to 80 kHz and filtered with a digital low-pass filter. Before the signal is digital to analogue converted (DAC), with an 11-bit switched capacitor DAC, the signal is multiplied with a DAC-amplitude factor. The use of a digital filter means that no external audio filtering is required for low-medium applications and minimal filtering is required for those applications requiring very high quality speech.

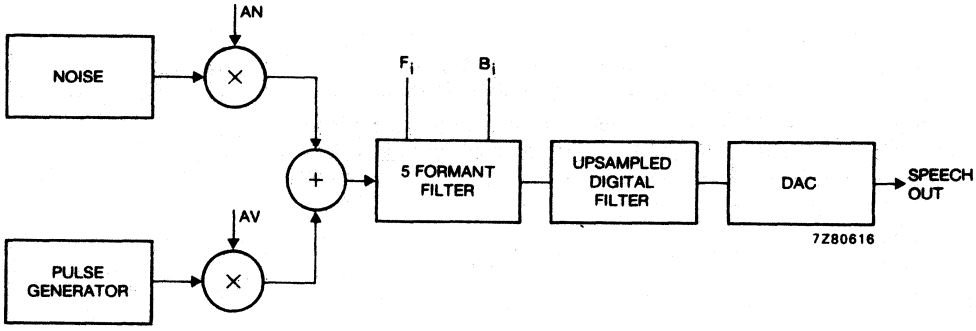


Fig. 3 Block diagram of formant synthesizer.

DATA FORMAT

Three types of format are used for data transfer to the synthesizer.

DAC-amplitude factor

The DAC-amplitude factor is one byte, which is used to optimize the digital speech signal to the 11-bit DAC. It is the first byte after a STOP or a BADSTOP or V_{DD} on. Table 2 indicates the amplitude factor.

byte	factor	dB
01110000	3,5	10,88
10110000	3,25	10,24
00110000	3,0	9,54
11010000	2,75	8,97
01010000	2,5	7,96
10010000	2,25	7,04
00010000	2,0	6,02
11100000	1,75	4,86
01100000	1,5	3,52
10100000	1,25	1,94
00100000	1,0	0,00
11000000	0,75	−2,50
01000000	0,5	−6,02
10000000	0,25	−12,04
00000000	0,0	
11110000	HEX code F0 is not allowed as a DAC amplitude	

Table 2 DAC amplitude factor.

Start pitch

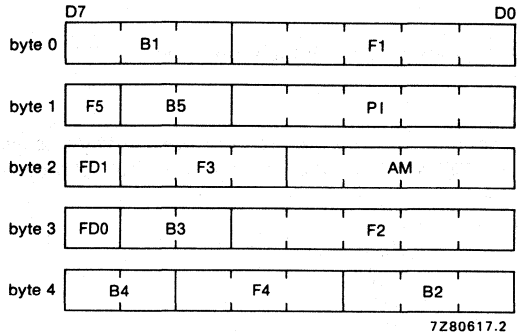
The second byte after a STOP or BADSTOP, or V_{DD} on is the start pitch. It is a one byte start value for the on-chip pitch-period generator.

Frame Data

The frame data is a five byte block which contains the filter and source information:

pitch increment/decrement value	5 bits
amplitude	4 bits
frame duration	2 bits
frequency of 1st formant	5 bits
frequency of 2nd formant	5 bits
frequency of 3rd formant	3 bits
frequency of 4th formant	3 bits
frequency of 5th formant	1 bit
bandwidth of 1st formant	3 bits
bandwidth of 2nd formant	3 bits
bandwidth of 3rd formant	2 bits
bandwidth of 4th formant	2 bits
bandwidth of 5th formant	2 bits
	40 bits = 5 bytes

The frame-data bits are organized as shown in Fig. 4.



It is not allowed to set byte 0 to the hexadecimal value 00.

Fig. 4 Format of frame-date.

CONTROL FORMAT

Command Write

A command write consists of two bytes, and it may occur before a data block. The four bits which can be written are shown in Fig. 5.

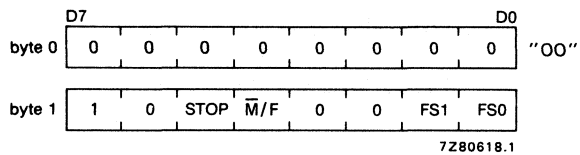


Fig. 5 Control write: first byte fixed, second byte control.

FS0, FS1 speed option

FS1	FS0	speech speed	standard-frame duration
0	0	100%	12,8 ms
0	1	145%	8,8 ms
1	0	123%	10,4 ms
1	1	73%	17,6 ms

$\overline{M}$/F, male/female option

$\overline{M}$/F = 0 male quantization table
= 1 female quantization table

STOP

STOP = 1 stop; repeat last complete frame with amplitude = 0 (no excitation signal)
= 0 if the frame data is not sent within the duration of a half frame, there will be a BADSTOP:

1. $\overline{REQ}$ = 1 STOP = 0
2. Repeat last frame with amplitude = 0
3. BUSY = 0

Status Read

Three status bits can be read out at any time without a preceding byte (00).
This is shown in Fig. 6.

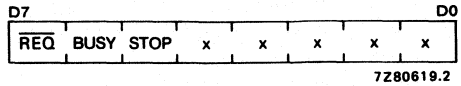


Fig. 6 Status read.

$\overline{REQ}$	= 1	No data required
	= 0	Synthesizer requesting for new data
BUSY	= 1	Busy (an utterance is pronounced)
	= 0	Idle, $\overline{REQ}$ will set to 1; the synthesizer is in STOP or BADSTOP mode
STOP		The STOP bit is the same as the stop bit written to the synthesizer during a command write.
		STOP = 1, BUSY = 0 stopped by the user.
		STOP = 0, BUSY = 0 BADSTOP because the data was not sent in time.

After initial power-up the status/command register is set to the following status:

FS0, FS1	= 0	Standard-frame duration of 12,8 ms
$\overline{M}$/F	= 0	Male quantization table
STOP	= 0	
BUSY	= 0	Idle
$\overline{REQ}$	= 1	No data required

DEVELOPMENT DATA

INTERFACE PROTOCOL

Data can be written to the synthesizer when $\overline{REQ}$ = 0 or, when $\overline{REQ}$ = 1 and BUSY = 0. Figure 7 shows the interface protocol of the synthesizer.

In parallel mode the synthesizer is activated by sending the DAC-amplitude factor. In serial mode the DAC-amplitude factor can be sent as soon as the synthesizer is powered-up.

The I²C transmitter/receiver will then acknowledge. When the request for the pitch-byte occurs the byte must be provided within the duration of a half standard frame. If the byte is not provided in time a BADSTOP will be generated.

During each data write operation, the status bit $\overline{REQ}$ will be set to '1'.
Within a frame data block, it disappears within a few microseconds, asking for the next byte of that block. If the bytes of frame data are not provided within the time-duration of a half frame, a BADSTOP will be generated.

I²C ADDRESS

On chip there is a I²C slave receiver/transmitter with the address:

7 6 5 4 3 2 1 0
0 0 1 0 0 0 0 R/W

POWER UP

The synthesizer will be set to power-up on a parallel-write sequence.

PAR-mode: The input-latches are active so they can receive the first byte

SER-mode: The I^2C transmitter/receiver will not acknowledge until the synthesizer has powered-up. To power up the synthesizer a parallel write sequence (Fig. 9) must be made to the synthesizer by using external logic for the control lines; at least one line must be toggled, $\overline{CE}$, while $\overline{W} = 0$ and $\overline{R}/W = 1$.
The synthesizer can be set to permanent power-up by hard-wired control pins ($\overline{CE} = 0$, $\overline{R}/W = 1$, $\overline{W} = 0$).

POWER DOWN MODE

When BUSY = 0 the synthesizer will be set to power-down. In the power-down mode the status/command register will be retained.
In power-down mode the clock-oscillator is switched off. After initial V_{DD} the synthesizer is in power-down mode.

HANDLING

All inputs and outputs are protected against electrostatic charge under normal handling conditions.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	conditions	symbol	min.	max.	unit
Supply voltage	any pin with respect to V_{SS}	V_{DD}	−0,3	7,5	V
Input voltage	any pin with respect to V_{SS}	V_I	−0,3	7,5	V
Output voltage	any pin with respect to V_{SS}	V_O	−0,3	7,5	V
D.C. input diode current	$V_I < V_{SS}$	$-I_{IK}$	–	20	mA
	$V_I > V_{DD}$	I_{IK}	–	20	mA
D.C. output diode current	$V_O < V_{SS}$	$-I_{OK}$	–	20	mA
	$V_O > V_{DD}$	I_{OK}	–	20	mA
Operating ambient temperature range		T_{amb}	−40	85	°C
Storage temperature range		T_{stg}	−55	125	°C

CHARACTERISTICS

T_{amb} = −45 to + 85 °C; supply voltage (V_{DD} to V_{SS}) = 4,5 to 5,5 V with respect to V_{SS}, unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	10	–	mA
Standby current	$I_{DD(SB)}$	–	200	–	μA
Inputs					
$\overline{CE}$, R/$\overline{W}$, $\overline{W}$					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
OSCI					
Input voltage HIGH	V_{IH}	2,2	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current V_{in} = 0 to 5,5 V	I_{IR}	−10	–	10	μA
Rise and fall times (note 2)	t_{rf}	–	–	50	ns
Input capacitance	C_I	–	–	7	pF
PARALLEL MODE					
Input Characteristics (D0 to D7)					
Input voltage HIGH	V_{IH}	2,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	0,8	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	7	pF
Output Characteristics (D5 to D7 only)					
Output voltage HIGH (I_{OH} = −100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
SERIAL MODE					
Input characteristics (SDA and SDL)					
Input voltage HIGH	V_{IH}	3,0	–	V_{DD}	V
Input voltage LOW	V_{IL}	0	–	1,5	V
Input leakage current (V_{in} = 0 to 5,5 V, output off)	I_{IR}	−10	–	10	μA
Input capacitance	C_I	–	–	10	pF

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Output Characteristics (SDA only, open drain)					
Output voltage LOW (I_{OL} = 3 mA)	V_{OL}	0	–	0,4	V
OSCILLATOR					
Crystal frequency	f_{XTAL}	–	6	6,1	MHz
V_{REF}					
Reference voltage	V_{REF}	1,9	–	$\frac{V_{DD}-1,5}{1,25}$	V
Input leakage current (active)	I_{IR}	–	5	–	μA
Outputs					
$\overline{REQ}$, BUSY					
Output voltage HIGH (I_{OH} = 100 μA)	V_{OH}	3,5	–	V_{DD}	V
Output voltage LOW (I_{OL} = 3,2 mA)	V_{OL}	0	–	0,4	V
Load capacitance	C_L	–	–	80	pF
Rise and fall times (note 3)	t_{rf}	–	–	50	ns
OUT					
Output voltage	V_{OUT}	0,66 x V_{REF}		1,34 x V_{REF}	V
Minimum external load		600	–	–	Ω
Timing characteristics (note 1) (Figs 8 and 9)					
Write enable	t_{WR}	200	–	–	ns
Data set-up for write	t_{DS}	150	–	–	ns
Data hold for write	t_{DH}	30	–	–	ns
Read enable	t_{RD}	200	–	–	ns
Data delay for read (note 2)	t_{DD}	–	–	150	ns
Data floating for read (note 2)	t_{DF}	–	–	150	ns
Control set-up	t_{CS}	0	–	–	ns
Control hold	t_{CH}	0	–	–	ns
REQ new (new byte of the same speech frame)	t_{RN}	–	# (≈ 3)		μs
REQ Valid	t_{RV}	0	–	–	ns
REQ Hold	t_{RH}	–	250	#	ns

NOTES TO THE CHARACTERISTICS

1. Timing reference level is 1,5 V; supply 5 V ± 10%; temperature range of −40 °C to 85 °C.
2. Levels greater than 2 V for a '1' or less than 0,8 V for a '0' are reached with a load of one TTL input and 50 pF.
3. Rise and fall times between 0,6 V and 2,2 V levels.

Values not yet available.

DEVELOPMENT DATA

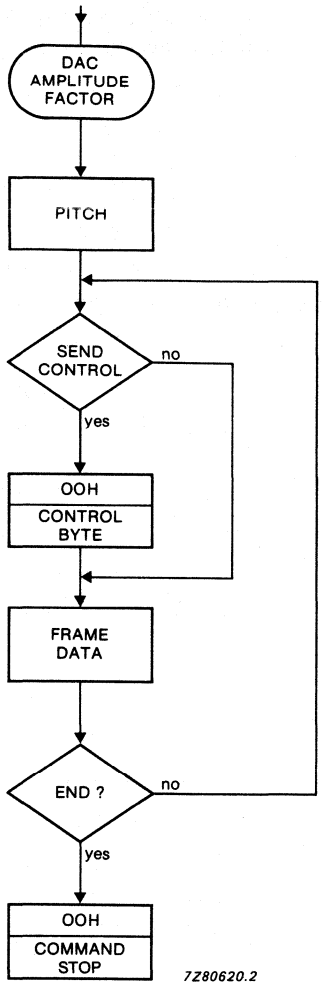
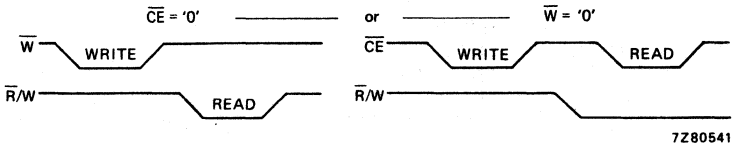


Fig. 7 Interface protocol.

Timing diagrams

The control signals $\overline{CE}$, $\overline{R}/W$ and $\overline{W}$ have been specified to enable easy interface to most microprocessors and microcomputers. For instance with connection to an MAB8048 microcomputer the $\overline{R}/W$ and $\overline{W}$ inputs can be used as the RD and WR strobe inputs.



Typical connection of control signals.

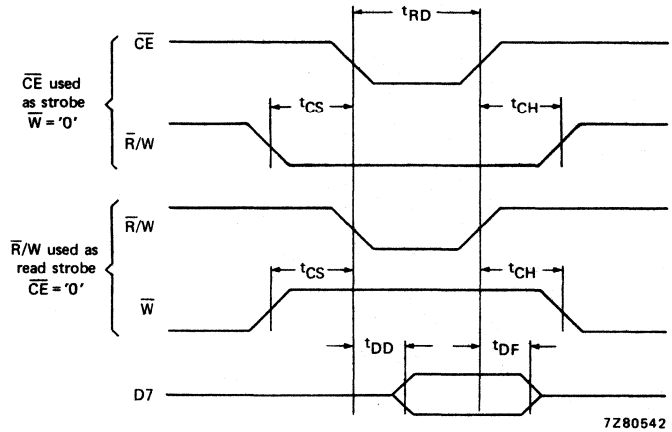


Fig. 8 Read timing.

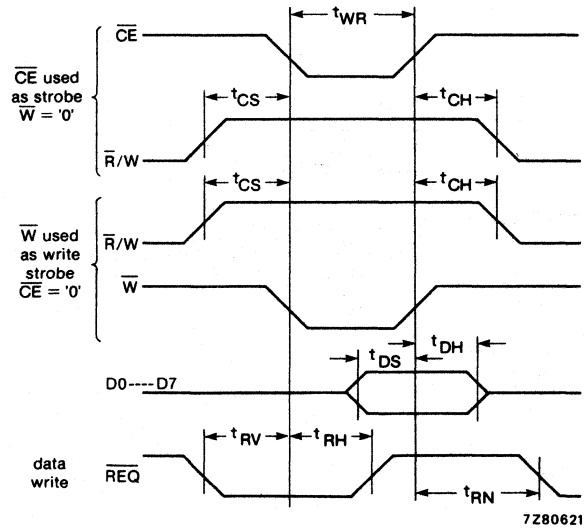


Fig. 9 Write timing.

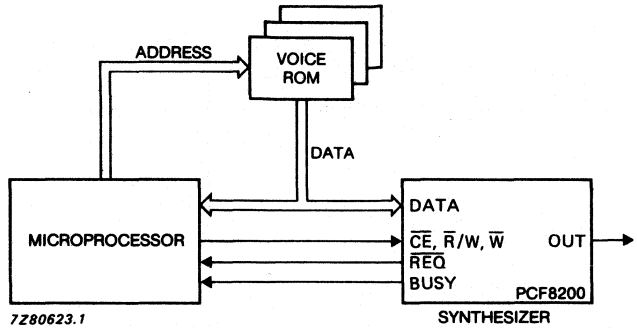


Fig. 10 Typical application configuration with parallel interface.

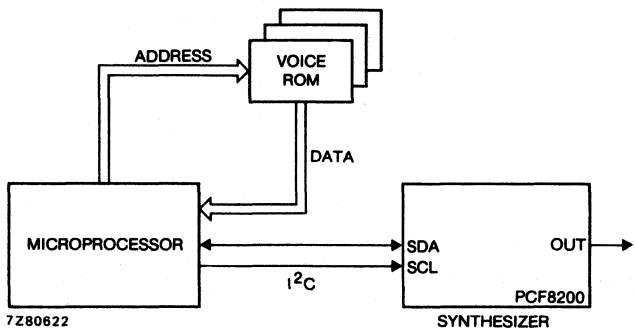


Fig. 11 Typical application configuration with series interface.

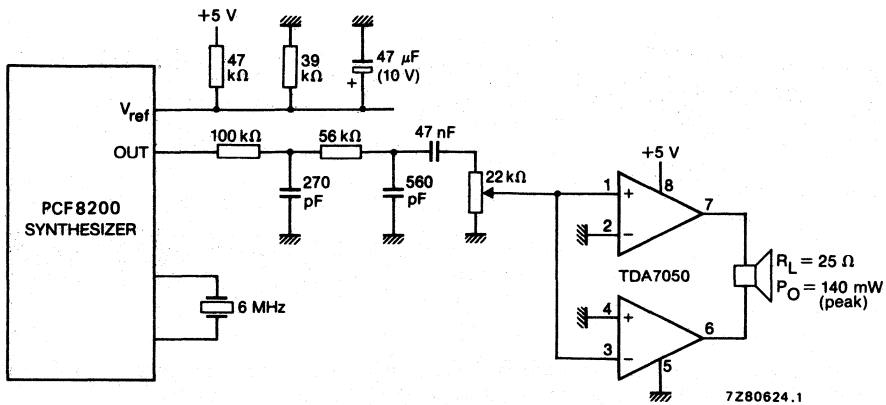


Fig. 12 An example of an output configuration.

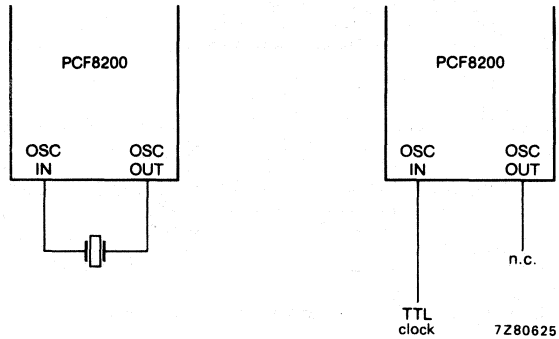


Fig. 13 Oscillator clock configurations.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

SINGLE-CHIP 8-BIT MICROCONTROLLER

DESCRIPTION

An advanced CMOS process is used to manufacture the PCF84CXX family of microcontrollers. The family consists of the following devices:

- PCF84C00 – 256 x 8 RAM, external program memory
- PCF84C21 – 2 K x 8 ROM, 64 x 8 RAM
- PCF84C41 – 4 K x 8 ROM, 128 x 8 RAM
- PCF84C81 – 8 K x 8 ROM, 256 x 8 RAM

Each version has 20 quasi-bidirectional I/O port lines, a serial I/O interface, a single-level vectored interrupt structure, an 8-bit timer/event counter and on-chip clock oscillator and clock circuits.

Each member of this microcontroller family is an efficient controller as well as an arithmetic processor. The instruction set is similar to that of the MAB8048 and the PCF84CXX family is pin- and instruction set compatible with the MAB8400 family.
The microcontrollers have facilities for both binary and BCD arithmetic plus bit-handling capabilities.

For detailed information see the user manual "Single-chip 8-bit microcontrollers".

Features

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead DIL or SO package
- 2 K, 4 K or 8 K x 8 ROM; also a ROM-less version
- 64, 128 or 256 x 8 RAM
- 20 quasi-bidirectional I/O port lines
- Two test inputs: one of which is also the external interrupt input
- Single-level vectored interrupts: external, timer/event counter, serial I/O
- I^2C hardware interface for serial data transfer on two lines (serial I/O data via an existing port line and clock via a dedicated line)
- 8-bit programmable timer/event counter
- Clock frequency range: 100 kHz to 10 MHz
- Over 80 instructions (similar to those of the MAB8048) all of 1 or 2 cycles
- Single supply voltage (2,5 V to 5,5 V)
- STOP and IDLE modes
- Power-on-reset circuit
- Operating temperature range: −40 to +85 °C
- High current output on Port 1: I_{OL} = 10 mA at V_{OL} = 1,2 V (all versions except the PCF84C00)

PACKAGE OUTLINES

PCF84C21/41/81P : 28-lead DIL; plastic (SOT117).
PCF84C21/41/81T : 28-lead mini-pack; plastic (SO28; SOT136A).
PCF84C00B : 28-lead 'piggy-back' package (with up to 28-pin EPROM on top).
PCF84C00T : 56-lead mini-pack; plastic (VSO56; SOT190).

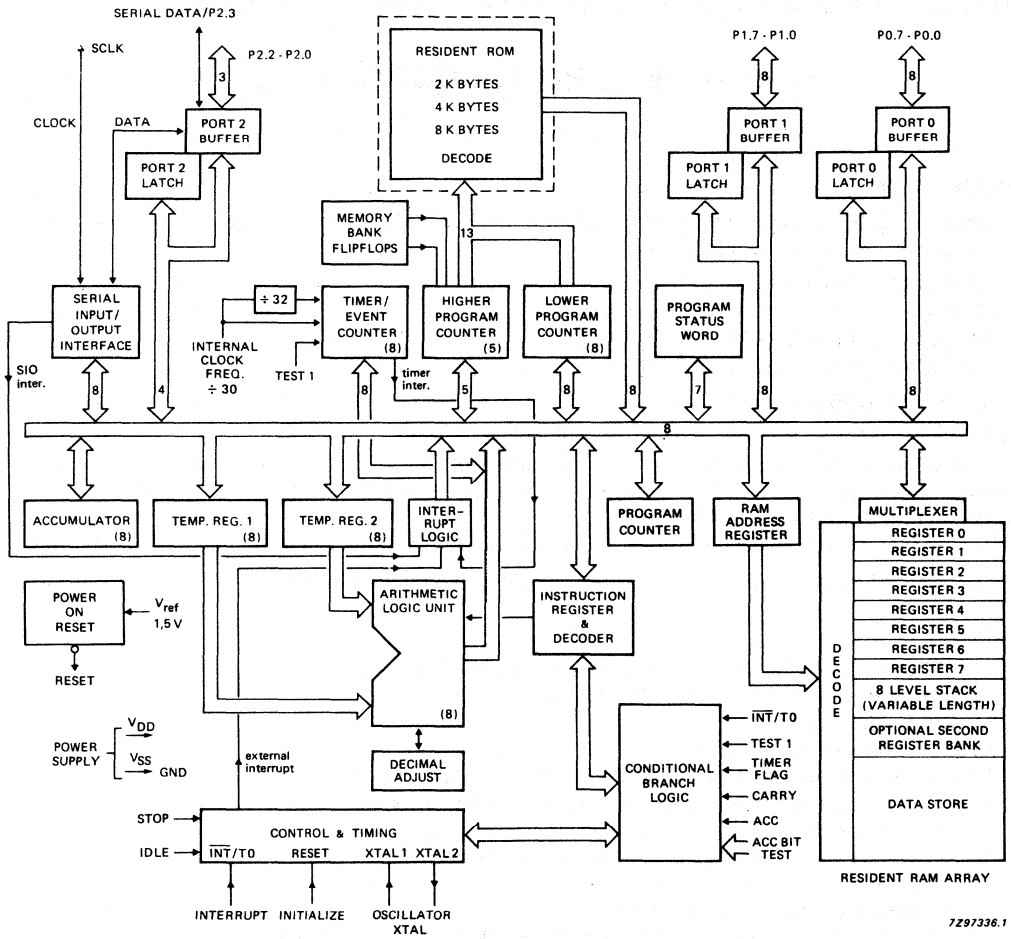


Fig. 1 PCF84CXX block diagram.

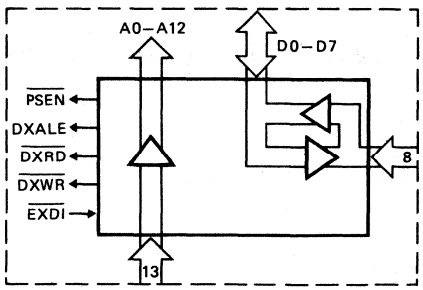


Fig. 1a Replacement of dotted section in Fig. 1, for the PCF84C00T ROM-less version.

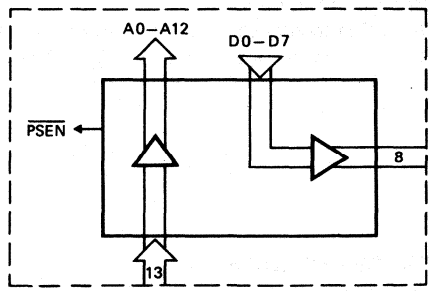


Fig. 1b Replacement of dotted section in Fig. 1, for the PCF84C00B 'piggy-back' version.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8566 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 24 segment drives: up to twelve 8-segment numeric characters; up to six 15-segment alphanumeric characters; or any graphics of up to 96 elements
- 24 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- 2,5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with the 40 segment LCD driver PCF8576
- Optimized pinning for single plane wiring in both single and multiple PCF8566 applications
- Space-saving 40-lead plastic mini-pack (VSO-40; SOT-158A)
- No external components required (even in multiple device applications)
- Manufactured in silicon gate CMOS process

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

PACKAGE OUTLINES

PCF8566P: 40-lead DIL; plastic (SOT129).
PCF8566T: 40-lead mini-pack (VSO40; SOT158A).

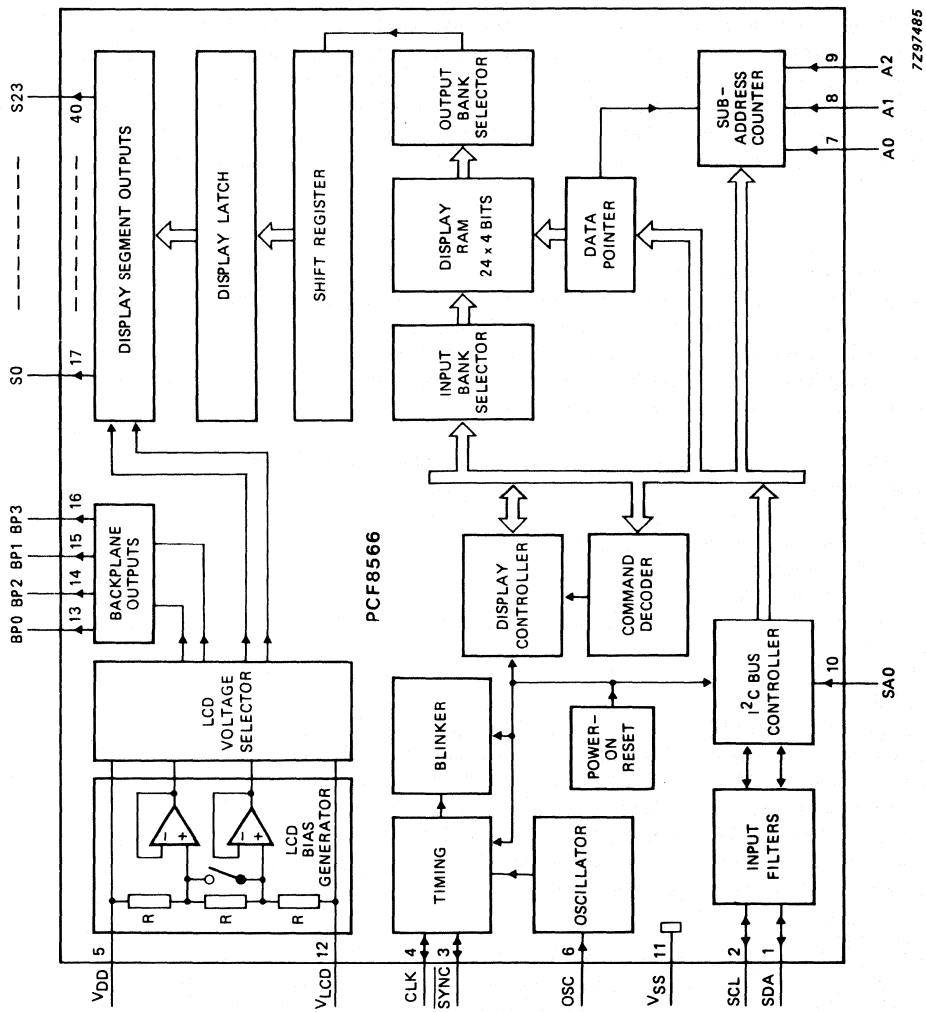


Fig. 1 Block diagram.

DEVELOPMENT DATA

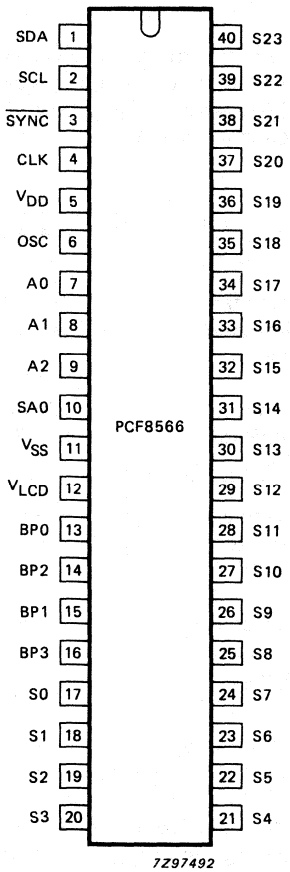


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{SYNC}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	I^2C bus subaddress inputs
9	A2	I^2C bus subaddress inputs
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	LCD backplane outputs
15	BP1	LCD backplane outputs
16	BP3	LCD backplane outputs
17 to 40	S0 to S23	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8566 is a versatile peripheral device designed to interface any microprocessor to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 24 segments. The display configurations possible with the PCF8566 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	96	12 digits + 12 indicator symbols	6 characters + 12 indicator symbols	96 dots (4 x 24)
3	72	9 digits + 9 indicator symbols	4 characters + 16 indicator symbols	72 dots (3 x 24)
2	48	6 digits + 6 indicator symbols	3 characters + 6 indicator symbols	48 dots (2 x 24)
1	24	3 digits + 3 indicator symbols	1 characters + 10 indicator symbols	24 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the two-line I²C bus communication channel with the PCF8566. The internal oscillator is selected by tying OSC (pin 6) to V_{SS}. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

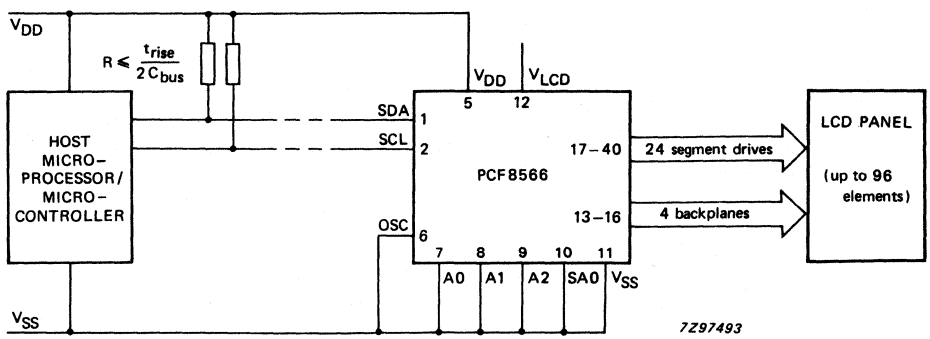


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8566 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

DEVELOPMENT DATA

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\ V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex). The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\ V_{off(rms)} = 2{,}449\ V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\ V_{off(rms)} = 2{,}309\ V_{off(rms)}$

These compare with $V_{op} = 3\ V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

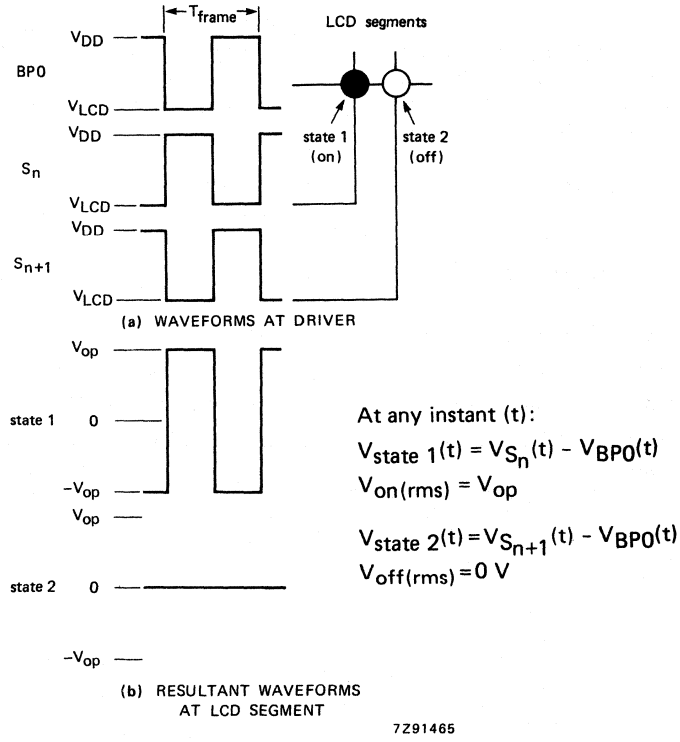


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8566 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

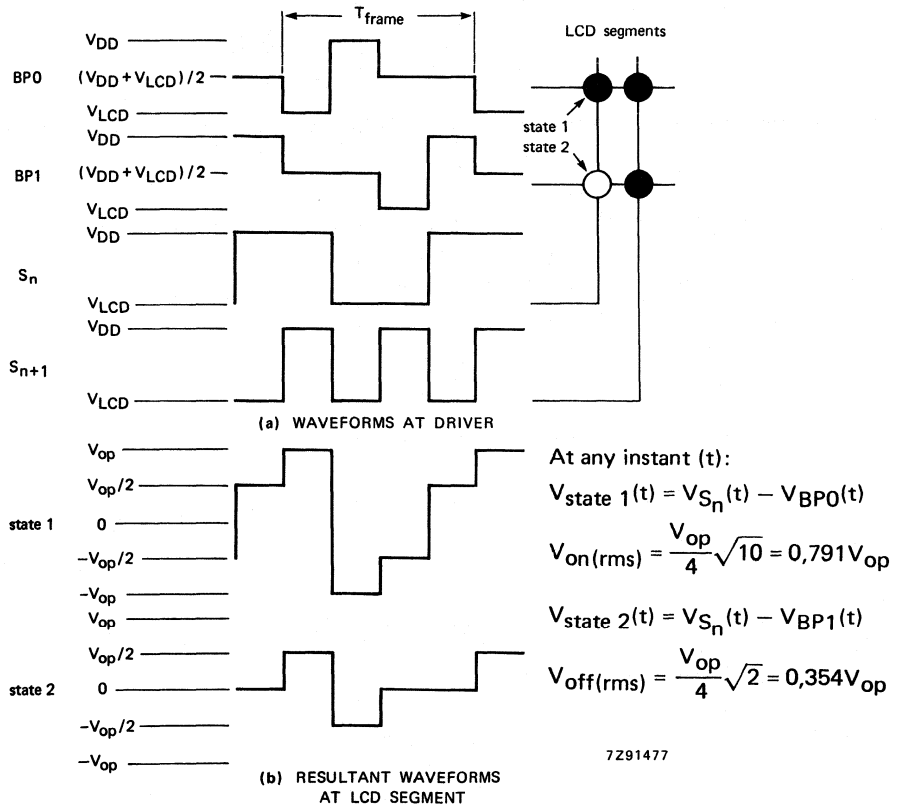


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

DEVELOPMENT DATA

LCD drive mode waveforms (continued)

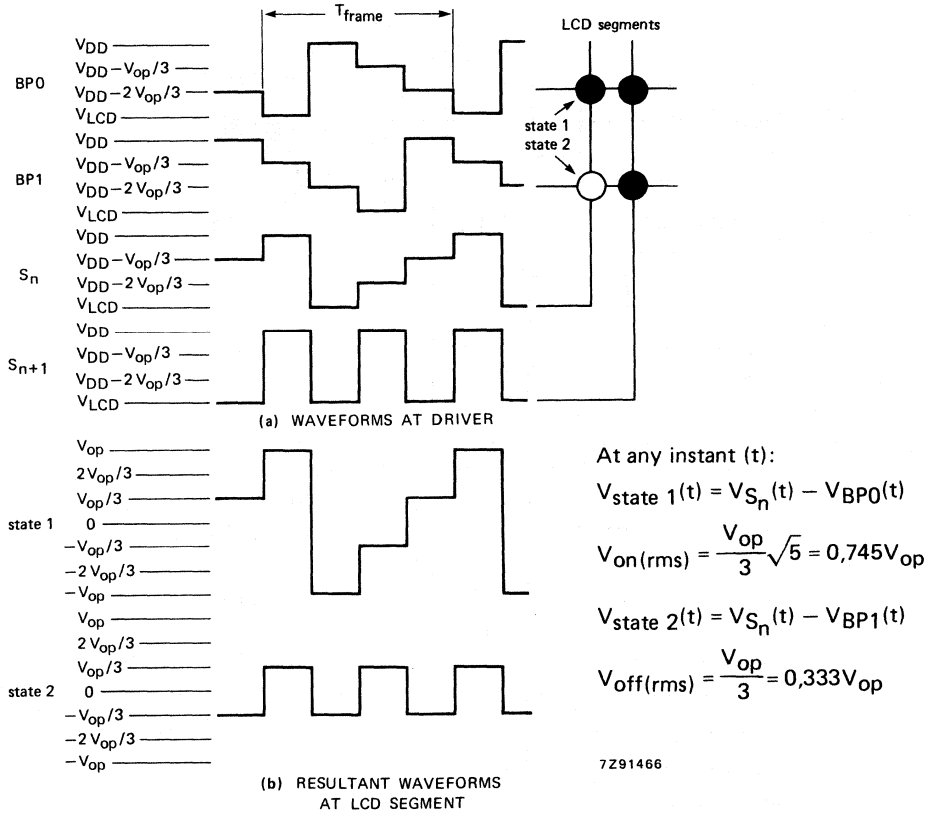


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive wavefront for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

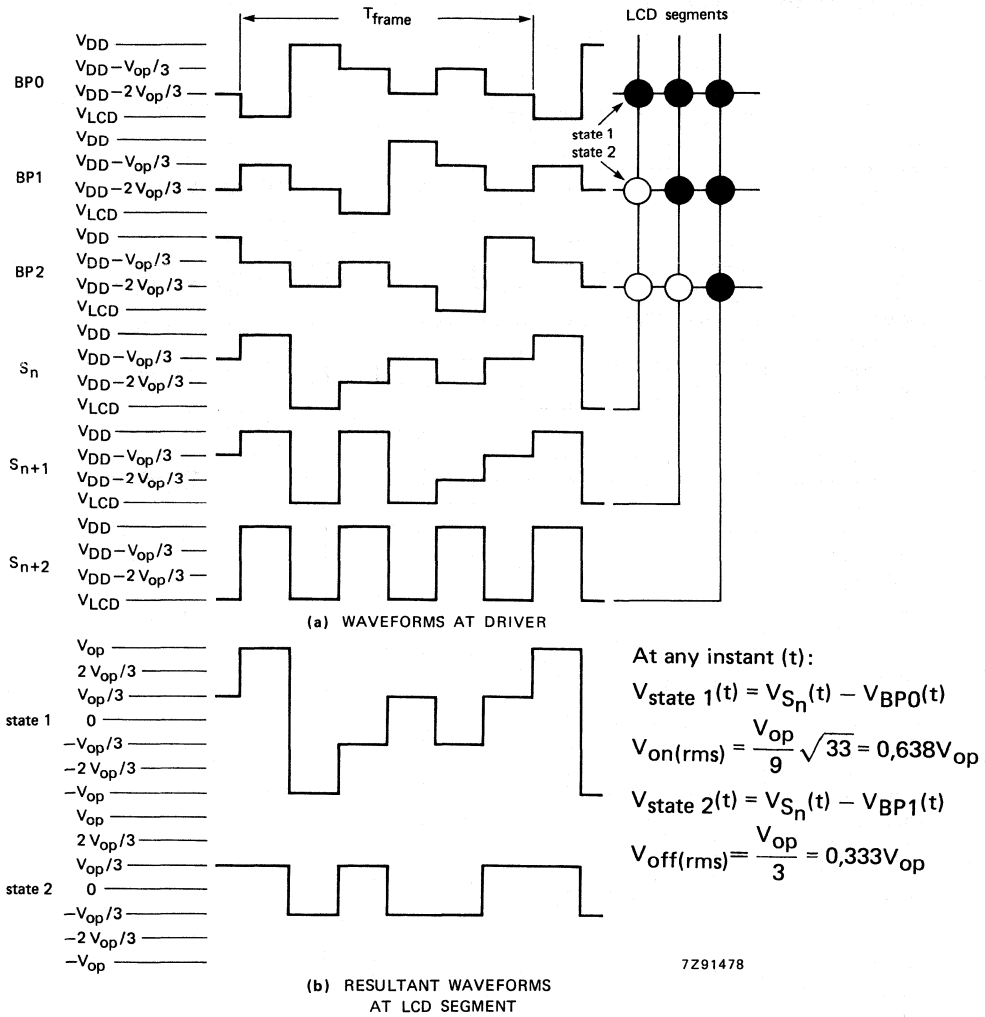


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

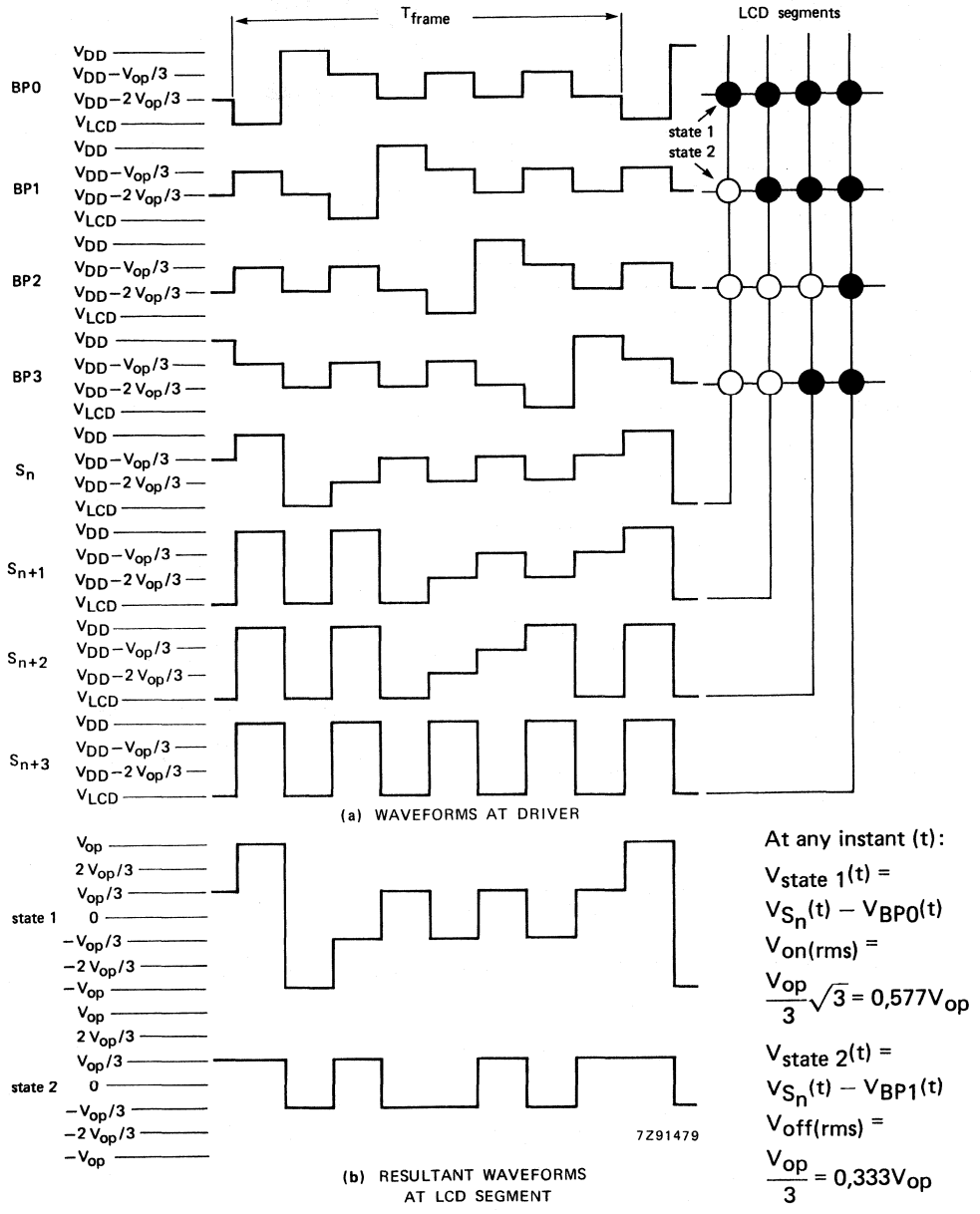


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

The internal logic and the LCD drive signals of the PCF8566 or PCF8576 are timed either by the built-in oscillator or from an external clock.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I^2C bus. To allow I^2C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state.

Internal clock

When the internal oscillator is used, OSC (pin 6) should be tied to V_{SS}. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8566s and PCF8576s in the system.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

Timing

The timing of the PCF8566 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by MODE SET commands when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8566 mode	f_{frame}	nominal f_{frame} (Hz)
normal mode	$f_{CLK}/2880$	64
power-saving mode	$f_{CLK}/480$	64

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller, this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line low until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 (pins 17 to 40) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 24 segment outputs are required the unused segment outputs should be left open-circuit.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 24 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 24 segments operated with respect to backplane BP0 (Fig. 9). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

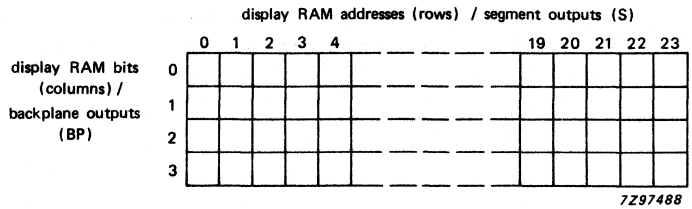


Fig. 9 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8566 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 10; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 10, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 10. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). A0, A1 and A2 should be tied to V_{SS} or V_{DD}. The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character.

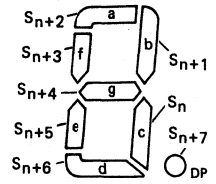
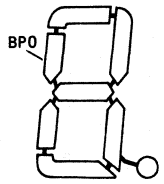
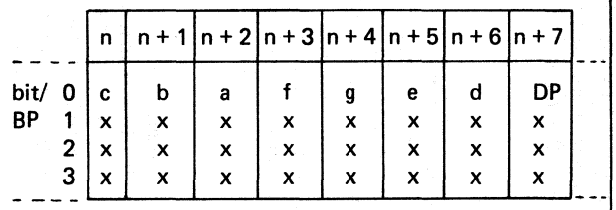
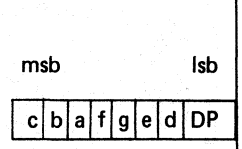
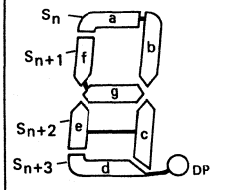
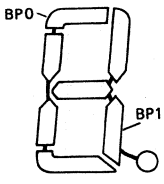
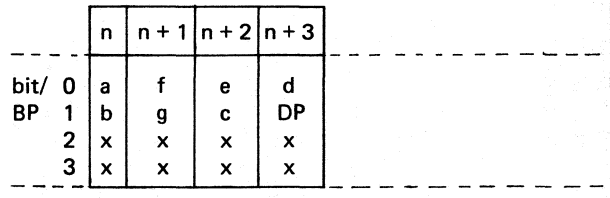
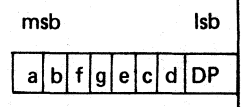
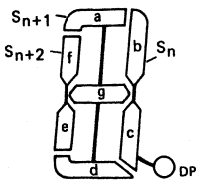
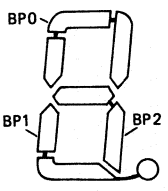
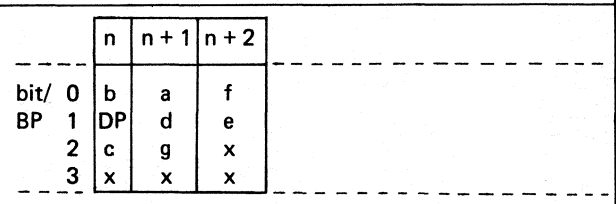
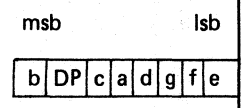
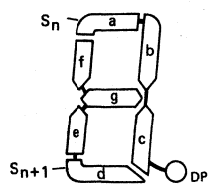
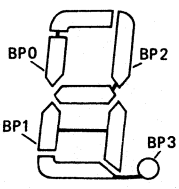
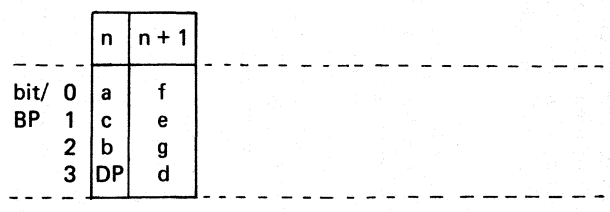
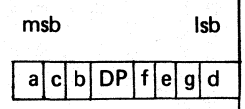
drive mode	LCD segments	LCD backplanes	display RAM filling order	transmitted display byte
static				
1 : 2 multiplex				
1 : 3 multiplex				
1 : 4 multiplex				

Fig. 10 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

7Z91469

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

DEVELOPMENT DATA

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

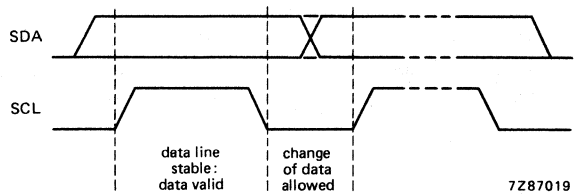


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

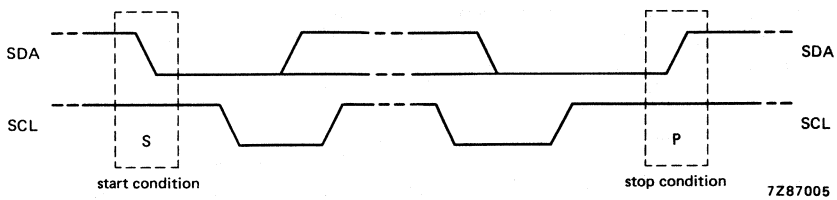


Fig. 12 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

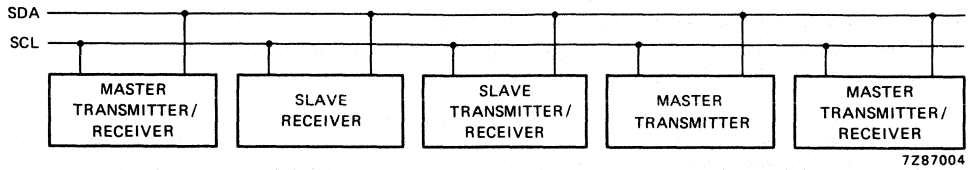


Fig. 13 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

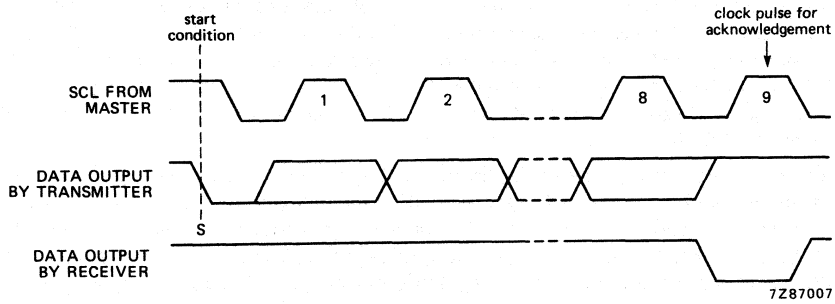


Fig. 14 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are available on request.

PCF8566 I²C bus controller

The PCF8566 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally left open-circuit or tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are left open-circuit or tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111110 and 0111111) are reserved for PCF8566. The least-significant bit of the slave address that a PCF8566 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8566 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8566s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 15. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8566 slave addresses available. All PCF8566s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8566s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8566 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8566. After the last display byte, the I²C bus master issues a stop condition (P).

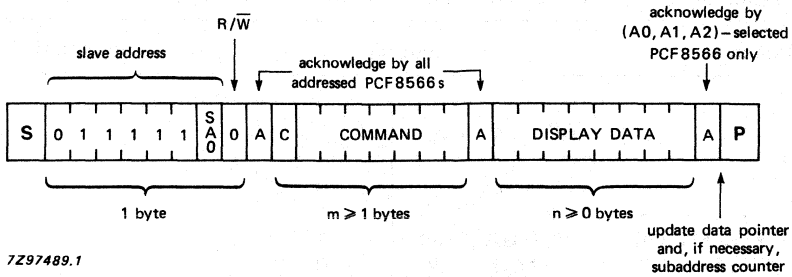


Fig. 15 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 16). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

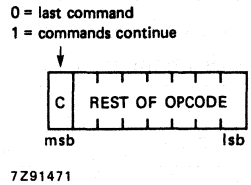


Fig. 16 General format of command byte.

The five commands available to the PCF8566 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8566 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 0 P4 P3 P2 P1 P0	bits P4 P3 P2 P1 P0 5-bit binary value of 0 to 23	Five bits of immediate data, bits P4 to P0, are transferred to the data pointer to define one of twenty-four display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

DEVELOPMENT DATA

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C | 1 | 1 | 1 | 1 | 0 | I | O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C | 1 | 1 | 1 | 0 | A | BF1 | BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0,5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8566s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8566s. When cascaded, several PCF8566s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (Fig. 17).

The $\overline{SYNC}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{SYNC}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8566s with differing SA0 levels are cascaded). $\overline{SYNC}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{SYNC}$ line at the onset of its last active backplane signal and monitors the $\overline{SYNC}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8566 to assert $\overline{SYNC}$. The timing relationships between the backplane waveforms and the $\overline{SYNC}$ signal for the various drive modes of the PCF8576 are shown in Fig. 18. The waveforms are identical with the parent device PCF8576. Casadability between PCF8566s and PCF8576s is possible, giving cost effective LCD applications.

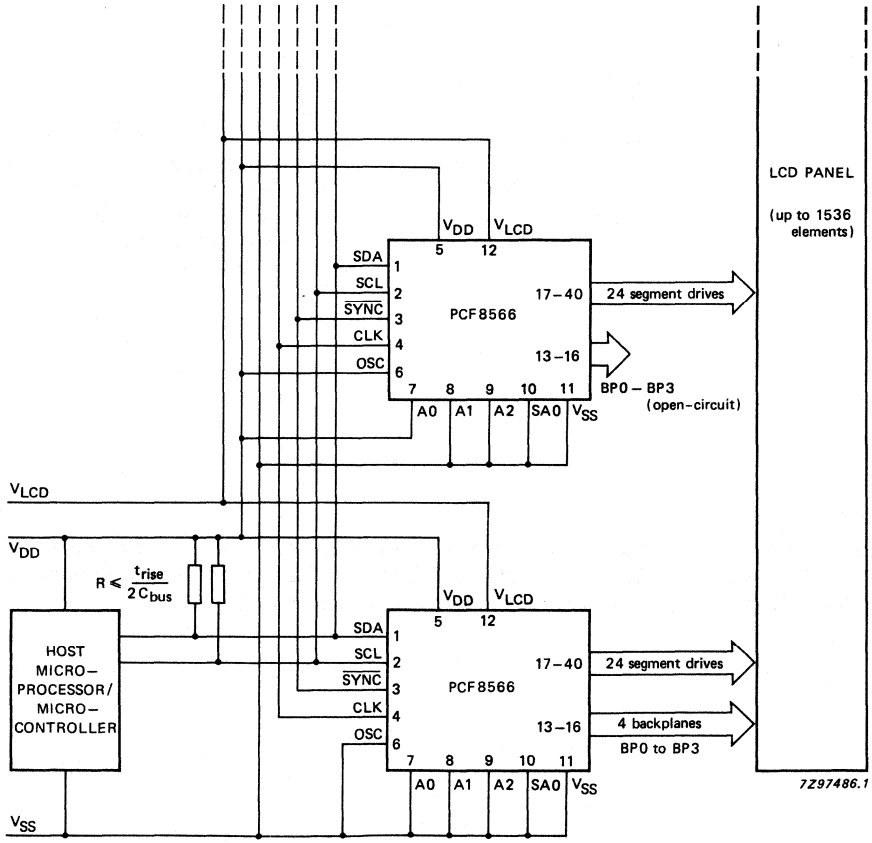


Fig. 17 Cascaded PCF8566 configuration.

DEVELOPMENT DATA

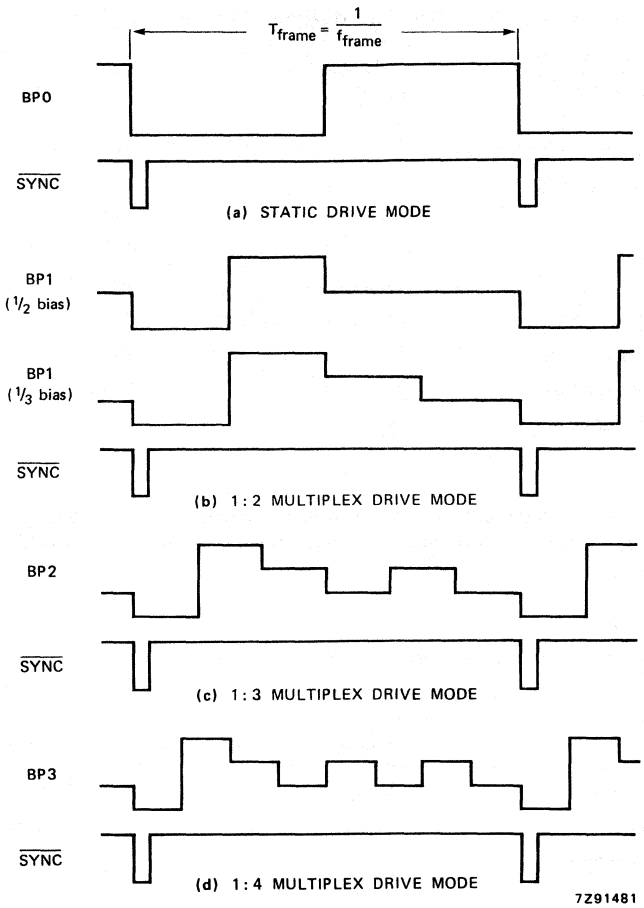


Fig. 18 Synchronization of the cascade for the various PCF8566 drive modes.

For single plane wiring of PCF8566s, see section "APPLICATION INFORMATION".

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range; see note	V_{DD}		−0,5 to + 7 V
LCD supply voltage range	V_{LCD}		V_{DD} −7 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S23; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
DC input current	$\pm I_I$	max.	20 mA
DC output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

Note

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

DC CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2,5	–	6	V
LCD supply voltage	V_{LCD}	V_{DD} −6	–	V_{DD} −2,5	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 1)	I_{DD}	–	30	90	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz; A0, A1 and A2 tied to V_{SS} (note 1)	I_{LP}	–	15	40	μA

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	$0,3\ V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7\ V_{DD}$	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD} –0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	–1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0, CLK, OSC, A0, A1, A2, SCL, SDA) at $V_I = V_{SS}$ or V_{DD}	$\pm I_L$	–	–	1	μA
Pull-down current (A0; A1; A2; OSC) at V_I = 1 V and V_{DD} = 5 V	I_{pd}	15	50	150	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	15	25	60	kΩ
Power-on reset level (note 2)	V_{REF}	–	1,3	2,0	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 3)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S23) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_{BP}	–	1	5	kΩ
Output impedance (S0 to S23) at $V_{LCD} = V_{DD}$ –5 V (note 4)	R_S	–	3	7,0	kΩ

AC CHARACTERISTICS (note 5)

V_{SS} = 0 V; V_{DD} = 2,5 to 6 V; V_{LCD} = V_{DD} −2,5 to V_{DD} −6 V;
T_{amb} = −40 to +85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V (note 6)	f_{CLK}	125	200	315	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at V_{LCD} = V_{DD} −5 V	t_{PLCD}	–	–	30	μs
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
2. Resets all logic when $V_{DD} < V_{REF}$.
3. Periodically sampled, not 100% tested.
4. Outputs measured one at a time.
5. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
6. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

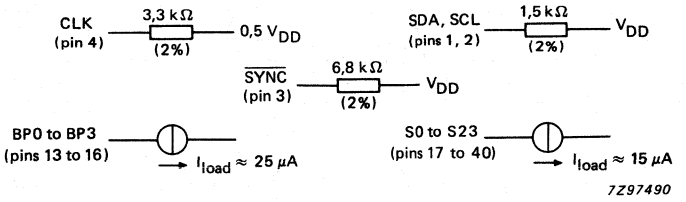


Fig. 19 Test loads.

DEVELOPMENT DATA

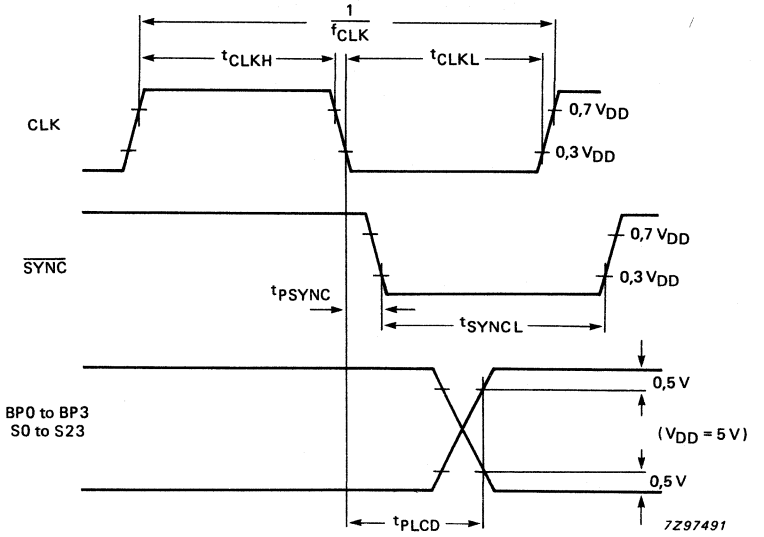


Fig. 20 Driver timing waveforms.

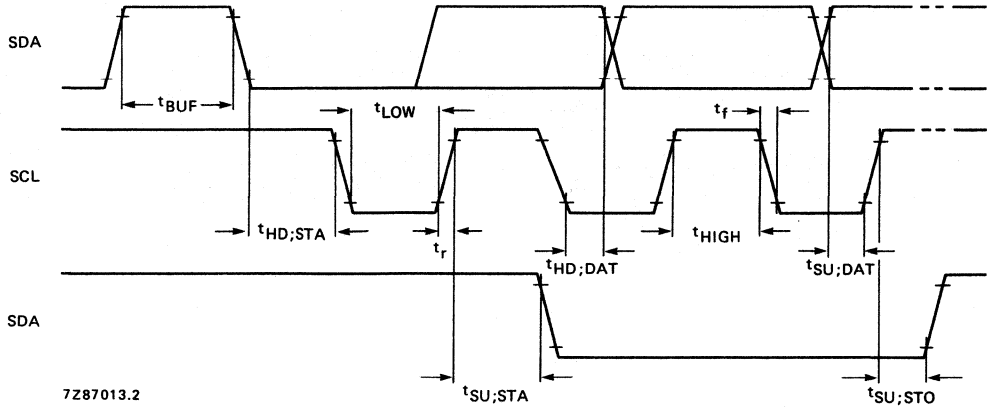
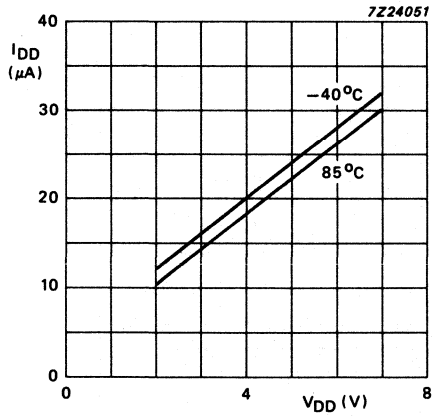
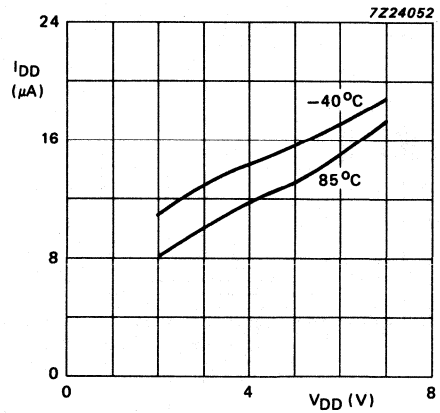


Fig. 21 I^2C bus timing waveforms.



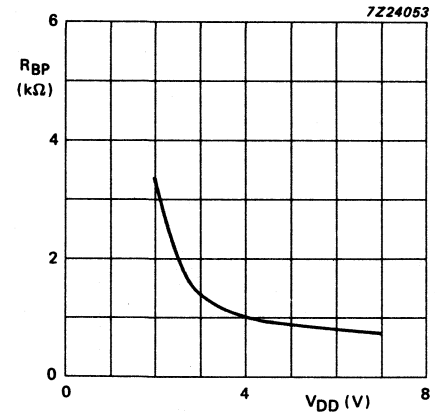
(a) Normal mode; V_{LCD} = 0 V; external clock = 200 kHz.



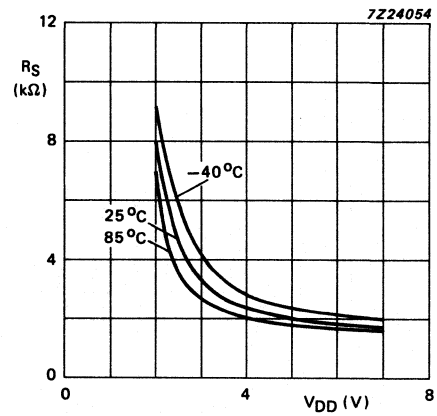
(b) Low power mode; V_{LCD} = 0 V; external clock = 35 kHz.

Fig. 22 Typical supply current characteristics.

DEVELOPMENT DATA



(a) Backplane output impedance BP0 to BP3 (R_{BP}); V_{DD} = 5 V; T_{amb} = −40 to + 85 °C.



(b) Segment output impedance S0 to S23 (R_S); V_{DD} = 5 V.

Fig. 23 Typical characteristics of LCD outputs.

APPLICATION INFORMATION

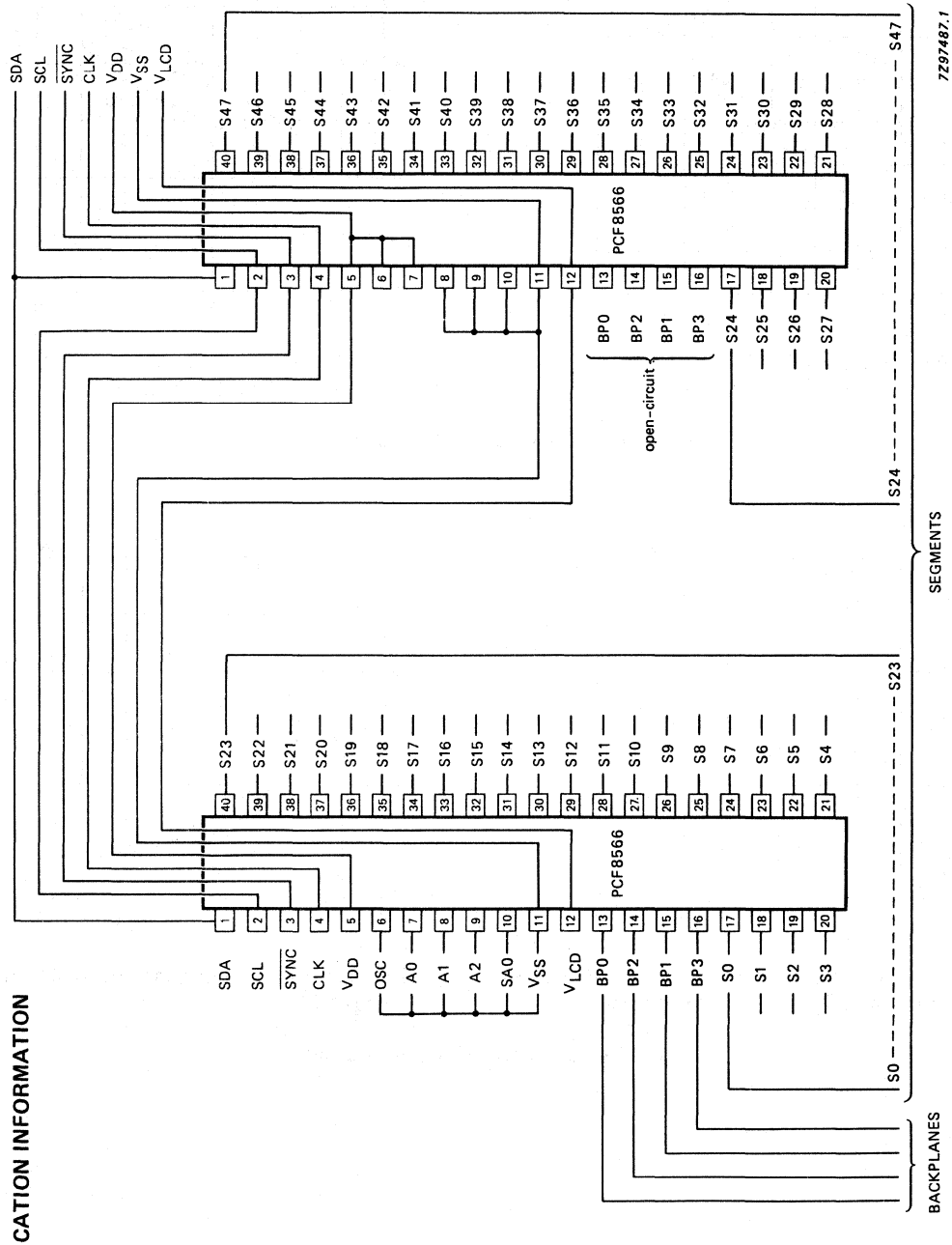


Fig. 24 Single plane wiring of packaged PCF8566s.

128 x 8 BIT/256 x 8 BIT STATIC RAMs WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8570, PCF8570C and PCF8571 are low-power static CMOS RAMs. The PCF8570 and PCF8570C are organized as 256 words by 8-bits and the PCF8571 is organized as 128 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I²C). The built-in word address register is incremented automatically after each written or read data byte. Three address pins A0, A1 and A2 are used for hardware address, allowing the use of up to eight devices connected to the bus without additional hardware. For system expansion over 8 devices the PCF8570/71 can be used in conjunction with the PCF8750C which has an alternative slave address for memory extension up to 16 devices.

Features

- Operating supply voltage 2,5 V to 6 V
- Low data retention voltage min. 1,0 V
- Low standby current max. 15 μA
- Power saving mode typ. 50 nA
- Serial input/output bus (I²C)
- Address by 3 hardware address pins
- Automatic word address incrementing
- 8-lead DIL package

Applications

- Telephony — RAM expansion for stored numbers in repertory dialling (e.g. PCD3343 applications)
- Radio and television — channel presets
- Video cassette recorder — channel presets
- General purpose — RAM expansion for the microcontroller families MAB8400, PCF84CXX and most other microcontrollers

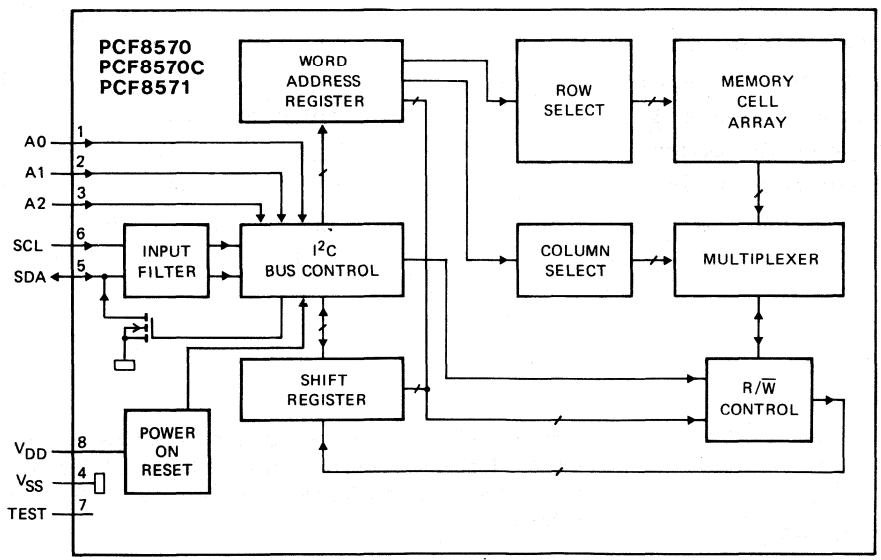


Fig. 1 Block diagram. 7Z90775.3

PACKAGE OUTLINES

PCF8570/PCF8570C/PCF8571/P: 8-lead DIL; plastic (SOT97).
PCF8570/PCF8570C/PCF8571/T: 8-lead mini-pack (SO8L; SOT176).

PINNING

1 to 3	A0 to A2	address inputs
4	V_{SS}	negative supply
5	SDA	serial data line } I^2C bus
6	SCL	serial clock line } I^2C bus
7	TEST	test input for test speed-up; must be connected to V_{SS} when not in use (power saving mode, see Figs 12 and 13)
8	V_{DD}	positive supply

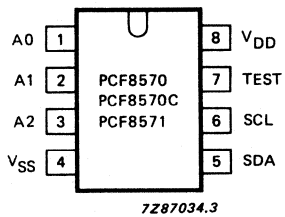


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8)	V_{DD}		−0,8 to + 8,0 V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8 V
DC input current (any input)	$\pm I_I$	max.	10 mA
DC output current (any output)	$\pm I_O$	max.	10 mA
Supply current (pin 8 or pin 4)	$\pm I_{DD}$; I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	50 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current at $V_I = V_{SS}$ or V_{DD};					
operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
standby at f_{SCL} = 0 Hz	I_{DDO}	–	–	15	μA
standby at T_{amb} = −25 to + 70 °C	I_{DDO}	–	–	5	μA
Power-on reset voltage level*	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW**	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH**	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\pm I_I$	–	–	250	nA
Clock frequency (Fig. 7)	f_{SCL}	0	–	100	kHz
Input capacitance (SCL, SDA) at $V_I = V_{SS}$	C_I	–	–	7	pF
Tolerable spike width on bus	t_{SW}	–	–	100	ns
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C	I_{DDR}	–	–	2	μA
Power saving mode (Fig. 12 and 13)					
Supply current at T_{amb} = 25 °C; TEST = V_{DD};					
PCF8570/8570C	I_{DDR}	–	50	400	nA
PCF8571	I_{DDR}	–	50	200	nA
Recovery time	t_{HD2}	–	50	–	μs

* The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$. The status of the device after a power-on reset condition can be tested by sending the slave address and testing the acknowledge bit.

** If the input voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow: this current must not exceed ± 0,5 mA.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

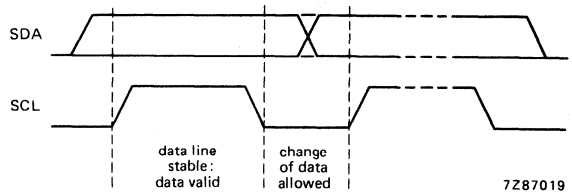


Fig. 3 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

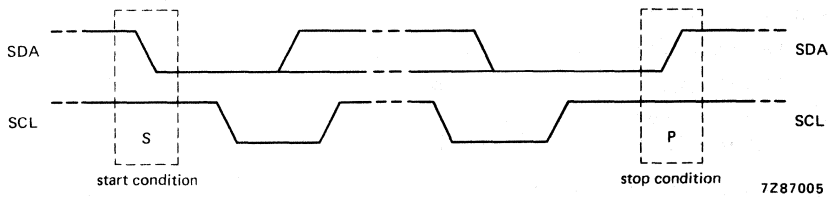


Fig. 4 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

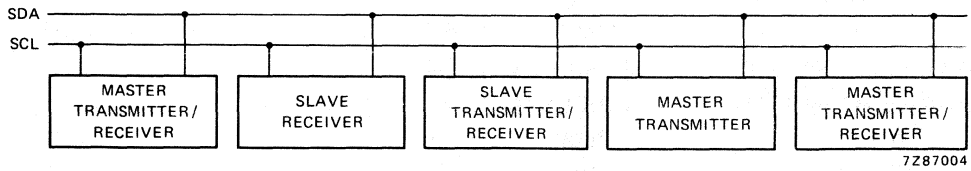


Fig. 5 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

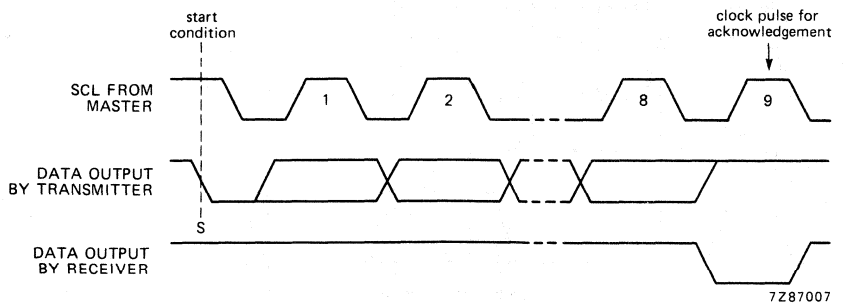


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

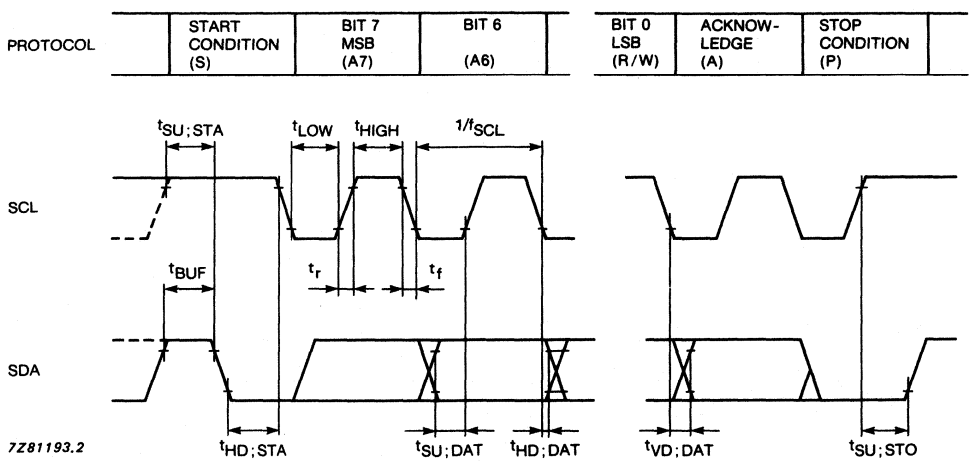


Fig. 7 I^2C bus timing diagram.

Bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for different PCF8570/PCF8570C/PCF8571 READ and WRITE cycles is shown in Fig. 8.

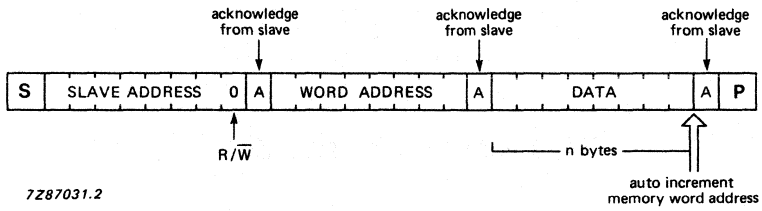


Fig. 8(a) Master transmits to slave receiver (WRITE mode).

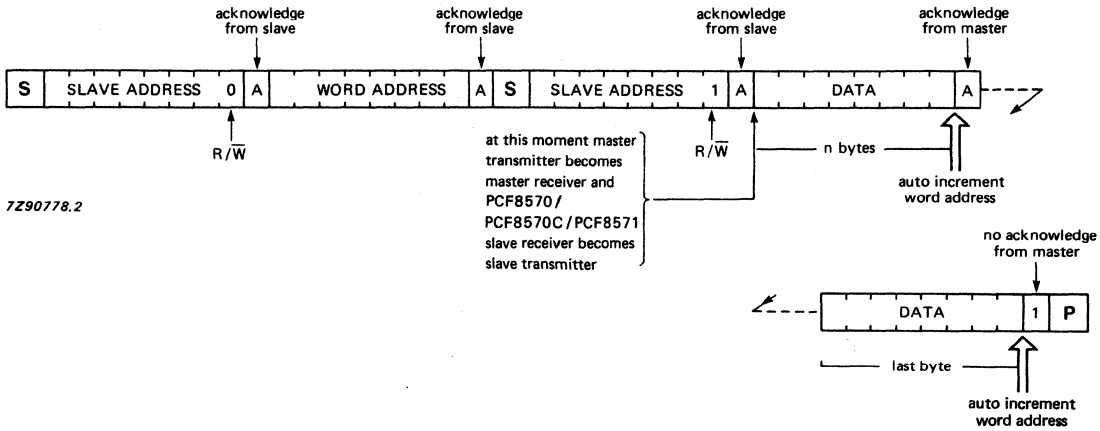


Fig. 8(b) Master reads after setting word address (WRITE word address; READ data).

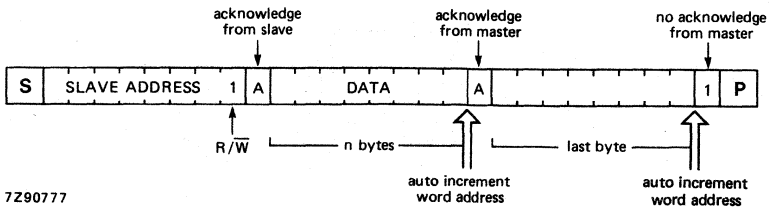


Fig. 8(c) Master reads slave immediately after first byte (READ mode).

APPLICATION INFORMATION

The PCF8570/PCF8571 slave address has a fixed combination 1010 as group 1, while group 2 is fully programmable (see Fig. 9). The PCF8570C has slave address 1011 as group 1, while group 2 is fully programmable (see Fig. 10).

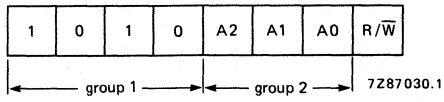


Fig. 9 PCF8570 and PCF8571 address.

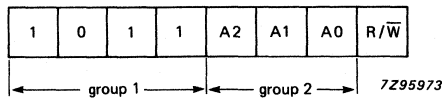


Fig. 10 PCF8570C address.

Note

A0, A1, and A2 inputs must be connected to V_{DD} or V_{SS} but not left open-circuit.

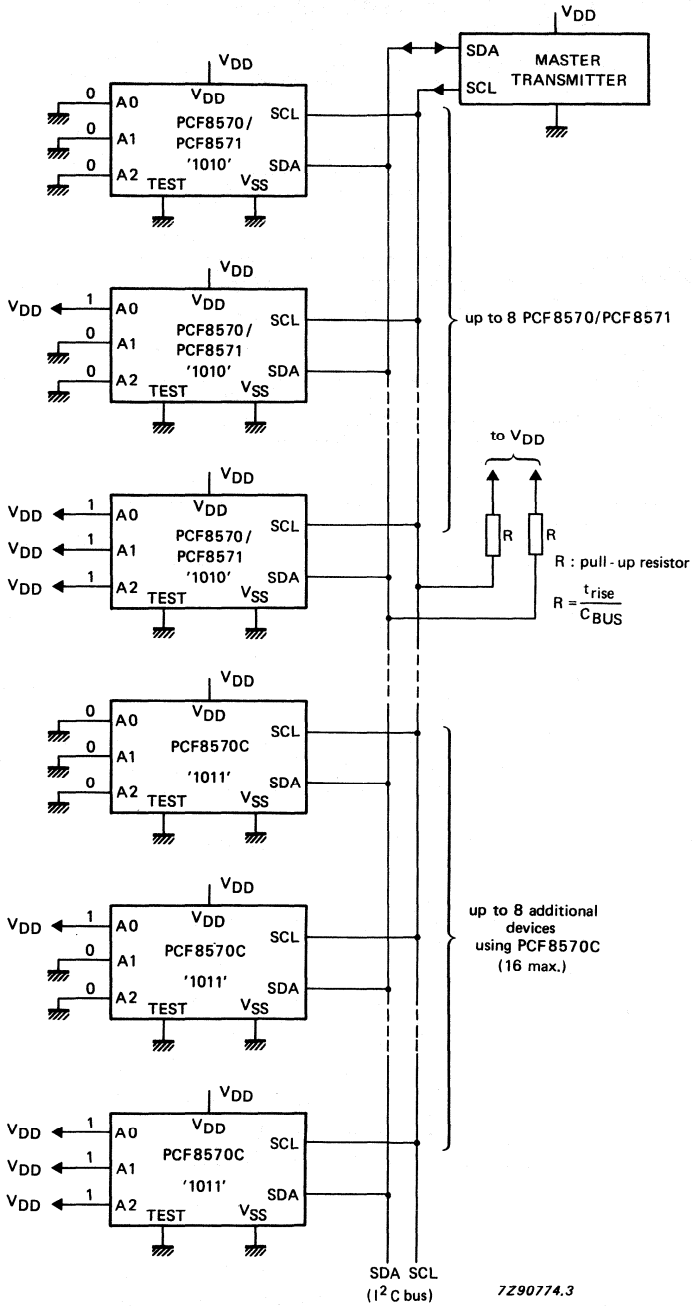
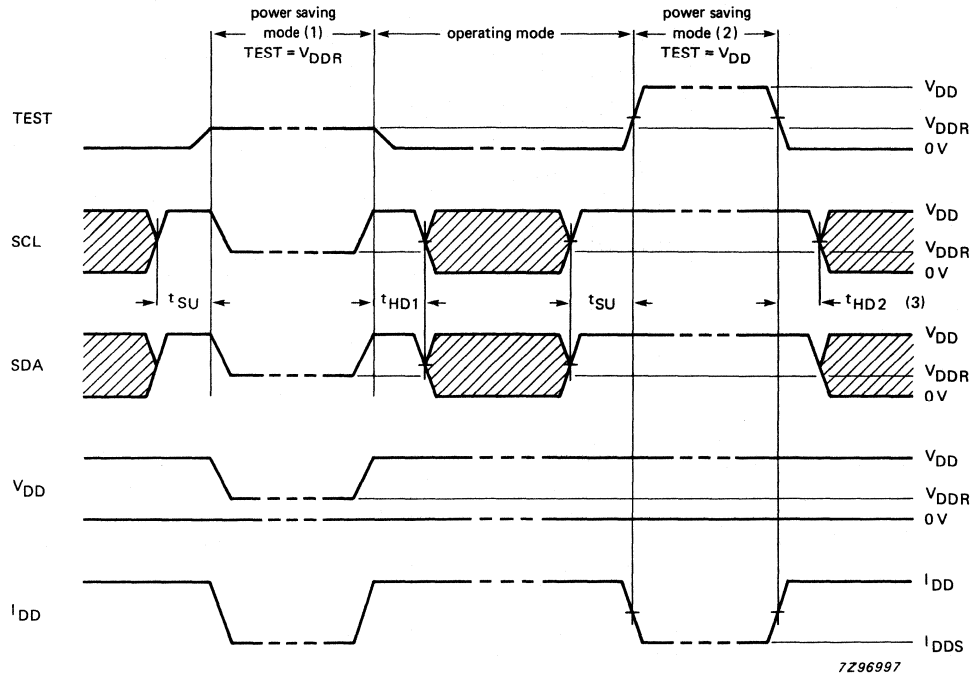


Fig. 11 Application diagram.

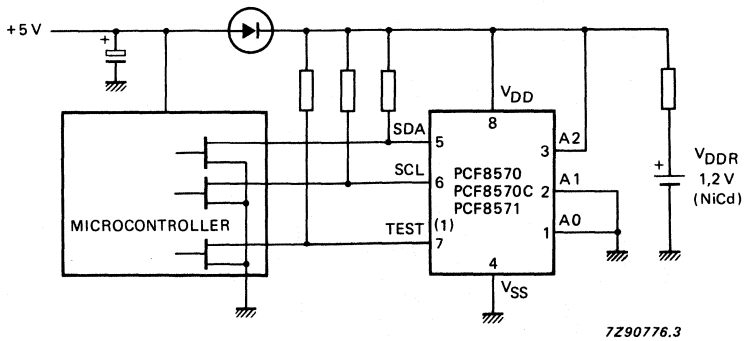
POWER SAVING MODE

With the condition **TEST** = V_{DD} or V_{DDR} the PCF8570/PCF8570C/PCF8571 goes into the power saving mode and I^2C bus logic is reset.



(1) Power saving mode without 5 V supply voltage.
(2) Power saving mode with 5 V supply voltage.
(3) t_{SU} and $t_{HD1} \geqslant 4\ \mu s$ and $t_{HD2} \geqslant 50\ \mu s$.

Fig. 12 Timing for power saving mode.



(1) In the operating mode TEST = 0; In the power saving mode TEST = V_{DDR}.

Fig. 13 Application example for power saving mode.

CLOCK/CALENDAR WITH SERIAL I/O

GENERAL DESCRIPTION

The PCF8573 is a low threshold, monolithic CMOS peripheral circuit that functions as a real time clock/calendar with an Inter IC (I^2C) bus interface.
The device incorporates an addressable time counter and an addressable alarm register for minutes, hours, days and months. Three special control/status flags, COMP, POWF and NODA are also available. Information is transferred via a serial, two-line bidirectional bus (I^2C). Back-up for the clock during supply interruption is provided by a 1.2 V nickel cadmium battery. The time base is generated from a 32,768 kHz crystal controlled oscillator.

Features

- Serial input/output bus (I^2C) interface for minutes, hours, days and months
- Additional pulse outputs for seconds and minutes
- Alarm register for presetting a time for alarm or remote switching functions
- Battery back-up for clock function during supply interruption
- Crystal oscillator control (32,768 kHz)

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	–	6,0	V
Supply voltage (I^2C interface)		$V_{DD}-V_{SS2}$	2,5	–	6,0	V
Crystal oscillator		f_{osc}	–	32,768	–	kHz

PACKAGE OUTLINES

PCF8573P: 16-lead DIL; plastic (SOT38).
PCF8573T: 16-lead mini-pack; plastic (SO16L; SOT162A).

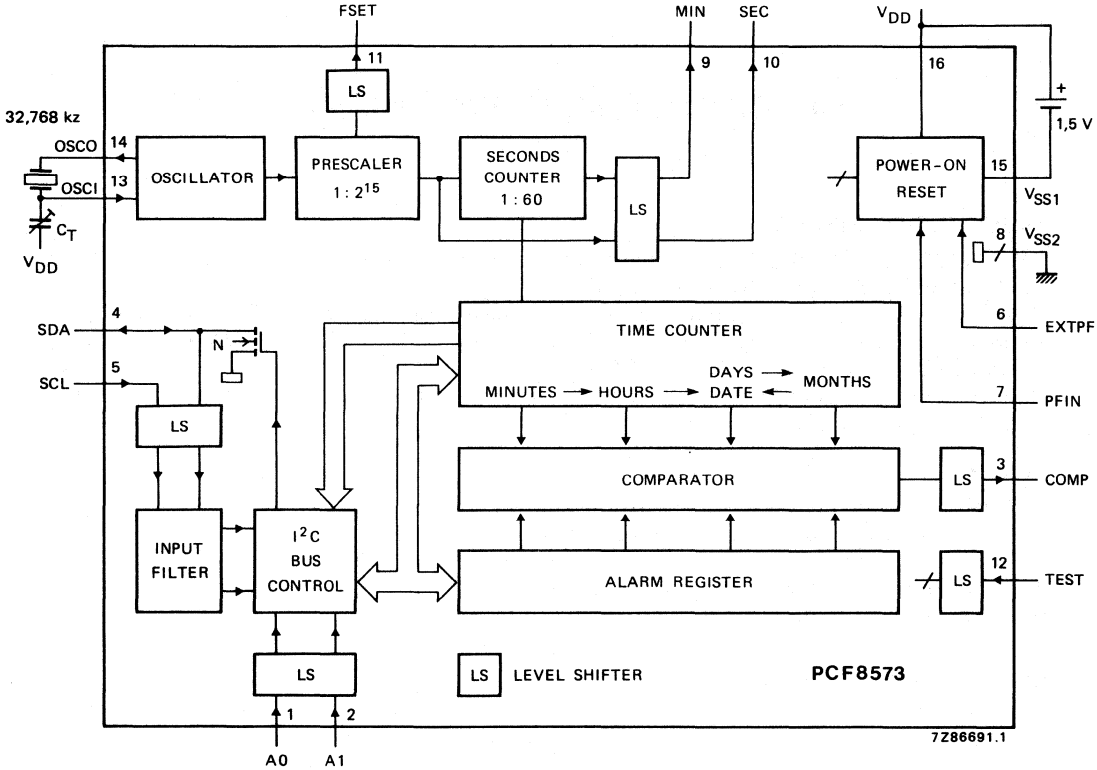


Fig. 1 Block diagram.

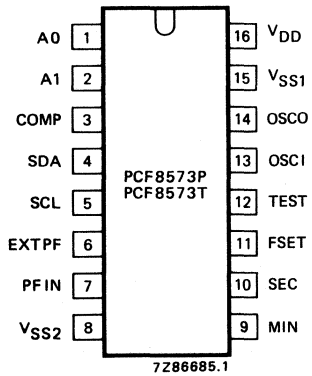


Fig. 2 Pinning diagram.

PINNING

1	A0	address input	
2	A1	address input	
3	COMP	comparator output	
4	SDA	serial data line	I^2C bus
5	SCL	serial clock line	I^2C bus
6	EXTPF	enable power fail flag input	
7	PFIN	power fail flag input	
8	V_{SS2}	negative supply 2 (I^2C interface)	
9	MIN	one pulse per minute output	
10	SEC	one pulse per second output	
11	FSET	oscillator tuning output	
12	TEST	test input; must be connected to V_{SS2} when not in use	
13	OSCI	oscillator input	
14	OSCO	oscillator input/output	
15	V_{SS1}	negative supply 1 (clock)	
16	V_{DD}	common positive supply	

FUNCTIONAL DESCRIPTION

Oscillator

The PCF8573 has an integrated crystal-controlled oscillator which provides the timebase for the prescaler. The frequency is determined by a single 32,768 kHz crystal connected between OSCI and OSCO. A trimmer is connected between OSCI and V_{DD}.

Prescaler and time counter

The prescaler provides a 128 Hz signal at the FSET output for fine adjustment of the crystal oscillator without loading it. The prescaler also generates a pulse once a second to advance the seconds counter. The carry of the prescaler and the seconds counter are available at the outputs SEC, MIN respectively, and are also readable via the I^2C bus. The mark-to-space ratio of both signals is 1 : 1. The time counter is advanced one count by the falling edge of output signal MIN. A transition from HIGH to LOW of output signal SEC triggers MIN to change state. The time counter counts minutes, hours, days and months, and provides a full calendar function which needs to be corrected once every four years. Cycle lengths are shown in Table 1.

Table 1 Cycle length of the time counter

unit	number of bits	counting cycle	carry for following unit	content of month counter
minutes	7	00 to 59	59 → 00	
hours	6	00 to 23	23 → 00	
days	6	01 to 28	28 → 01	2 (note 1)
			or 29 → 01	2 (note 1)
		01 to 30	30 → 01	4, 6, 9, 11
		01 to 31	31 → 01	1, 3, 5, 7, 8, 10, 12
months	5	01 to 12	12 → 01	

Note to Table 1

1. Day counter may be set to 29 by a write transmission with EXECUTE ADDRESS.

Alarm register

The alarm register is a 24-bit memory. It stores the time-point for the next setting of the status flag COMP. Details of writing and reading of the alarm register are included in the description of the characteristics of the I^2C bus.

Comparator

The comparator compares the contents of the alarm register and the time counter, each with a length of 24 bits. When these contents are equal the flag COMP will be set 4 ms after the falling edge of MIN. This set condition occurs once at the beginning of each minute. This information is latched, but can be cleared by an instruction via the I^2C bus. A clear instruction may be transmitted immediately after the flag is set and will be executed. Flag COMP information is also available at the output COMP. The comparison may be based upon hours and minutes only if the internal flag NODA (no date) is set. Flag NODA can be set and cleared by separate instructions via the I^2C bus, but it is undefined until the first set or clear instruction has been received. Both COMP and NODA flags are readable via the I^2C bus.

FUNCTIONAL DESCRIPTION (continued)

Power on/power fail detection

If the voltage $V_{DD}-V_{SS1}$ falls below a certain value the operation of the clock becomes undefined. Thus a warning signal is required to indicate that faultless operation of the clock is not guaranteed. This information is latched in a flag called POWF (Power Fail) and remains latched after restoration of the correct supply voltage until a write procedure with EXECUTE ADDRESS has been received. The flag POWF can be set by an internally generated power fail level-discriminator signal for application with ($V_{DD}-V_{SS1}$) greater than V_{TH1}, or by an externally generated power fail signal for application with ($V_{DD}-V_{SS1}$) less than V_{TH1}. The external signal must be applied to the input PFIN. The input stage operates with signals of any slow rise and fall times. Internally or externally controlled POWF can be selected by input EXTPF as shown in Table 2.

Table 2 Power fail selection

EXTPF	PFIN	function
0	0	power fail is sensed internally
0	1	test mode
1	0	power fail is sensed externally
1	1	no power fail sensed

0 : connected to V_{SS1} (LOW)
1 : connected to V_{DD} (HIGH)

The external power fail control operates by absence of the $V_{DD}-V_{SS2}$ supply. Therefore the input levels applied to PFIN and EXTPF must be within the range of $V_{DD}-V_{SS1}$. A LOW level at PFIN indicates a power fail. POWF is readable via the I^2C bus. A power on reset for the I^2C bus control is generated on-chip when the supply voltage $V_{DD}-V_{SS2}$ is less than V_{TH2}.

Interface level shifters

The level shifters adjust the 5 V operating voltage ($V_{DD}-V_{SS2}$) of the microcontroller to the internal supply voltage ($V_{DD}-V_{SS1}$) of the clock/calendar. The oscillator and counter are not influenced by the $V_{DD}-V_{SS2}$ supply voltage. If the voltage $V_{DD}-V_{SS2}$ is absent ($V_{SS2} = V_{DD}$) the output signal of the level shifter is HIGH because V_{DD} is the common node of the $V_{DD}-V_{SS2}$ and the $V_{DD}-V_{SS1}$ supplies. Because the level shifters invert the input signal, the internal circuit behaves as if a LOW signal is present on the inputs. FSET, SEC, MIN and COMP are CMOS push-pull output stages. The driving capability of these outputs is lost when the supply voltage $V_{DD}-V_{SS2} = 0$.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer (see Fig. 3)

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

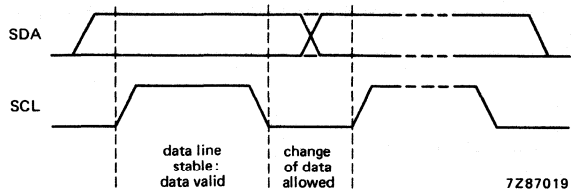


Fig. 3 Bit transfer.

Start and stop conditions (see Fig. 4)

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

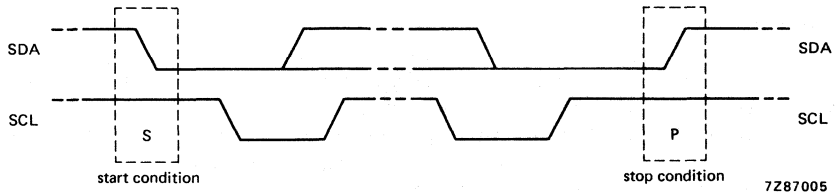


Fig. 4 Definition of start and stop conditions.

System configuration (see Fig. 5)

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

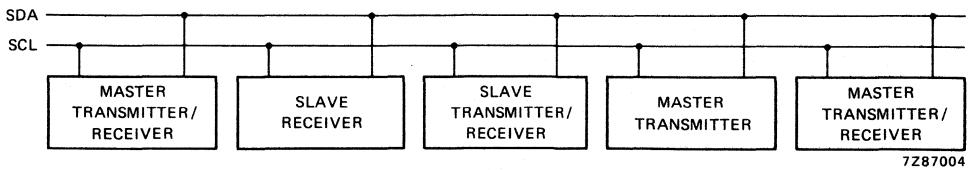


Fig. 5 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge (see Fig. 6)

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition. (See Fig. 11 and Fig. 12.)

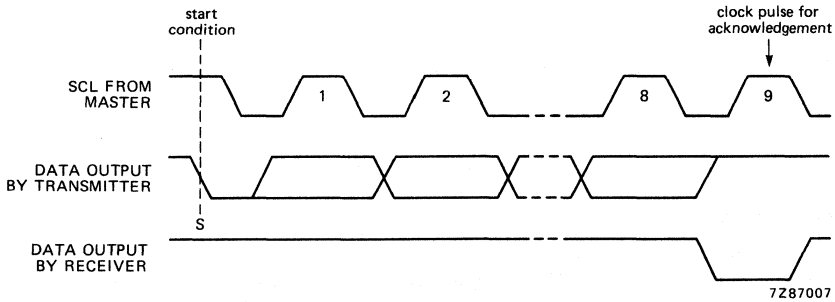


Fig. 6 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 7.

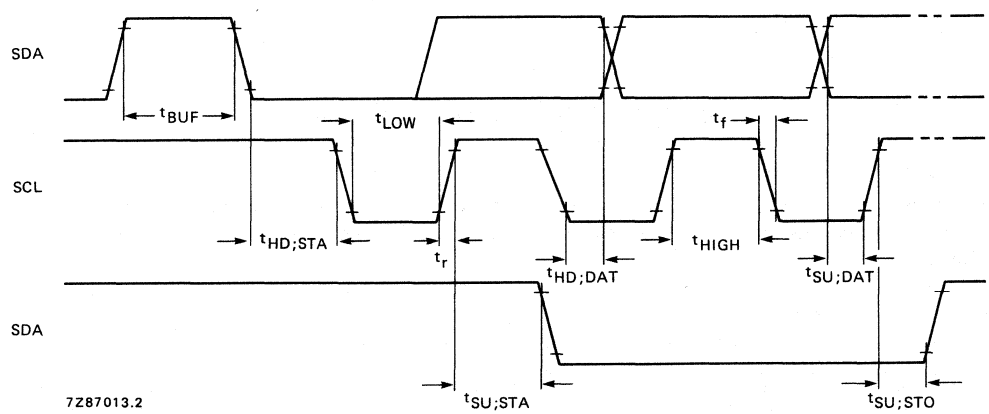


Fig. 7 Timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS2}.

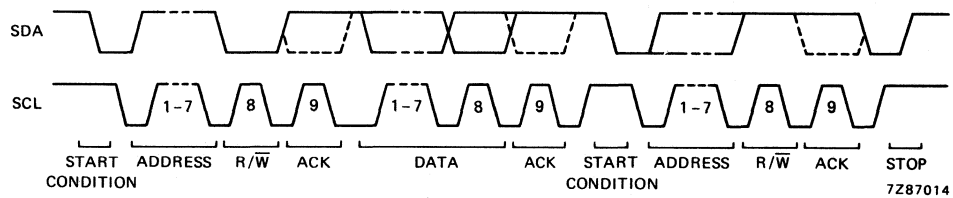


Fig. 8 Complete data transfer.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The clock/calendar acts as a slave receiver or slave transmitter. Therefore the clock signal SCL is only an input signal, but the data signal SDA is a bidirectional line. The clock calendar slave address is shown in Fig. 9.

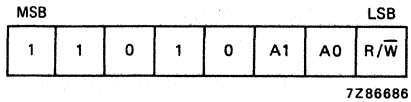


Fig. 9 Slave address.

The subaddress bits A0 and A1 correspond to the two hardware address pins A0 and A1 which allows the device to have 1 of 4 different addresses.

Clock/calendar READ/WRITE cycles

The I²C bus configuration for different clock/calendar READ and WRITE cycles is shown in Fig. 10 and Fig. 11.

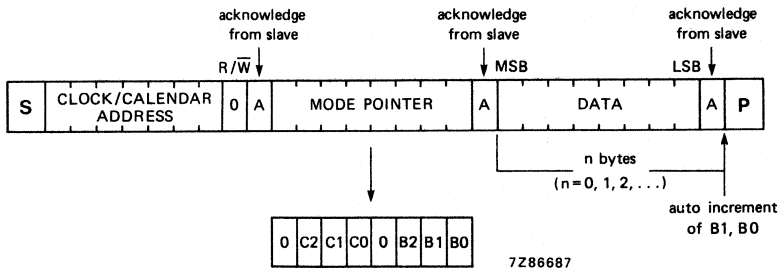


Fig. 10 Master transmitter transmits to clock/calendar slave receiver.

The write cycle is used to set the time counter, the alarm register and the flags. The transmission of the clock/calendar address is followed by the MODE-POINTER-WORD which contains a CONTROL-nibble (Table 3) and an ADDRESS-nibble (Table 4). The ADDRESS-nible is valid only if the preceding CONTROL-nibble is set to EXECUTE ADDRESS. The third transmitted word contains the data to be written into the time counter or alarm register.

Table 3 CONTROL-nibble

	C2	C1	C0	function
0	0	0	0	execute address
0	0	0	1	read control/status flags
0	0	1	0	reset prescaler, including seconds counter; without carry for minute counter
0	0	1	1	time adjust, with carry for minute counter (see note)
0	1	0	0	reset NODA flag
0	1	0	1	set NODA flag
0	1	1	0	reset COMP flag

Note

If the seconds counter is below 30 there is no carry. This causes a time adjustment of max. −30 s. From the count 30 there is a carry which adjusts the time by max. + 30 s.

Table 4 ADDRESS-nibble

	B2	B1	B0	addressed to:
0	0	0	0	time counter hours
0	0	0	1	time counter minutes
0	0	1	0	time counter days
0	0	1	1	time counter months
0	1	0	0	alarm register hours
0	1	0	1	alarm register minutes
0	1	1	0	alarm register days
0	1	1	1	alarm register months

At the end of each data word the address bits B1, B0 will be incremented automatically provided the preceding CONTROL-nibble is set to EXECUTE ADDRESS. There is no carry to B2.

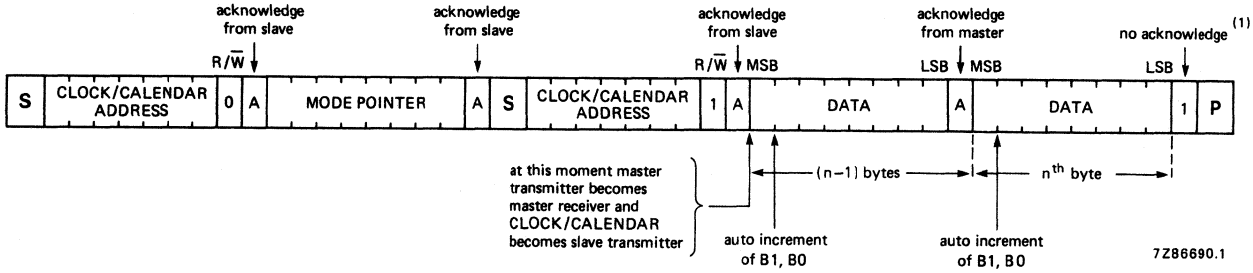
Table 5 shows the placement of the BCD upper and lower digits in the DATA byte for writing into the addressed part of the time counter and alarm register respectively.

Table 5 Placement of BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to:
X	X	D	D	D	D	D	D	hours
X	D	D	D	D	D	D	D	minutes
X	X	D	D	D	D	D	D	days
X	X	X	D	D	D	D	D	months

Where:

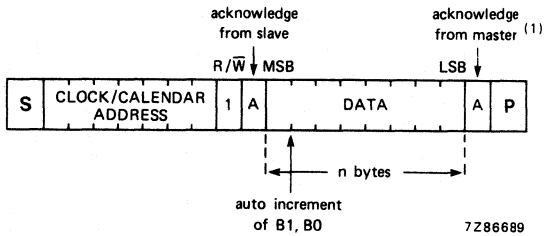
"X" is the don't care bit
"D" is the data bit
Acknowledgement response of the clock calendar as slave receiver is shown in Table 6.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 11 Master transmitter reads clock/calendar after setting mode pointer.

To read the addressed part of the time counter and alarm register, plus information from specified control/status flags, the BCD digits in the DATA byte are organized as shown in Table 7.



(1) The master receiver must signal an end of data to the slave transmitter by *not* generating an acknowledge on the *last byte* that has been clocked out of the slave.

Fig. 12 Master reads clock/calendar immediately after first byte.

The status of the MODE-POINTER-WORD concerning the CONTROL-nibble remains unchanged until a write to MODE POINTER condition occurs.

ADDRESSING (continued)

Table 6 Slave receiver acknowledgement

mode pointer								acknowledge on byte		
								address	mode pointer	data
	C2	C1	C0		B2	B1	B0			
0	0	0	0	0	X	X	X	yes	yes	yes
0	0	0	0	1	X	X	X	yes	no	no
0	0	0	1	X	X	X	X	yes	yes	no
0	0	1	0	X	X	X	X	yes	yes	no
0	0	1	1	X	X	X	X	yes	yes	no
0	1	0	0	X	X	X	X	yes	yes	no
0	1	0	1	X	X	X	X	yes	yes	no
0	1	1	0	X	X	X	X	yes	yes	no
0	1	1	1	X	X	X	X	yes	no	no
1	X	X	X	X	X	X	X	yes	no	no

Where:

"X" is the don't care bit.

Table 7 Organization of the BCD digits in the DATA byte

MSB DATA LSB								
upper digit				lower digit				
UD	UC	UB	UA	LD	LC	LB	LA	addressed to
0	0	D	D	D	D	D	D	hours
0	D	D	D	D	D	D	D	minutes
0	0	D	D	D	D	D	D	days
0	0	0	D	D	D	D	D	months
0	0	0	*	**	NODA	COMP	POWF	control/status flags

Where:

"D" is the data bit.
* = minutes.
** = seconds.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	condition	symbol	min.	max.	unit
Supply voltage ranges		$V_{DD}-V_{SS1}$	−0,3	8	V
		$V_{DD}-V_{SS2}$	−0,3	8	V
Voltage input (pins 4; 5)		V_I	$V_{SS2}-0,8$	$V_{DD}+0,8$	V*
Voltage input (pins 6; 7; 13, 14)		V_I	$V_{SS1}-0,6$	$V_{DD}+0,6$	V
Voltage on any other pin		V_I	$V_{SS2}-0,6$	$V_{DD}+0,6$	V
Input current		I_I	–	10	mA
Output current		I_O	–	10	mA
Power dissipation per output		P_O	–	100	mW
Total power dissipation		P_{tot}	–	200	mW
Operating ambient temperature range		T_{amb}	−40	+85	°C
Storage temperature range		T_{stg}	−55	+125	°C

HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS devices').

* Impedance min. 500 Ω.

CHARACTERISTICS

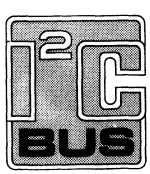
V_{SS2} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified. Typical values at T_{amb} = + 25 °C.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage I^2C interface		$V_{DD}-V_{SS2}$	2,5	5,0	6,0	V
Supply voltage (clock)		$V_{DD}-V_{SS1}$	1,1	1,5	$V_{DD}-V_{SS2}$	V
Supply current V_{SS1}	$V_{DD}-V_{SS1}$ = 1,5 V	$-I_{SS1}$	–	3	10	μA
	$V_{DD}-V_{SS1}$ = 5 V	$-I_{SS1}$	–	12	50	μA
Supply current V_{SS2}	$V_{DD}-V_{SS2}$ = 5 V; (I_O = 0 mA on all outputs)	$-I_{SS2}$	–	–	50	μA
Inputs SCL, SDA, A0, A1, TEST						
Input voltage HIGH		V_{IH}	0,7 x V_{DD}	–	–	V
Input voltage LOW		V_{IL}	–	–	0,3 x V_{DD}	V
Input leakage current	$V_I = V_{SS2}$ to V_{DD}	$\pm I_I$	–	–	1	μA
Inputs EXTPF, PFIN						
Input voltage HIGH		$V_{IH}-V_{SS1}$	0,7 x $V_{DD}-V_{SS1}$	–	–	V
Input voltage LOW		$V_{IL}-V_{SS1}$	0	–	0,3 x $V_{DD}-V_{SS1}$	V
Input leakage current	$V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	1,0	μA
	T_{amb} = 25 °C; $V_I = V_{SS1}$ to V_{DD}	$\pm I_I$	–	–	0,1	μA

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs SEC, MIN, COMP, FSET (normal buffer outputs)						
Output voltage HIGH	$V_{DD}-V_{SS2}$ = 2,5 V; $-I_O$ = 0,1 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; $-I_O$ = 0,5 mA	V_{OH}	$V_{DD}-0,4$	–	–	V
Output voltage LOW	$V_{DD}-V_{SS2}$ = 2,5 V; I_O = 0,3 mA	V_{OL}	–	–	0,4	V
	$V_{DD}-V_{SS2}$ = 4 to 6 V; I_O = 1,6 mA	V_{OL}	–	–	0,4	V
Output SDA (n channel open drain)						
Output "ON"	I_O = 3 mA; $V_{DD}-V_{SS2}$ = 2,5 to 6 V	V_{OL}	–	–	0,4	V
Output "OFF" (leakage current)	$V_{DD}-V_{SS2}$ = 6 V; V_O = 6 V	I_O	–	–	1	μA
Internal threshold voltage						
Power failure detection		V_{TH1}	1	1,2	1,4	V
Power "ON" reset	$V_{SCL} = V_{SDA} = V_{DD}$	V_{TH2}	1,5	2,0	2,5	V
Rise and fall times of input signals						
Input EXTPF		t_r, t_f	–	–	1	μs
Input PFIN		t_r, t_f	–	–	∞	μs
Input signals except EXTPF and PFIN between V_{IL} and V_{IH} levels						
rise time		t_r	–	–	1	μs
fall time		t_f	–	–	0,3	μs

parameter	conditions	symbol	min.	typ.	max.	unit
Frequency at SCL	$V_{DD}-V_{SS2}$ = 4 to 6 V					
Pulse width LOW (Fig. 7)		t_{LOW}	4,7	–	–	μs
Pulse width HIGH (Fig. 7)		t_{HIGH}	4	–	–	μs
Noise suppression time constant at SCL and SDA input		T_I	0,25	1	2,5	μs
Input capacitance (SDA; SCL)		C_I	–	–	7	pF
Oscillator						
Integrated oscillator capacitance		C_{OUT}	–	40	–	pF
Oscillator feedback resistance		R_f	–	3	–	MΩ
Oscillator stability	$\Delta(V_{DD}-V_{SS1})$ = 100 mV; at $V_{DD}-V_{SS1}$ = 1,55 V; T_{amb} = 25 °C	f/f_{osc}	–	2×10^{-6}	–	–
Quartz crystal parameters	f = 32,768 kHz					
Series resistance		R_S	–	–	40	kΩ
Parallel capacitance		C_L	–	9	–	pF
Trimmer capacitance		C_T	5	–	25	pF



Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

APPLICATION INFORMATION

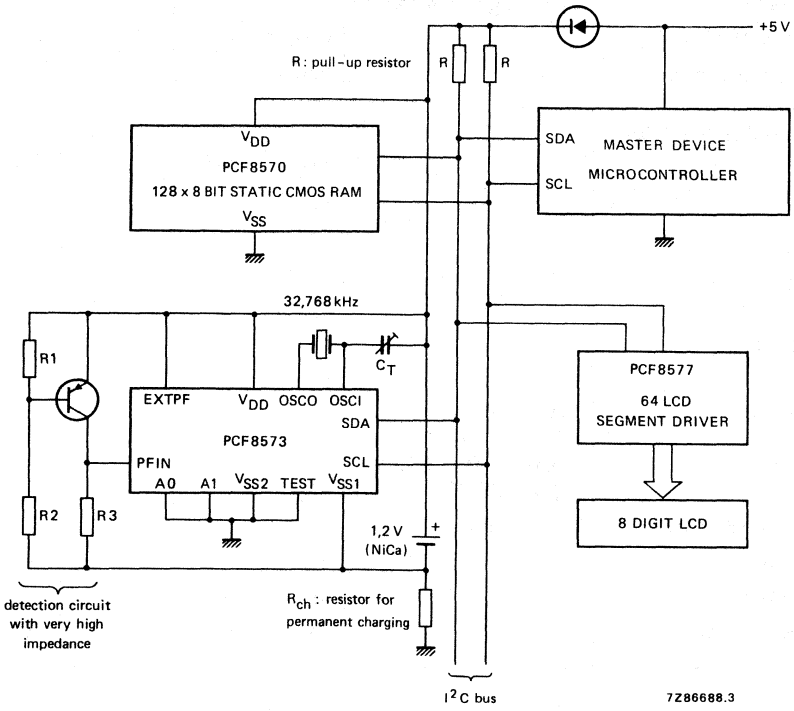


Fig. 13 Application example of the PCF8573 clock/calendar.

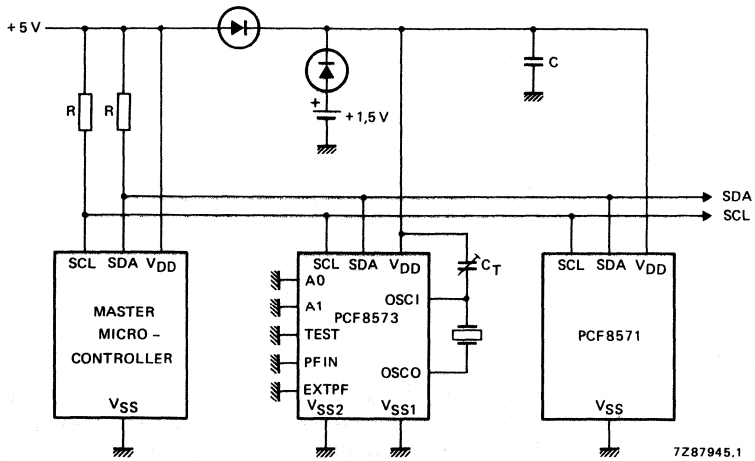


Fig. 14 Application example of the PCF8573 with common V_{SS1} and V_{SS2} supply.

REMOTE 8-BIT I/O EXPANDER FOR I²C BUS

GENERAL DESCRIPTION

The PCF8574 is a single-chip silicon gate CMOS circuit. It provides remote I/O expansion for the MAB8400 and PCF84CXX microcontroller families via the two-line serial bidirectional bus (I²C).
It can also interface microcomputers without a serial interface to the I²C bus (as a slave function only).
The device consists of an 8-bit quasi-bidirectional port and an I²C interface.
The PCF8574 has low current consumption and includes latched outputs with high current drive capability for directly driving LEDs. It also possesses an interrupt line (INT) which is connected to the interrupt logic of the microcomputer on the I²C bus. By sending an interrupt signal on this line, the remote I/O can inform the microcomputer if there is incoming data on its ports without having to communicate via the I²C bus. This means that the PCF8574 can remain a simple slave device.

The PCF8574 and the PCF8574A versions differ only in their slave address as shown in Fig. 10.

Features

- Operating supply voltage 2,5 V to 6 V
- Low stand-by current consumption max. 10 μA
- Bidirectional expander
- Open drain interrupt output
- 8-bit remote I/O port for the I²C bus
- Peripheral for the MAB8400 and PCF84CXX microcontroller families
- Latched outputs with high current drive capability for directly driving LEDs
- Address by 3 hardware address pins for use of up to 8 devices (up to 16 with PCF8574A)

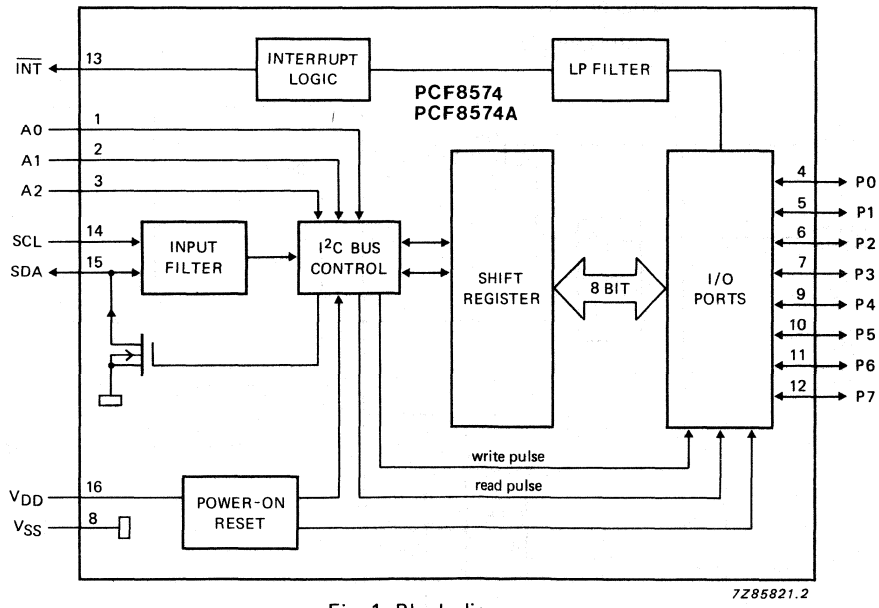


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8574P, PCF8574AP: 16-lead DIL; plastic (SOT38).
PCF8574T, PCF8574AT: 16-lead mini-pack; plastic (SO16L; SOT162A).

PINNING

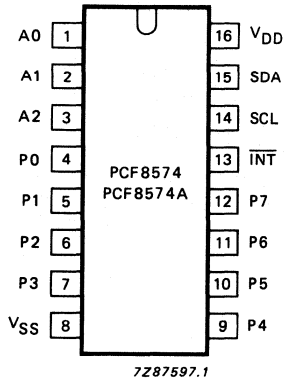


Fig. 2 Pinning diagram.

1 to 3	A0 to A2	address inputs
4 to 7 9 to 12	P0 to P3 P4 to P7	8-bit quasi-bidirectional I/O port
8	V_{SS}	negative supply
13	$\overline{INT}$	interrupt output
14	SCL	serial clock line
15	SDA	serial data line
16	V_{DD}	positive supply

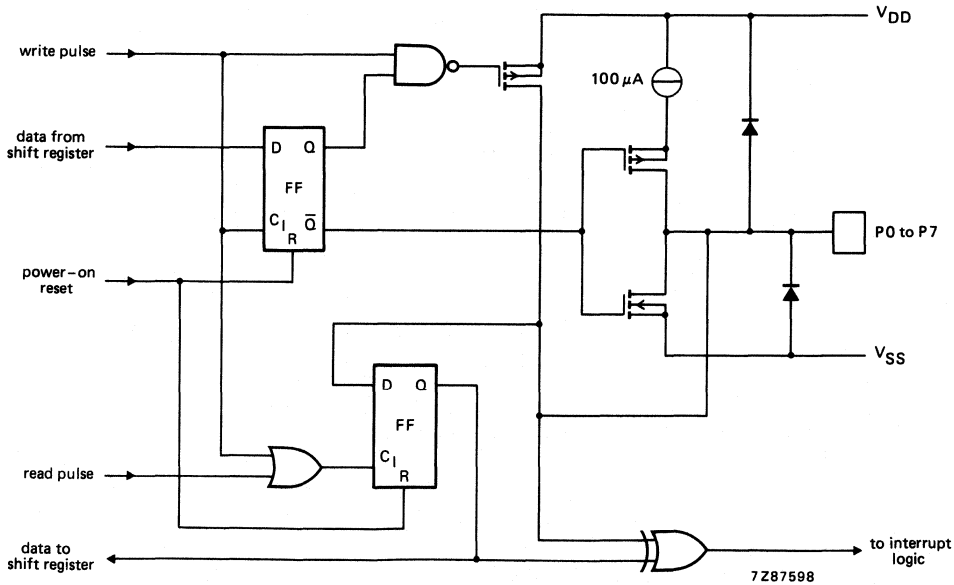


Fig. 3 Simplified schematic diagram of each port.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

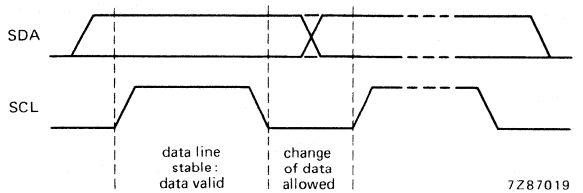


Fig. 4 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

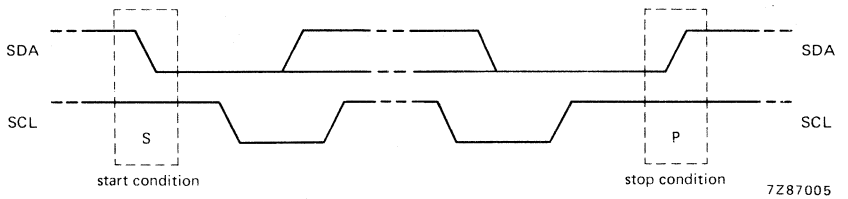


Fig. 5 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

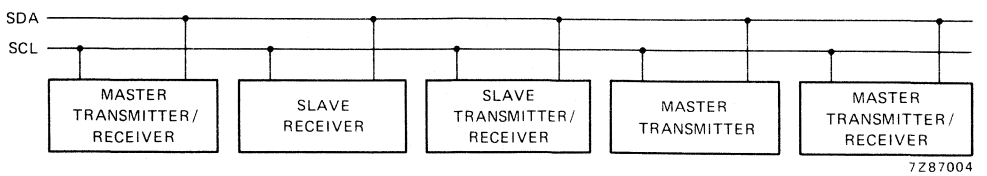


Fig. 6 System configuration.

CHARACTERISTICS OF THE I²C BUS (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

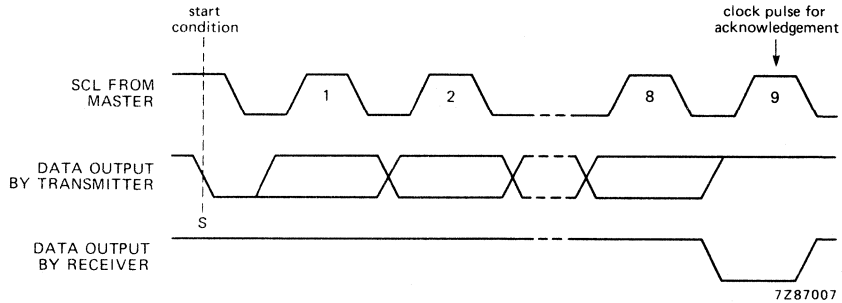


Fig. 7 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 8.

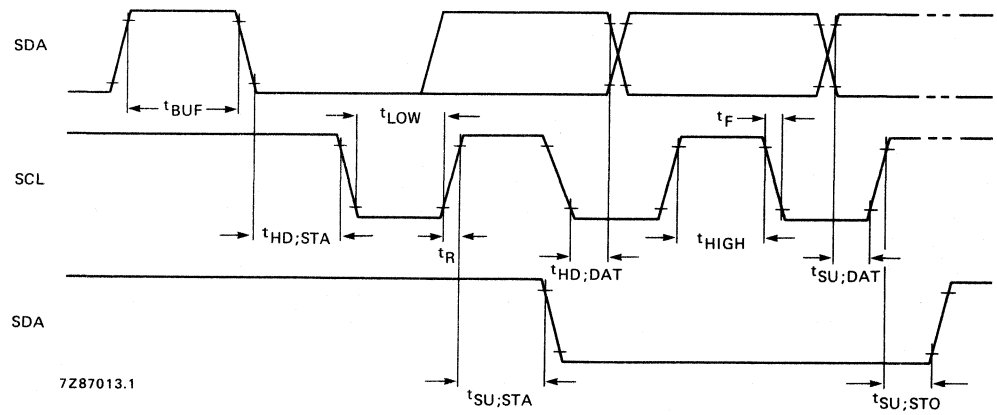


Fig. 8 I²C bus timing.

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

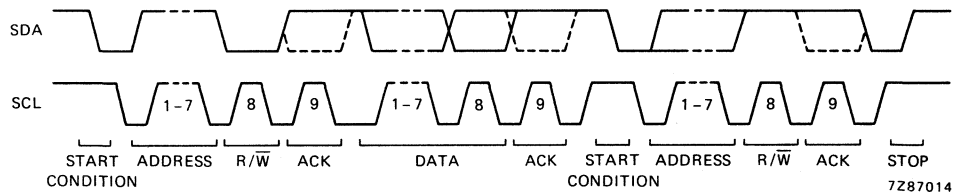


Fig. 9 Complete data transfer.

Where:

Clock t_{LOWmin} 4,7 μs

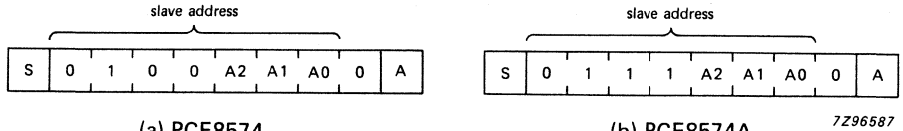
$t_{HIGHmin}$ 4 μs

The dashed line is the acknowledgement of the receiver

Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

FUNCTIONAL DESCRIPTION

Addressing (see Figs 10, 11 and 12)



(a) PCF8574. (b) PCF8574A.

Fig. 10 PCF8574 and PCF8574A slave addresses.

Each bit of the PCF8574 I/O port can be independently used as an input or an output. Input data is transferred from the port to the microcomputer by the READ mode. Output data is transmitted to the port by the WRITE mode.

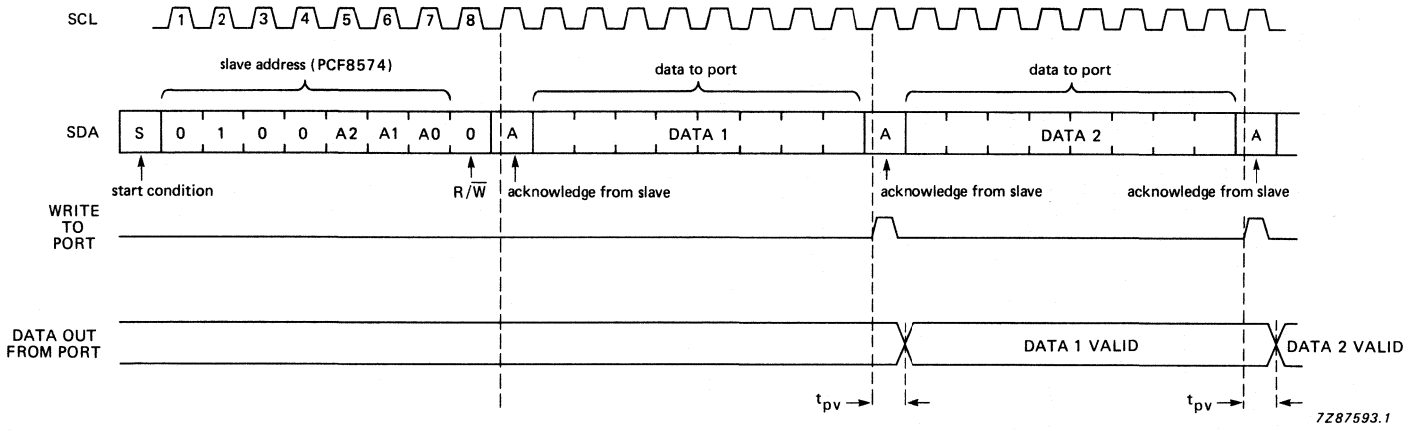


Fig. 11 WRITE mode (output port).

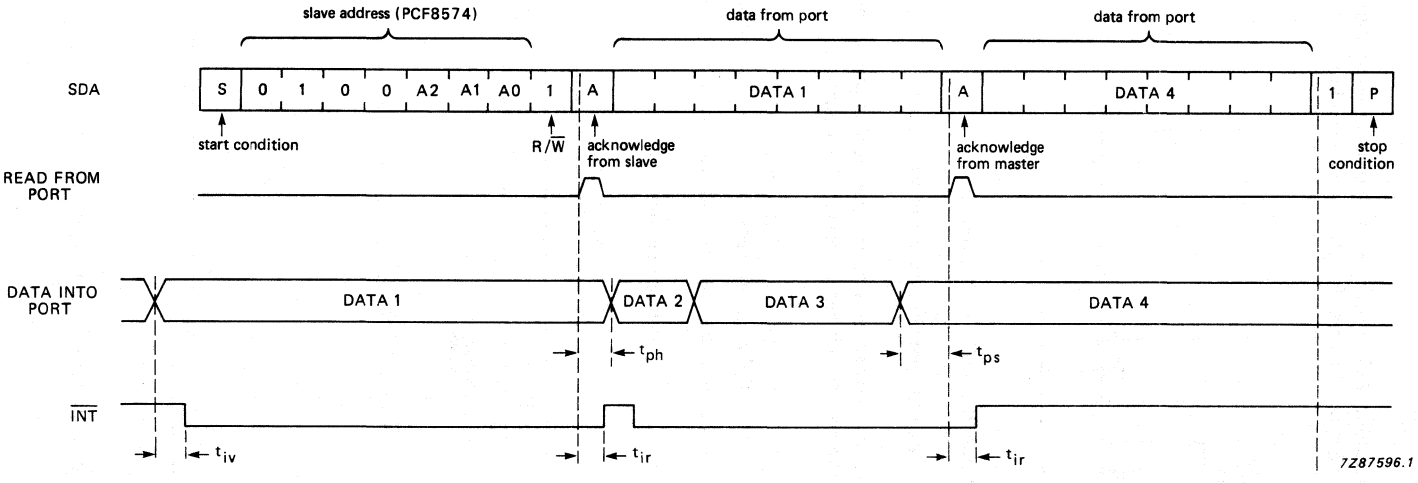


Fig. 12 READ mode (input port).

Note

A LOW-to-HIGH transition of SDA, while SCL is HIGH is defined as the stop condition (P). Transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the last acknowledge phase is valid (output mode). Input data is lost.

Interrupt (see Figs 13 and 14)

The PCF8574/PCF8574A provides an open drain output ($\overline{INT}$) which can be fed to a corresponding input of the microcomputer. This gives these chips a type of master function which can initiate an action elsewhere in the system.

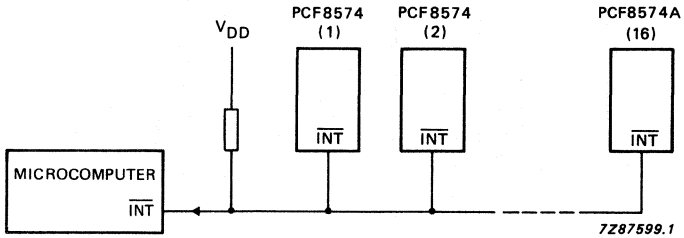


Fig. 13 Application of multiple PCF8574s with interrupt.

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time t_{iv} the signal $\overline{INT}$ is valid.
Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from or written to the port which has generated the interrupt.
Resetting occurs as follows:

- In the READ mode at the acknowledge bit after the rising edge of the SCL signal.
- In the WRITE mode at the acknowledge bit after the HIGH to LOW transition of the SCL signal.

Each change of the ports after the resettings will be detected and after the next rising clock edge, will be transmitted as $\overline{INT}$.
Reading from or writing to another device does not affect the interrupt circuit.

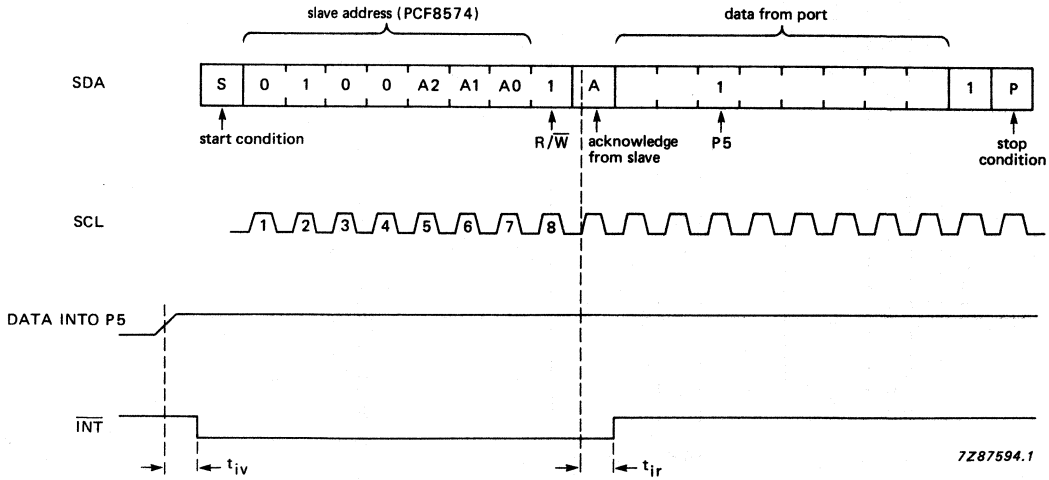


Fig. 14 Interrupt generated by a change of input to port P5.

FUNCTIONAL DESCRIPTION (continued)

Quasi-bidirectional I/O ports (see Fig. 15)

A quasi-bidirectional port can be used as an input or output without the use of a control signal for data direction. The bit designated as an input must first be loaded with a logic 1. In this mode only a current source to V_{DD} is active. An additional strong pull-up to V_{DD} allows fast rising edges into heavily loaded outputs. These devices turn on when an output changes from LOW to HIGH, and are switched off by the negative edge of SCL. SCL should not remain HIGH when a short-circuit to V_{SS} is allowed (input mode).

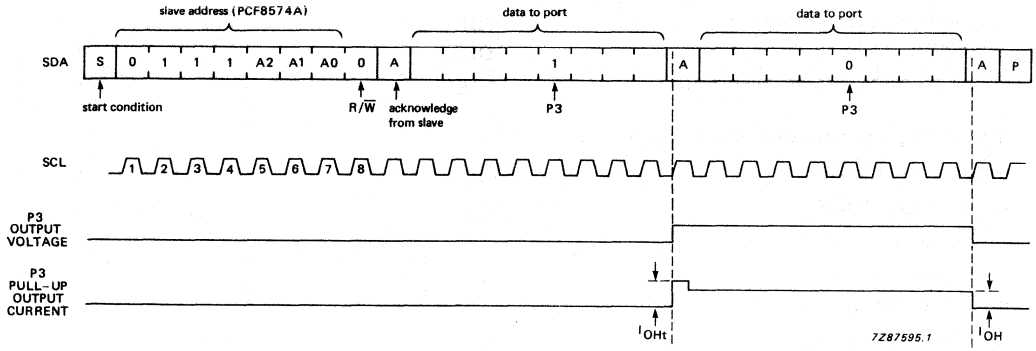


Fig. 15 Transient pull-up current I_{OHt} while P3 changes from LOW-to-HIGH and back to LOW.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 7 V
Input voltage range (any pin)	V_I		V_{SS}−0,5 to V_{DD} + 0,5 V
D.C. current into any input	$\pm I_I$	max.	20 mA
D.C. current into any output	$\pm I_O$	max.	25 mA
V_{DD} or V_{SS} current	$\pm I_{DD}$; I_{SS}	max.	100 mA
Total power dissipation	P_{tot}	max.	400 mW
Power dissipation per output	P_o	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C
Operating ambient temperature range	T_{amb}		−40 to + 85 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

CHARACTERISTICS

V_{DD} = 2,5 to 6 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 16)					
Supply voltage	V_{DD}	2,5	–	6	V
Supply current					
at V_{DD} = 6 V; no load, inputs at V_{DD}, V_{SS}					
operating; (SCL = 100 kHz)	I_{DD}	–	40	100	μA
standby	I_{DDO}	–	1,5	10	μA
Power-on reset voltage level (note 1)	V_{REF}	–	1,3	2,4	V
Input SCL; input/output SDA (pins 14; 15)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Output current LOW					
at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Input/Output leakage current	$\|I_L\|$	–	–	1	yA
Clock frequency (see Fig. 8)	f_{SCL}	–	–	100	kHz
Tolerable spike width					
at SCL and SDA input	t_s	–	–	100	ns
Input capacitance (SCL, SDA)					
at V_I = V_{SS}	C_I	–	–	7	pF
I/O ports (pins 4 to 7; 9 to 12)					
Input voltage LOW	V_{IL}	−0,5 V	–	$0,3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0,7V_{DD}$	–	V_{DD} + 0,5 V	V
Maximum allowed input current					
through protection diode					
at $V_I \geqslant V_{DD}$ or $\leqslant V_{SS}$	$\pm I_{IHL}$	–	–	400	μA
Output current LOW					
at V_{OL} = 1 V; V_{DD} = 5 V	I_{OL}	10	30	–	mA
Output current HIGH					
at V_{OH} = V_{SS} (current source only)	$-I_{OH}$	30	100	300	μA
Transient pull-up current HIGH					
during acknowledge (see Fig. 16)					
at V_{OH} = V_{SS}	$-I_{OHt}$	–	0,5	–	mA
Input/Output capacitance	$C_{I/O}$	–	–	10	pF
Port timing; $C_L \leqslant$ 100 pF (see Figs 12 and 13)					
Output data valid	t_{pv}	–	–	4	μs
Input data set-up	t_{ps}	0	–	–	μs
Input data hold	t_{ph}	4	–	–	μs

parameter	symbol	min.	typ.	max.	unit
Interrupt $\overline{INT}$ (pin 13)					
Output current LOW at V_{OL} = 0,4 V	I_{OL}	1,6	–	–	mA
Output current HIGH at $V_{OH} = V_{DD}$	$\|I_{OH}\|$	–	–	1	μA
$\overline{INT}$ timing; $C_L \leqslant 100$ pF (see Fig. 13)					
Input data valid	t_{iv}	–	–	4	μs
Reset delay	t_{ir}	–	–	4	μs
Select inputs A0, A1, A2 (pins 1 to 3)					
Input voltage LOW	V_{IH}	−0,5 V	–	$0{,}3V_{DD}$	V
Input voltage HIGH	V_{IH}	$0{,}7V_{DD}$	–	V_{DD} + 0,5 V	V
Input leakage current at $V_I = V_{DD}$ or V_{SS}	$\|I_L\|$	–	–	100	nA

Note 1

The power-on reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$ and sets all ports to logic 1 (input mode with current source to V_{DD}).

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

UNIVERSAL LCD DRIVER FOR LOW MULTIPLEX RATES

GENERAL DESCRIPTION

The PCF8576 is a peripheral device which interfaces to almost any liquid crystal display (LCD) having low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 40 segments and can easily be cascaded for larger LCD applications. The PCF8576 is compatible with most microprocessors/microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

Features

- Single-chip LCD controller/driver
- Selectable backplane drive configuration: static or 2/3/4 backplane multiplexing
- Selectable display bias configuration: static, 1/2 or 1/3
- Internal LCD bias generation with voltage-follower buffers
- 40 segment drives: up to twenty 8-segment numeric characters; up to ten 15-segment alphanumeric characters; or any graphics of up to 160 elements
- 40 x 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- Versatile blinking modes
- LCD and logic supplies may be separated
- Wide power supply range: from 2 V for low-threshold LCDs and up to 9 V for guest-host LCDs and high-threshold (automobile) twisted nematic LCDs
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with any 4-bit, 8-bit or 16-bit microprocessors/microcontrollers
- May be cascaded for large LCD applications (up to 2560 segments possible)
- Cascadable with the 24 segment LCD driver PCF8566
- Optimized pinning for single plane wiring in both single and multiple PCF8576 applications
- Space-saving 56-lead plastic mini-pack (VSO-56)
- Very low external component count (at most one resistor, even in multiple device applications)
- Compatible with chip-on-glass technology
- Manufactured in silicon gate CMOS process

Purchase of Philips' I^2C components conveys a license under the Philips' I^2C patent to use the components in the I^2C-system provided the system conforms to the I^2C specifications defined by Philips.

PACKAGE OUTLINES

PCF8576T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8576U: uncased chip in tray
PCF8576U/10: chip-on-film frame carrier (FFC)

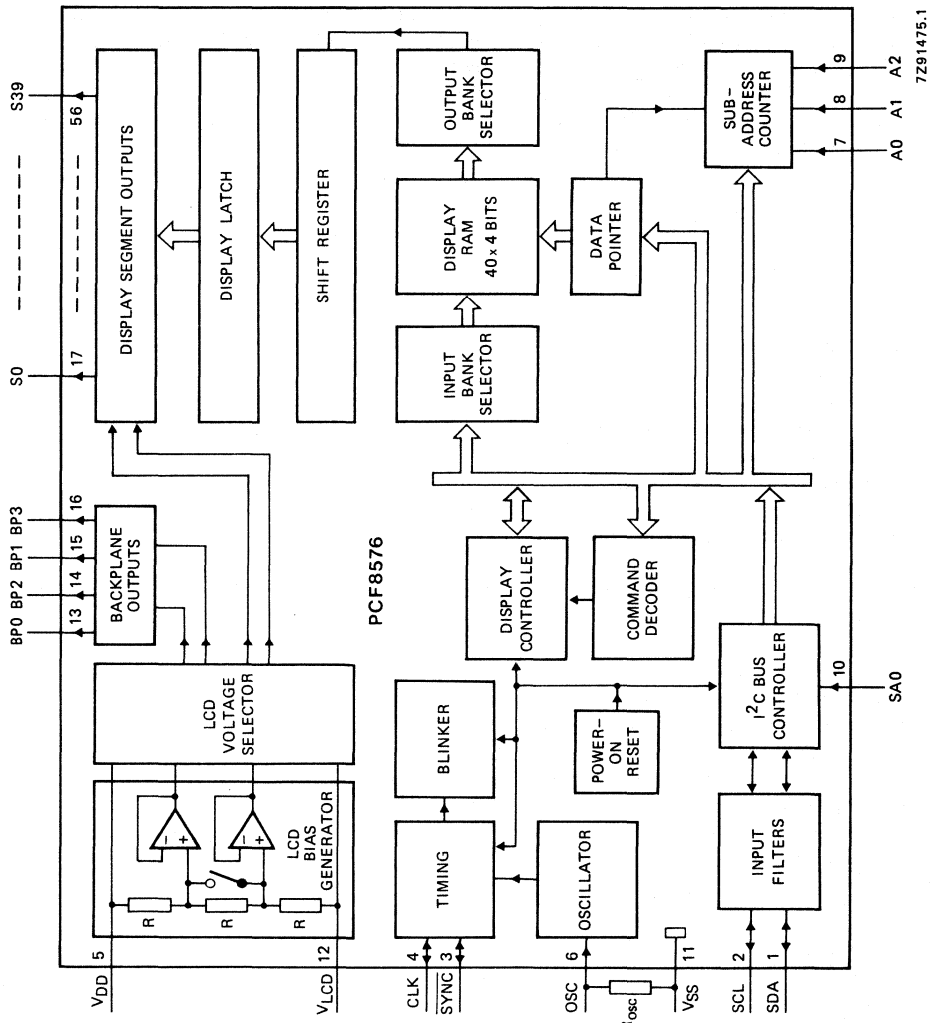


Fig. 1 Block diagram.

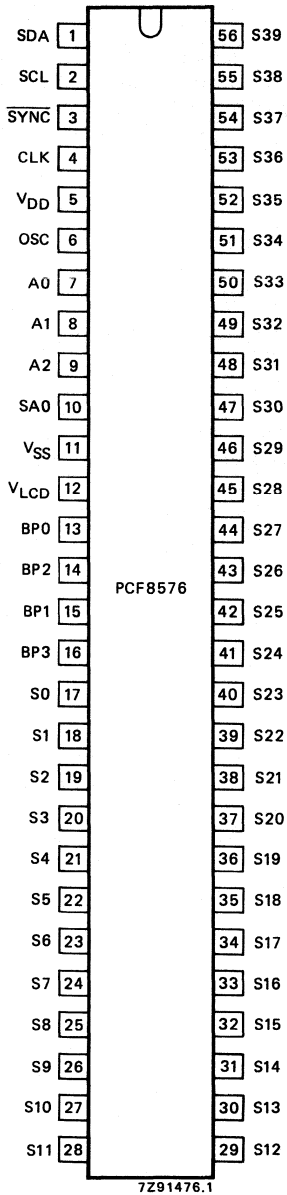


Fig. 2 Pinning diagram.

PINNING

1	SDA	I^2C bus data input/output
2	SCL	I^2C bus clock input/output
3	$\overline{\text{SYNC}}$	cascade synchronization input/output
4	CLK	external clock input/output
5	V_{DD}	positive supply voltage
6	OSC	oscillator input
7	A0	I^2C bus subaddress inputs
8	A1	
9	A2	
10	SA0	I^2C bus slave address bit 0 input
11	V_{SS}	logic ground
12	V_{LCD}	LCD supply voltage
13	BP0	LCD backplane outputs
14	BP2	
15	BP1	
16	BP3	
17 to 56	S0 to S39	LCD segment outputs

FUNCTIONAL DESCRIPTION

The PCF8576 is a versatile peripheral device designed to interface any microprocessor/microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 40 segments. The display configurations possible with the PCF8576 depend on the number of active backplane outputs required; a selection of display configurations is given in Table 1.

Table 1 Selection of display configurations

active back-plane outputs	no. of segments	7-segment numeric	14-segment alphanumeric	dot matrix
4	160	20 digits + 20 indicator symbols	10 characters + 20 indicator symbols	160 dots (4 x 40)
3	120	15 digits + 15 indicator symbols	8 characters + 8 indicator symbols	120 dots (3 x 40)
2	80	10 digits + 10 indicator symbols	5 characters + 10 indicator symbols	80 dots (2 x 40)
1	40	5 digits + 5 indicator symbols	2 characters + 12 indicator symbols	40 dots

All of the display configurations given in Table 1 can be implemented in the typical system shown in Fig. 3. The host microprocessor/microcontroller maintains the 2-line I²C bus communication channel with the PCF8576. A resistor connected between OSC (pin 6) and V_{SS} (pin 11) controls the device clock frequency. The appropiate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are to the power supplies (V_{DD}, V_{SS} and V_{LCD}) and to the LCD panel chosen for the application.

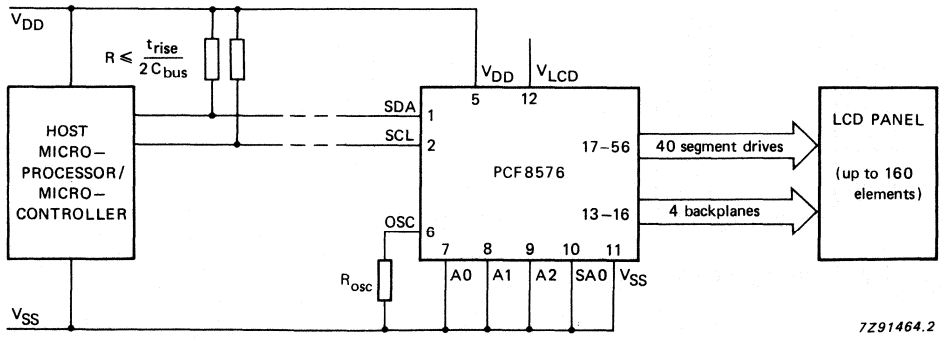


Fig. 3 Typical system configuration.

Power-on reset

At power-on the PCF8576 resets to a defined starting condition as follows:

1. All backplane outputs are set to V_{DD}.
2. All segment outputs are set to V_{DD}.
3. The drive mode '1 : 4 multiplex with 1/3 bias' is selected.
4. Blinking is switched off.
5. Input and output bank selectors are reset (as defined in Table 5).
6. The I^2C bus interface is initialized.
7. The data pointer and the subaddress counter are cleared.

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

LCD bias generator

The full-scale LCD voltage (V_{op}) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the V_{LCD} supply to pin 12. Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{DD} and V_{LCD}. The centre resistor can be switched out of circuit to provide a ½ bias voltage level for the 1 : 2 multiplex configuration.

LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD according to the selected LCD drive configuration. The operation of the voltage selector is controlled by MODE SET commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{op} = V_{DD} - V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 2.

Table 2 Preferred LCD drive modes: summary of characteristics

LCD drive mode	LCD bias configuration	$\frac{V_{off(rms)}}{V_{op}}$	$\frac{V_{on\ (rms)}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$
static (1 BP)	static (2 levels)	0	1	∞
1 : 2 MUX (2 BP)	1/2 (3 levels)	$\sqrt{2}/4 = 0{,}354$	$\sqrt{10}/4 = 0{,}791$	$\sqrt{5} = 2{,}236$
1 : 2 MUX (2 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{5}/3 = 0{,}745$	$\sqrt{5} = 2{,}236$
1 : 3 MUX (3 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{33}/9 = 0{,}638$	$\sqrt{33}/3 = 1{,}915$
1 : 4 MUX (4 BP)	1/3 (4 levels)	$1/3 = 0{,}333$	$\sqrt{3}/3 = 0{,}577$	$\sqrt{3} = 1{,}732$

LCD voltage selector (continued)

A practical value for V_{op} is determined by equating $V_{off(rms)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10% contrast. In the static drive mode a suitable choice is $V_{op} \gtrapprox 3\,V_{th}$.
Multiplex drive ratios of 1 : 3 and 1 : 4 with 1/2 bias are possible but the discrimination and hence the contrast ratios are smaller ($\sqrt{3} = 1{,}732$ for 1 : 3 multiplex or $\sqrt{21}/3 = 1{,}528$ for 1 : 4 multiplex).
The advantage of these modes is a reduction of the LCD full scale voltage V_{op} as follows:

1 : 3 multiplex (1/2 bias) : $V_{op} = \sqrt{6}\,V_{off(rms)} = 2{,}449\,V_{off(rms)}$

1 : 4 multiplex (1/2 bias) : $V_{op} = 4\sqrt{3}/3\;V_{off(rms)} = 2{,}309\,V_{off(rms)}$

These compare with $V_{op} = 3\,V_{off(rms)}$ when 1/3 bias is used.

LCD drive mode waveforms

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Fig. 4.

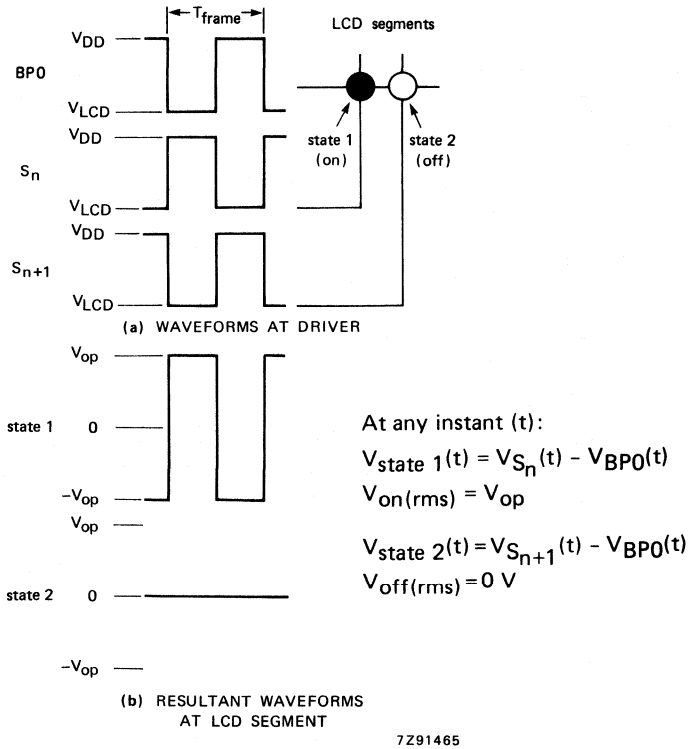


Fig. 4 Static drive mode waveforms: $V_{op} = V_{DD} - V_{LCD}$.

When two backplanes are provided in the LCD the 1 : 2 multiplex drive mode applies. The PCF8576 allows use of 1/2 or 1/3 bias in this mode as shown in Figs 5 and 6.

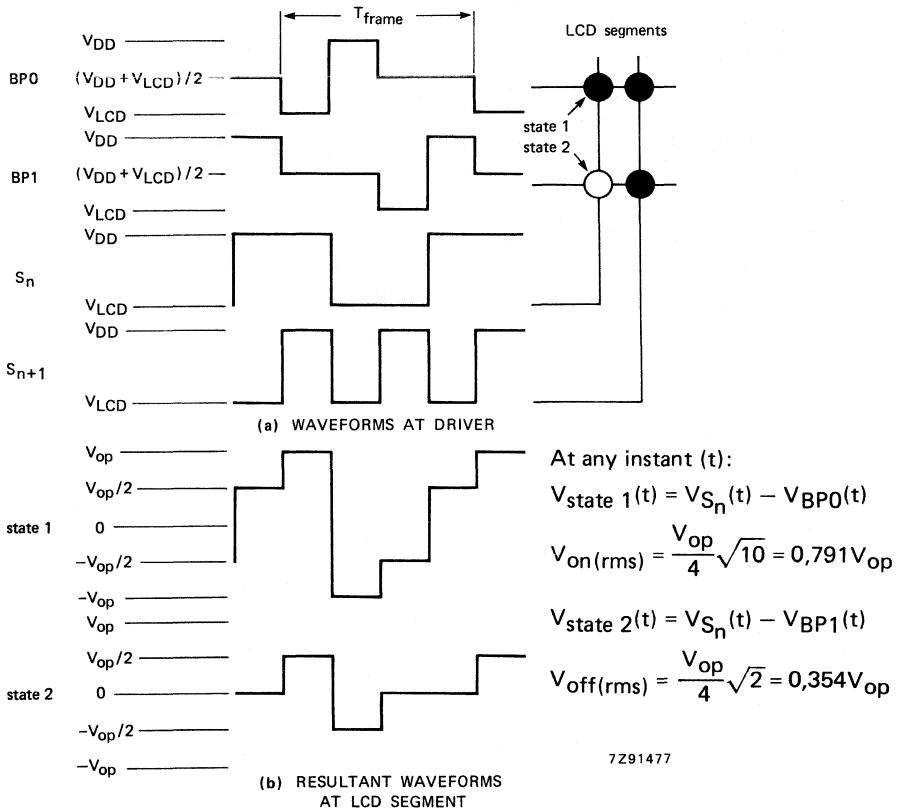


Fig. 5 Waveforms for 1 : 2 multiplex drive mode with 1/2 bias: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

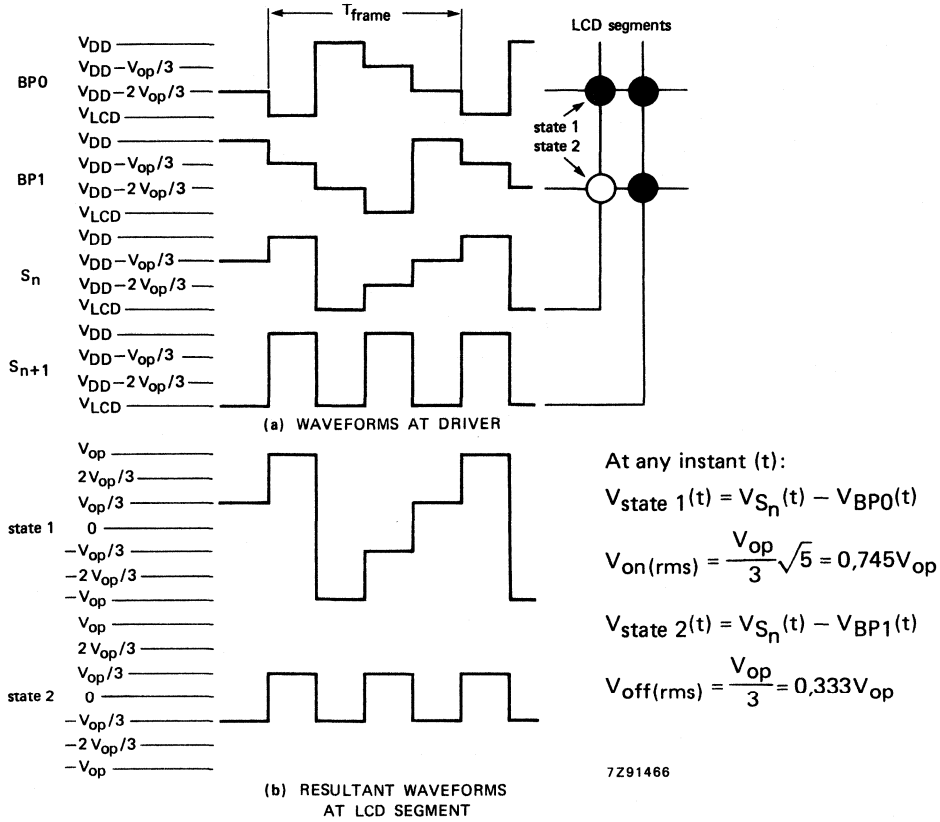


Fig. 6 Waveforms for 1 : 2 multiplex drive mode with 1/3 bias: $V_{op} = V_{DD} - V_{LCD}$.

The backplane and segment drive waveform for the 1 : 3 multiplex drive mode (three LCD backplanes) and for the 1 : 4 multiplex drive mode (four LCD backplanes) are shown in Figs 7 and 8 respectively.

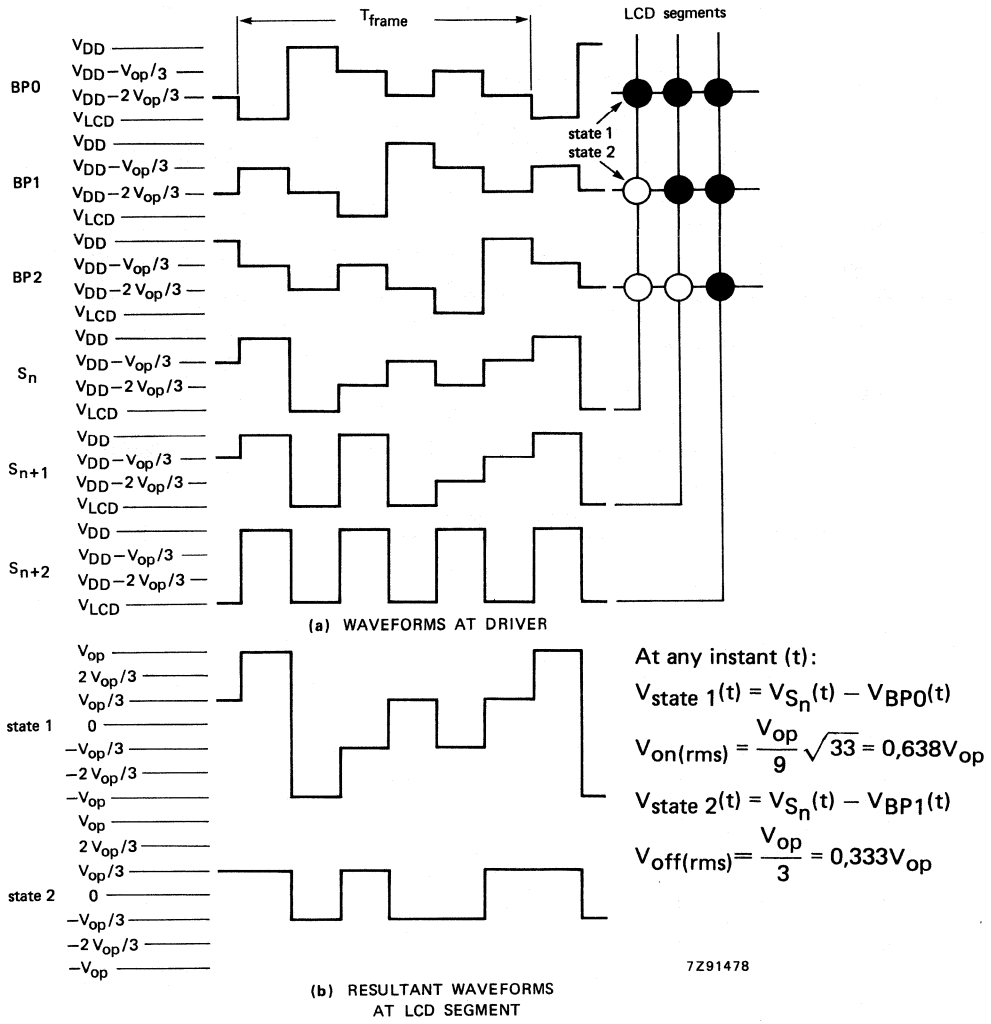


Fig. 7 Waveforms for 1 : 3 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

LCD drive mode waveforms (continued)

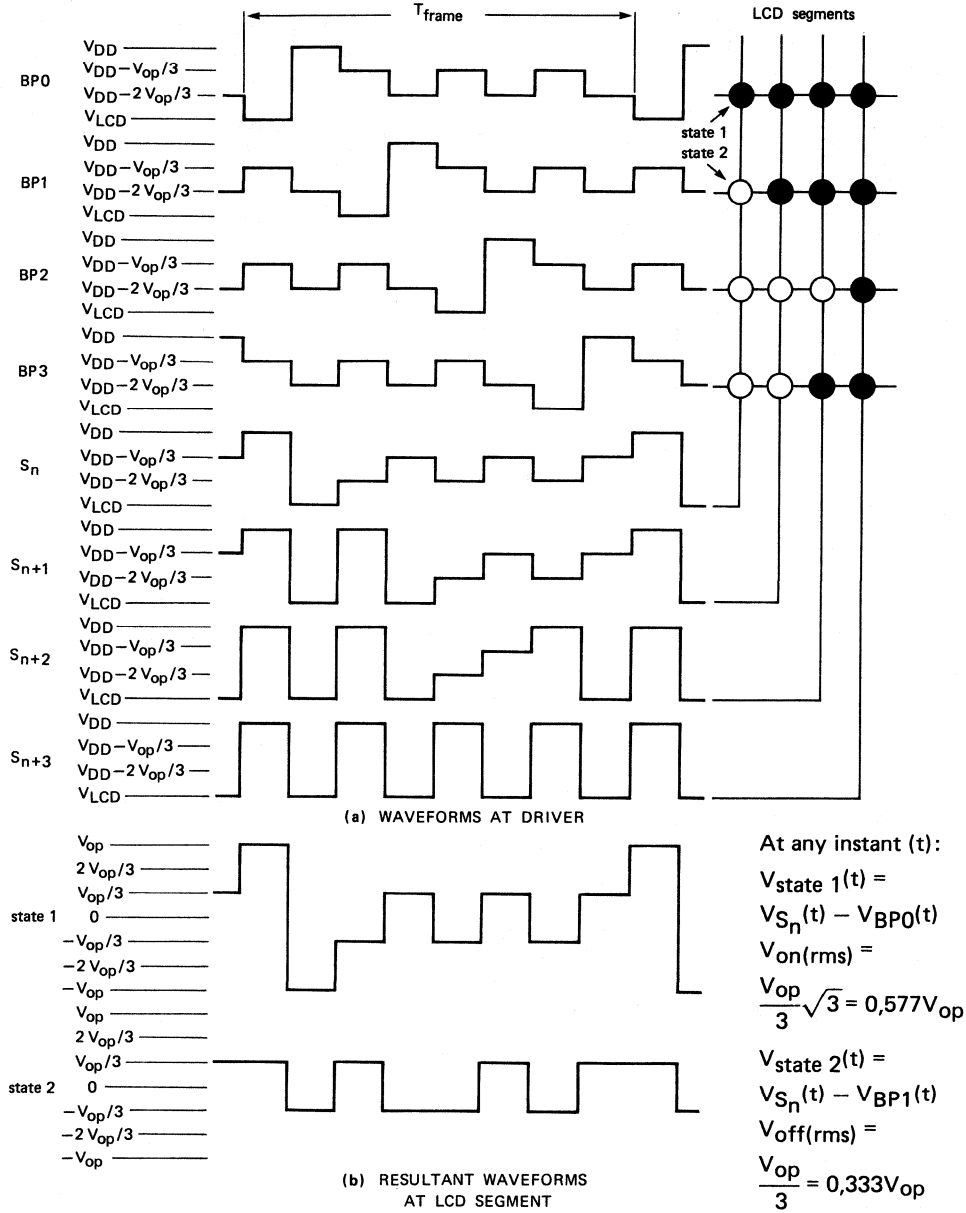


Fig. 8 Waveforms for 1 : 4 multiplex drive mode: $V_{op} = V_{DD} - V_{LCD}$.

Oscillator

Internal clock

The internal logic and the LCD drive signals of the PCF8576 are timed either by the built-in oscillator or from an external clock. When the internal oscillator is used, frequency control is performed by a single resistor connected between OSC (pin 6) and V_{SS} (pin 11) as shown in Fig. 9. In this case, the output from CLK (pin 4) provides the clock signal for cascaded PCF8576s in the system.

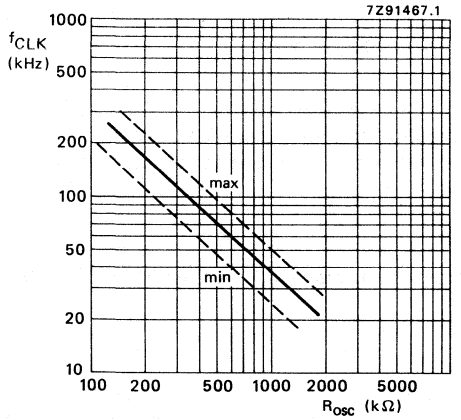


Fig. 9 Oscillator frequency as a function of R_{osc}: $f_{CLK} \approx (3{,}4 \times 10^7 / R_{osc})$ kHz·Ω.

External clock

The condition for external clock is made by tying OSC (pin 6) to V_{DD}; CLK (pin 4) then becomes the external clock input.

The clock frequency (f_{CLK}) determines the LCD frame frequency and the maximum rate for data reception from the I²C bus. To allow I²C bus transmissions at their maximum data rate of 100 kHz, f_{CLK} should be chosen to be above 125 kHz.

A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a d.c. state.

Timing

The timing of the PCF8576 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal $\overline{SYNC}$ maintains the correct timing relationship between the PCF8576s in the system. The timing also generates the LCD frame frequency which it derives as an integer multiple of the clock frequency (Table 3). The frame frequency is set by the choice of value for R_{osc} when internal clock is used, or by the frequency applied to pin 4 when external clock is used.

Table 3 LCD frame frequencies

PCF8576 mode	recommended R_{osc} (kΩ)	f_{frame}	nominal f_{frame} (Hz)
normal mode	180	$f_{CLK}/2880$	64
power-saving mode	1200	$f_{CLK}/480$	64

Timing (continued)

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the normal mode, R_{osc} = 180 kΩ will result in the nominal frame frequency. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six and for the same frame frequency R_{osc} will be 1,2 MΩ. The reduced clock frequency and the increased value of R_{osc} together contribute to a significant reduction in power dissipation. The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the I^2C bus. When a device is unable to 'digest' a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the I^2C bus but no data loss occurs.

Display latch

The display latch holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display latch, the LCD segment outputs and one column of the display RAM.

Shift register

The shift register serves to transfer display information from the display RAM to the display latch while previous data are displayed.

Segment outputs

The LCD drive section includes 40 segment outputs S0 to S39 (pins 17 to 56) which should be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with the data resident in the display latch. When less than 40 segment outputs are required the unused segment outputs should be left open.

Backplane outputs

The LCD drive section includes four backplane outputs BP0 to BP3 which should be connected directly to the LCD. The backplane output signals are generated in accordance with the selected LCD drive mode. If less than four backplane outputs are required the unused outputs can be left open. In the 1 : 3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities. In the 1 : 2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities. In the static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

Display RAM

The display RAM is a static 40 x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the 'on' state of the corresponding LCD segment; similarly, a logic 0 indicates the 'off' state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM column corresponds to the 40 segments operated with respect to backplane BP0 (Fig. 10). In multiplexed LCD applications the segment data of the second, third and fourth column of the display RAM are time-multiplexed with BP1, BP2 and BP3 respectively.

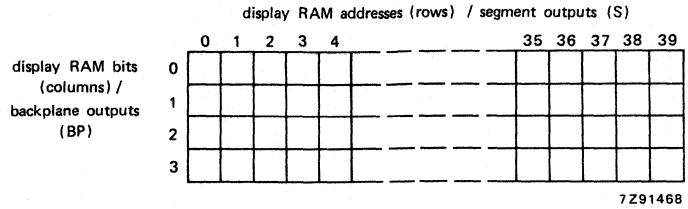


Fig. 10 Display RAM bit-map showing direct relationship between display RAM addresses and segment outputs, and between bits in a RAM word and backplane outputs.

When display data are transmitted to the PCF8576 the display bytes received are stored in the display RAM according to the selected LCD drive mode. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Fig. 11; the RAM filling organization depicted applies equally to other LCD types.

With reference to Fig. 11, in the static drive mode the eight transmitted data bits are placed in bit 0 of eight successive display RAM addresses. In the 1 : 2 multiplex drive mode the eight transmitted data bits are placed in bits 0 and 1 of four successive display RAM addresses. In the 1 : 3 multiplex drive mode these bits are placed in bits 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overriding adjacent data because full bytes are always transmitted. In the 1 : 4 multiplex drive mode the eight transmitted data bits are placed in bits 0, 1, 2 and 3 of two successive display RAM addresses.

Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the LOAD DATA POINTER command. Following this, an arriving data byte is stored starting at the display RAM address indicated by the data pointer thereby observing the filling order shown in Fig. 11. The data pointer is automatically incremented according to the LCD configuration chosen. That is, after each byte is stored, the contents of the data pointer are incremented by eight (static drive mode), by four (1 : 2 multiplex drive mode), by three (1 : 3 multiplex drive mode) or by two (1 : 4 multiplex drive mode).

Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter agree with the hardware subaddress applied to A0, A1 and A2 (pins 7, 8, and 9). The subaddress counter value is defined by the DEVICE SELECT command. If the contents of the subaddress counter and the hardware subaddress do not agree then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

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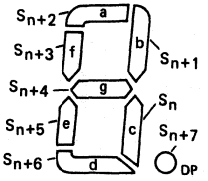
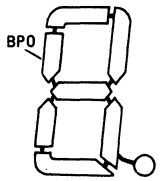
<tr><td>static</td><td> 
</td><td> 
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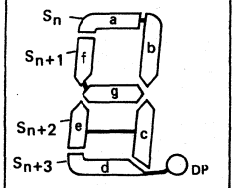
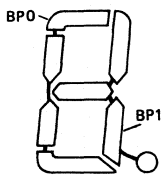
multiplex</td><td> 
</td><td> 
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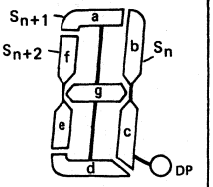
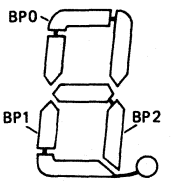
multiplex</td><td> 
</td><td> 
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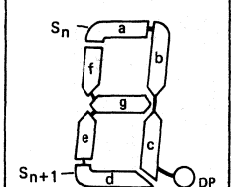
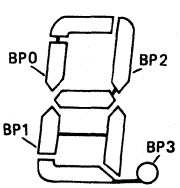
multiplex</td><td> 
</td><td> 
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a c b DP f e g d</td></tr>
</table>

Fig. 11 Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C bus (x = data bit unchanged).

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Subaddress counter (continued)

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are being sent to the display RAM, automatic wrap-over to the next PCF8576 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1 : 3 multiplex mode).

Output bank selector

This selects one of the four bits per display RAM address for transfer to the display latch. The actual bit chosen depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence. In 1 : 4 multiplex, all RAM addresses of bit 0 are the first to be selected, these are followed by the contents of bit 1, bit 2 and then bit 3. Similarly in 1 : 3 multiplex, bits 0, 1 and 2 are selected sequentially. In 1 : 2 multiplex, bits 0 then 1 are selected and, in the static mode, bit 0 is selected.

The PCF8576 includes a RAM bank switching feature in the static and 1 : 2 multiplex drive modes. In the static drive mode, the BANK SELECT command may request the contents of bit 2 to be selected for display instead of bit 0 contents. In the 1 : 2 drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

Input bank selector

The input bank selector loads display data into the display RAM according to the selected LCD drive configuration. Display data can be loaded in bit 2 in static drive mode or in bits 2 and 3 in 1 : 2 drive mode by using the BANK SELECT command. The input bank selector functions independently of the output bank selector.

Blinker

The display blinking capabilities of the PCF8576 are very versatile. The whole display can be blinked at frequencies selected by the BLINK command. The blinking frequencies are integer multiples of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating, as shown in Table 4.

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1 : 2 LCD drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the BLINK command.

In the 1 : 3 and 1 : 4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display is to be blinked at a frequency other than the nominal blinking frequency, this can be effectively performed by resetting and setting the display enable bit E at the required rate using the MODE SET command.

Blinker (continued)

Table 4 Blinking frequencies

blinking mode	normal operating mode ratio	power-saving mode ratio	nominal blinking frequency f_{blink} (Hz)
off	–	–	blinking off
2 Hz	$f_{CLK}/92160$	$f_{CLK}/15360$	2
1 Hz	$f_{CLK}/184320$	$f_{CLK}/30720$	1
0,5 Hz	$f_{CLK}/368640$	$f_{CLK}/61440$	0,5

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

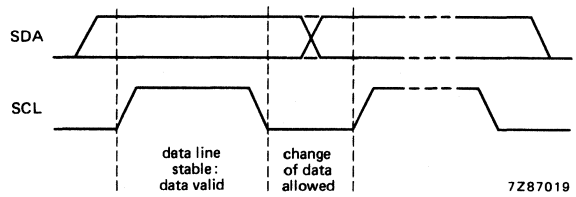


Fig. 12 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

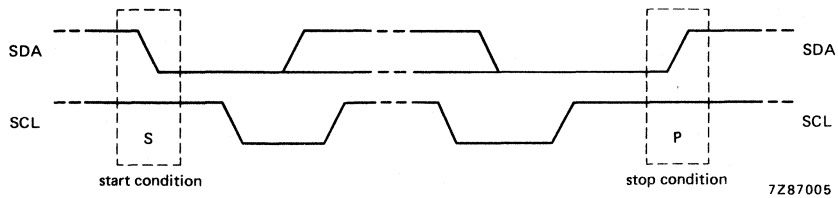


Fig. 13 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is a "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

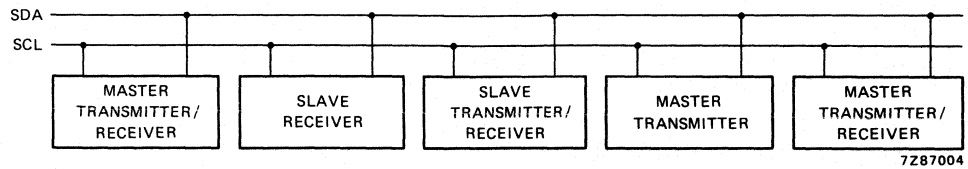


Fig. 14 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

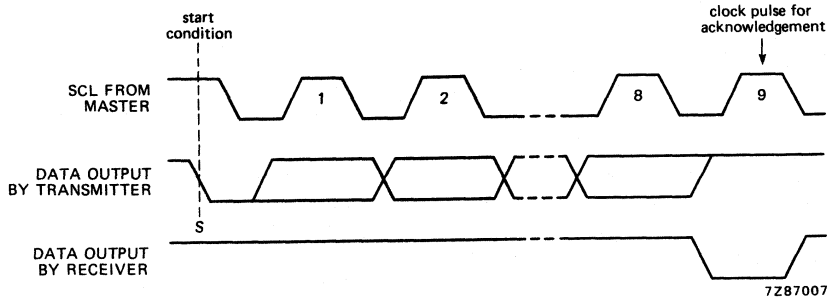


Fig. 15 Acknowledgement on the I^2C bus.

Note

The general characteristics and detailed specification of the I^2C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

PCF8576 I²C bus controller

The PCF8576 acts as an I²C slave receiver. It does not initiate I²C bus transfers or transmit data to an I²C master receiver. The only data output from the PCF8576 are the acknowledge signals of the selected devices. Device selection depends on the I²C bus slave address, on the transferred command data and on the hardware subaddress.

In single device applications, the hardware subaddress inputs A0, A1 and A2 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to V_{SS} or V_{DD} according to a binary coding scheme such that no two devices with a common I²C slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8576 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8576 forces the SCL line LOW until its internal operations are completed. This is known as the 'clock synchronization feature' of the I²C bus and serves to slow down fast transmitters. Data loss does not occur.

Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

I²C bus protocol

Two I²C bus slave addresses (0111000 and 0111001) are reserved for PCF8576. The least-significant bit of the slave address that a PCF8576 will respond to is defined by the level tied at its input SA0 (pin 10). Therefore, two types of PCF8576 can be distinguished on the same I²C bus which allows:

(a) up to 16 PCF8576s on the same I²C bus for very large LCD applications;

(b) the use of two types of LCD multiplex on the same I²C bus.

The I²C bus protocol is shown in Fig. 16. The sequence is initiated with a start condition (S) from the I²C bus master which is followed by one of the two PCF8576 slave addresses available. All PCF8576s with the corresponding SA0 level acknowledge in parallel the slave address but all PCF8576s with the alternative SA0 level ignore the whole I²C bus transfer. After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8576s. The last command byte is tagged with a cleared most-significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8576s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display data bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data are directed to the intended PCF8576 device. The acknowledgement after each byte is made only by the (A0, A1, A2) addressed PCF8576. After the last display byte, the I²C bus master issues a stop condition (P).

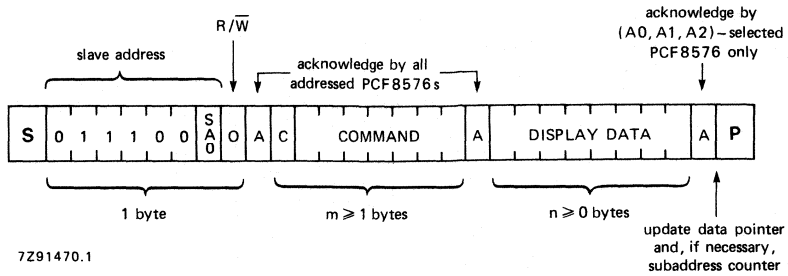


Fig. 16 I²C bus protocol.

Command decoder

The command decoder identifies command bytes that arrive on the I²C bus. All available commands carry a continuation bit C in their most-significant bit position (Fig. 17). When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If the bit is reset, it indicates the last command byte of the transfer. Further bytes will be regarded as display data.

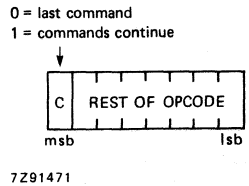


Fig. 17 General format of command byte.

The five commands available to the PCF8576 are defined in Table 5.

Command decoder (continued)

Table 5 Definition of PCF8576 commands

command/opcode	options	description
MODE SET C 1 0 LP E B M1 M0	LCD drive mode: bits M1 M0 static (1 BP): 0 1 1 : 2 MUX (2 BP): 1 0 1 : 3 MUX (3 BP): 1 1 1 : 4 MUX (4 BP): 0 0 LCD bias: bit B 1/3 bias: 0 1/2 bias: 1 display status: bit E disabled (blank): 0 enabled: 1 mode: bit LP normal mode: 0 power-saving mode: 1	Defines LCD drive mode Defines LCD bias configuration Defines display status The possibility to disable the display allows implementation of blinking under external control Defines power dissipation mode
LOAD DATA POINTER C 0 P5 P4 P3 P2 P1 P0	bits P5 P4 P3 P2 P1 P0 6-bit binary value of 0 to 39	Six bits of immediate data, bits P5 to P0, are transferred to the data pointer to define one of forty display RAM addresses
DEVICE SELECT C 1 1 0 0 A2 A1 A0	bits A0 A1 A2 3-bit binary value of 0 to 7	Three bits of immediate data, bits A0 to A2, are transferred to the subaddress counter to define one of eight hardware subaddresses

<table>
<tr><th>command/opcode</th><th>options</th><th>description</th></tr>
<tr><td>BANK SELECT

C 1 1 1 1 0 I O</td><td>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit I</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
<table>
<tr><td>static</td><td>1 : 2 MUX</td><td>bit O</td></tr>
<tr><td>RAM bit 0
RAM bit 2</td><td>RAM bits 0, 1
RAM bits 2, 3</td><td>0
1</td></tr>
</table>
</td><td>Defines input bank selection (storage of arriving display data)

Defines output bank selection (retrieval of LCD display data)

The BANK SELECT command has no effect in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
<tr><td>BLINK

C 1 1 1 0 A BF1 BF0</td><td>
<table>
<tr><td>blink frequency</td><td>bits BF1</td><td>BF0</td></tr>
<tr><td>off</td><td>0</td><td>0</td></tr>
<tr><td>2 Hz</td><td>0</td><td>1</td></tr>
<tr><td>1 Hz</td><td>1</td><td>0</td></tr>
<tr><td>0,5 Hz</td><td>1</td><td>1</td></tr>
</table>
<table>
<tr><td>blink mode</td><td>bit A</td></tr>
<tr><td>normal blinking
alternation blinking</td><td>0
1</td></tr>
</table>
</td><td>Defines the blinking frequency

Selects the blinking mode; normal operation with frequency set by bits BF1, BF0, or blinking by alternation of display RAM banks. Alternation blinking does not apply in 1 : 3 and 1 : 4 multiplex drive modes</td></tr>
</table>

Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8576 and coordinates their effects. The controller is also responsible for loading display data into the display RAM as required by the filling order.

Cascaded operation

In large display configurations, up to 16 PCF8576s can be distinguished on the same I²C bus by using the 3-bit hardware subaddress (A0, A1, A2) and the programmable I²C slave address (SA0). It is also possible to cascade up to 16 PCF8576s. When cascaded, several PCF8576s are synchronized so that they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8576s of the cascade contribute additional segment outputs but their backplane outputs are left open (Fig. 18).

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8576s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidently lost (e.g. by noise in adverse electrical environments; or by the definition of a multiplex mode when PCF8576s with differing SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output section being realized as an open-drain driver with an internal pull-up resistor. A PCF8576 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8576 to assert $\overline{\text{SYNC}}$. The timing relationships between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8576 are shown in Fig. 19.

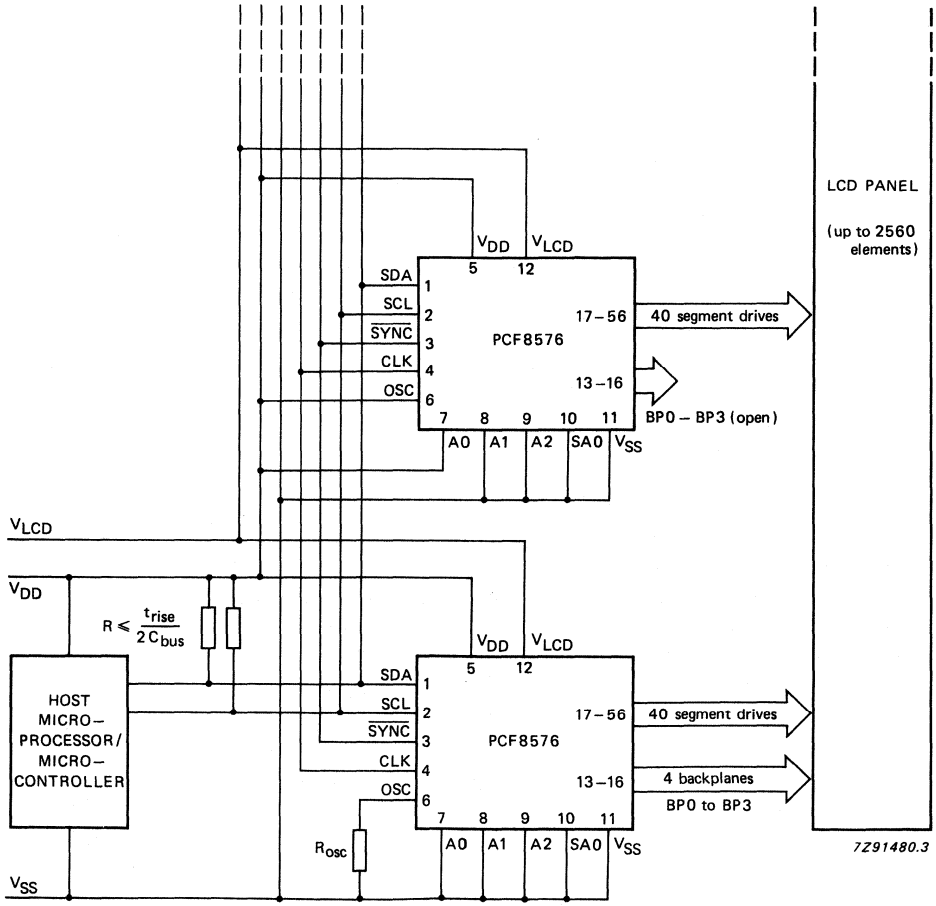
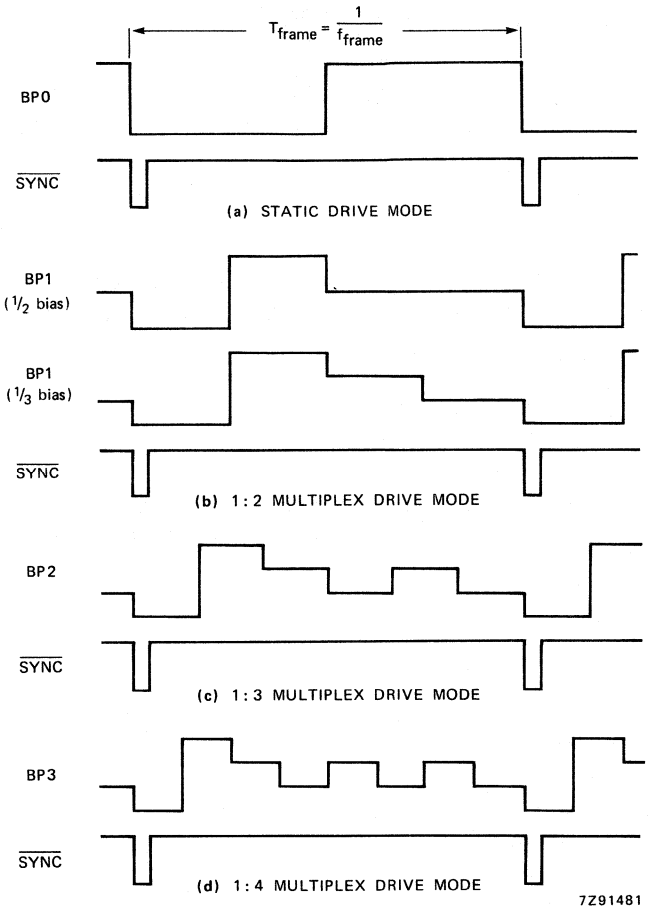


Fig. 18 Cascaded PCF8576 configuration.



Note

Excessive capacitive coupling between SCL or CLK and SYNC may cause erroneous synchronization. If this proves to be a problem, the capacitance of the $\overline{SYNC}$ line should be increased (e.g. by an external capacitor between $\overline{SYNC}$ and V_{DD}). Degradation of the positive edge of the $\overline{SYNC}$ pulse may be countered by an external pull-up resistor.

Fig. 19 Synchronization of the cascade for the various PCF8576 drive modes.

For single plane wiring of packaged PCF8576s and chip-on-glass cascading, see 'APPLICATION INFORMATION'.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to + 11 V
LCD supply voltage range	V_{LCD}		V_{DD}−11 to V_{DD} V
Input voltage range (SCL; SDA; A0 to A2; OSC; CLK; $\overline{SYNC}$; SA0)	V_I		V_{SS} −0,5 to V_{DD} + 0,5 V
Output voltage range (S0 to S39; BP0 to BP3)	V_O		V_{LCD}−0,5 to V_{DD} + 0,5 V
D.C. input current	$\pm I_I$	max.	20 mA
D.C. output current	$\pm I_O$	max.	25 mA
V_{DD}, V_{SS} or V_{LCD} current	$\pm I_{DD}$, $\pm I_{SS}$, $\pm I_{LCD}$	max.	50 mA
Power dissipation per package	P_{tot}	max.	400 mW
Power dissipation per output	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to + 150 °C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

D.C. CHARACTERISTICS

V_{SS} = 0 V; V_{DD} = 2 to 9 V; V_{LCD} = V_{DD}−2 to V_{DD}−9 V;

T_{amb} = −40 to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Operating supply voltage	V_{DD}	2	–	9	V
LCD supply voltage (note 1)	V_{LCD}	V_{DD}−9	–	V_{DD}−2	V
Operating supply current (normal mode) at f_{CLK} = 200 kHz (note 2)	I_{DD}	–	–	180	μA
Power-saving mode supply current at V_{DD} = 3,5 V; V_{LCD} = 0 V; f_{CLK} = 35 kHz (note 2)	I_{LP}	–	–	60	μA
Logic					
Input voltage LOW	V_{IL}	V_{SS}	–	0,3 V_{DD}	V
Input voltage HIGH	V_{IH}	0,7 V_{DD}	–	V_{DD}	V
Output voltage LOW at I_O = 0 mA	V_{OL}	–	–	0,05	V
Output voltage HIGH at I_O = 0 mA	V_{OH}	V_{DD}−0,05	–	–	V
Output current LOW (CLK, $\overline{SYNC}$) at V_{OL} = 1,0 V; V_{DD} = 5 V	I_{OL1}	1	–	–	mA
Output current HIGH (CLK) at V_{OH} = 4,0 V; V_{DD} = 5 V	I_{OH}	–	–	−1	mA
Output current LOW (SDA; SCL) at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL2}	3	–	–	mA
Leakage current (SA0; A0 to A2; CLK; SCL; SDA) at V_I = V_{SS} or V_{DD}	$\pm I_{L1}$	–	–	1	μA

parameter	symbol	min.	typ.	max.	unit
Leakage current (OSC) at $V_I = V_{DD}$	$\pm I_{L2}$	–	–	1	μA
Pull-up resistor ($\overline{SYNC}$)	R_{SYNC}	20	50	150	kΩ
Power-on reset level (note 3)	V_{REF}	–	1,0	1,6	V
Tolerable spike width on bus	t_{sw}	–	–	100	ns
Input capacitance (note 4)	C_I	–	–	7	pF
LCD outputs					
D.C. voltage component (BP0 to BP3) at C_{BP} = 35 nF	$\pm V_{BP}$	–	20	–	mV
D.C. voltage component (S0 to S39) at C_S = 5 nF	$\pm V_S$	–	20	–	mV
Output impedance (BP0 to BP3) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_{BP}	–	–	5	kΩ
Output impedance (S0 to S39) at $V_{LCD} = V_{DD}-5$ V (note 5)	R_S	–	–	7,0	kΩ

A.C. CHARACTERISTICS (note 6)

V_{SS} = 0 V; V_{DD} = 2 to 9 V; $V_{LCD} = V_{DD}-2$ to $V_{DD}-9$ V;
$T_{amb} = -40$ to + 85 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Oscillator frequency (normal mode) at V_{DD} = 5 V; R_{osc} = 180 kΩ (note 7)	f_{CLK}	125	185	288	kHz
Oscillator frequency (power-saving mode) at V_{DD} = 3,5 V; R_{osc} = 1,2 MΩ	f_{CLKLP}	21	31	48	kHz
CLK HIGH time	t_{CLKH}	1	–	–	μs
CLK LOW time	t_{CLKL}	1	–	–	μs
$\overline{SYNC}$ propagation delay	t_{PSYNC}	–	–	400	ns
$\overline{SYNC}$ LOW time	t_{SYNCL}	1	–	–	μs
Driver delays with test loads at $V_{LCD} = V_{DD}-5$ V	t_{PLCD}	–	–	30	μs

A.C. CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
I²C bus					
Bus free time	t_{BUF}	4,7	–	–	μs
Start condition hold time	$t_{HD;STA}$	4	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4	–	–	μs
Start condition set-up time (repeated start code only)	$t_{SU;STA}$	4,7	–	–	μs
Data hold time	$t_{HD;DAT}$	0	–	–	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Rise time	t_R	–	–	1	μs
Fall time	t_F	–	–	300	ns
Stop condition set-up time	$t_{SU;STO}$	4,7	–	–	μs

Notes to characteristics

1. $V_{LCD} \leqslant V_{DD}-3$ V for 1/3 bias.
2. Outputs open; inputs at V_{SS} or V_{DD}; external clock with 50% duty factor; I²C bus inactive.
3. Resets all logic when $V_{DD} < V_{REF}$.
4. Periodically sampled, not 100% tested.
5. Outputs measured one at a time.
6. All timing values referred to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.
7. At $f_{CLK} < 125$ kHz, I²C bus maximum transmission speed is derated.

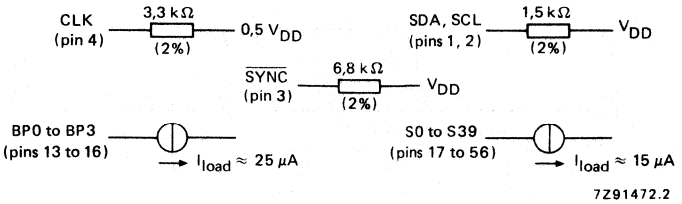


Fig. 20 Test loads.

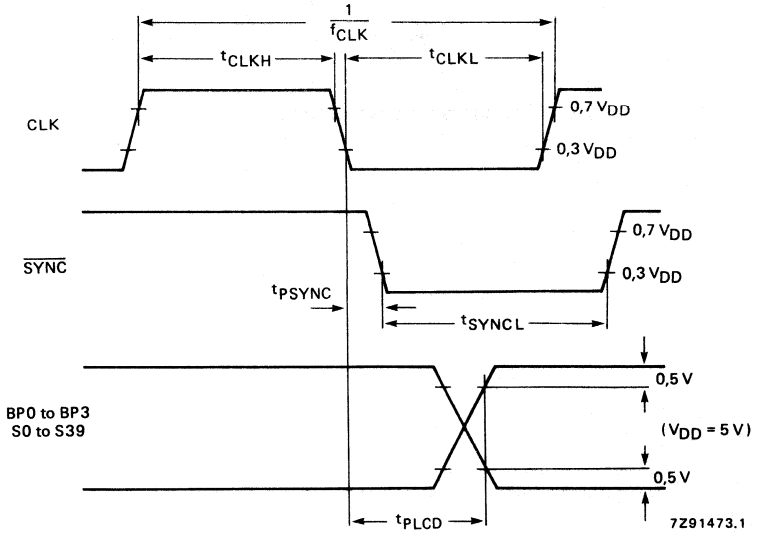


Fig. 21 Driver timing waveforms.

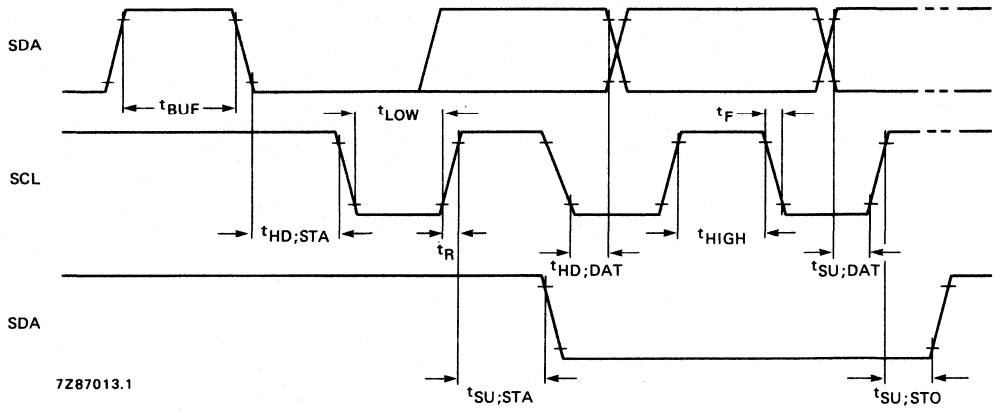
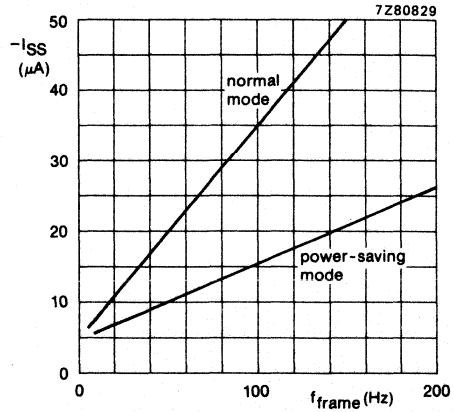
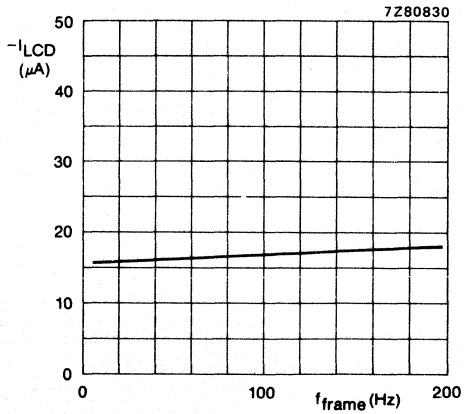


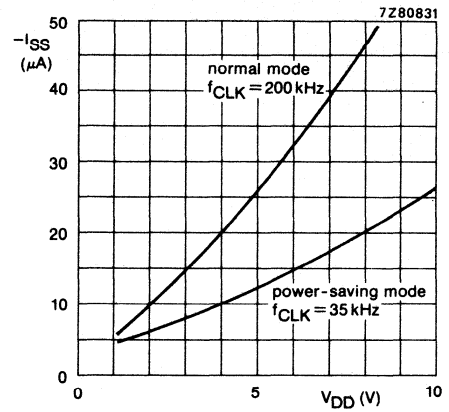
Fig. 22 I²C bus timing waveforms.



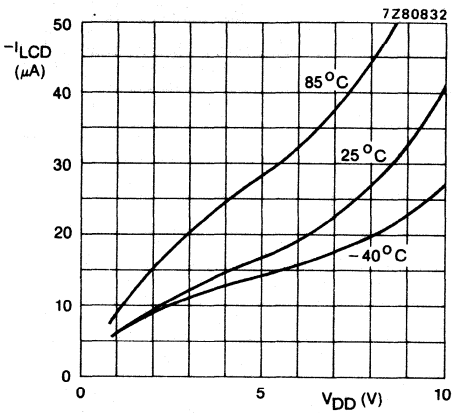
(a) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V; T_{amb} = 25 °C.

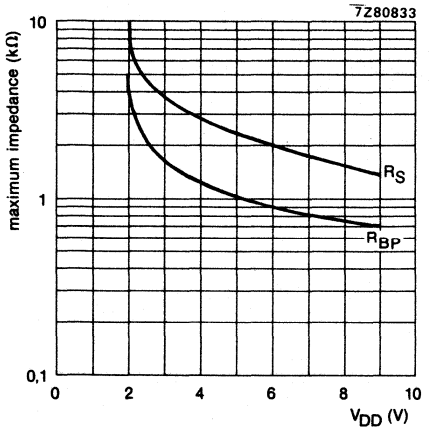


(c) V_{LCD} = 0 V; external clock; T_{amb} = −40 to + 85 °C.

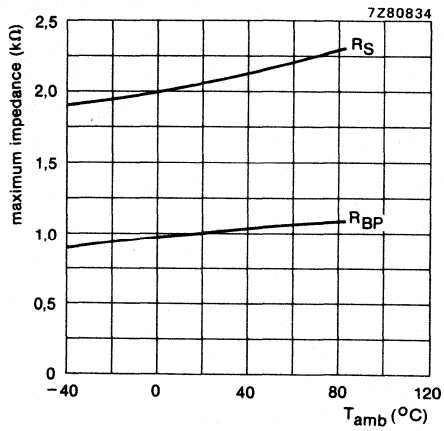


(d) V_{LCD} = 0 V; external clock; f_{CLK} = nominal frequency.

Fig. 23 Typical supply current characteristics.



(a) V_{LCD} = 0 V; T_{amb} = 25 °C.



(b) V_{DD} = 5 V; V_{LCD} = 0 V.

Fig. 24 Typical characteristics of LCD outputs.

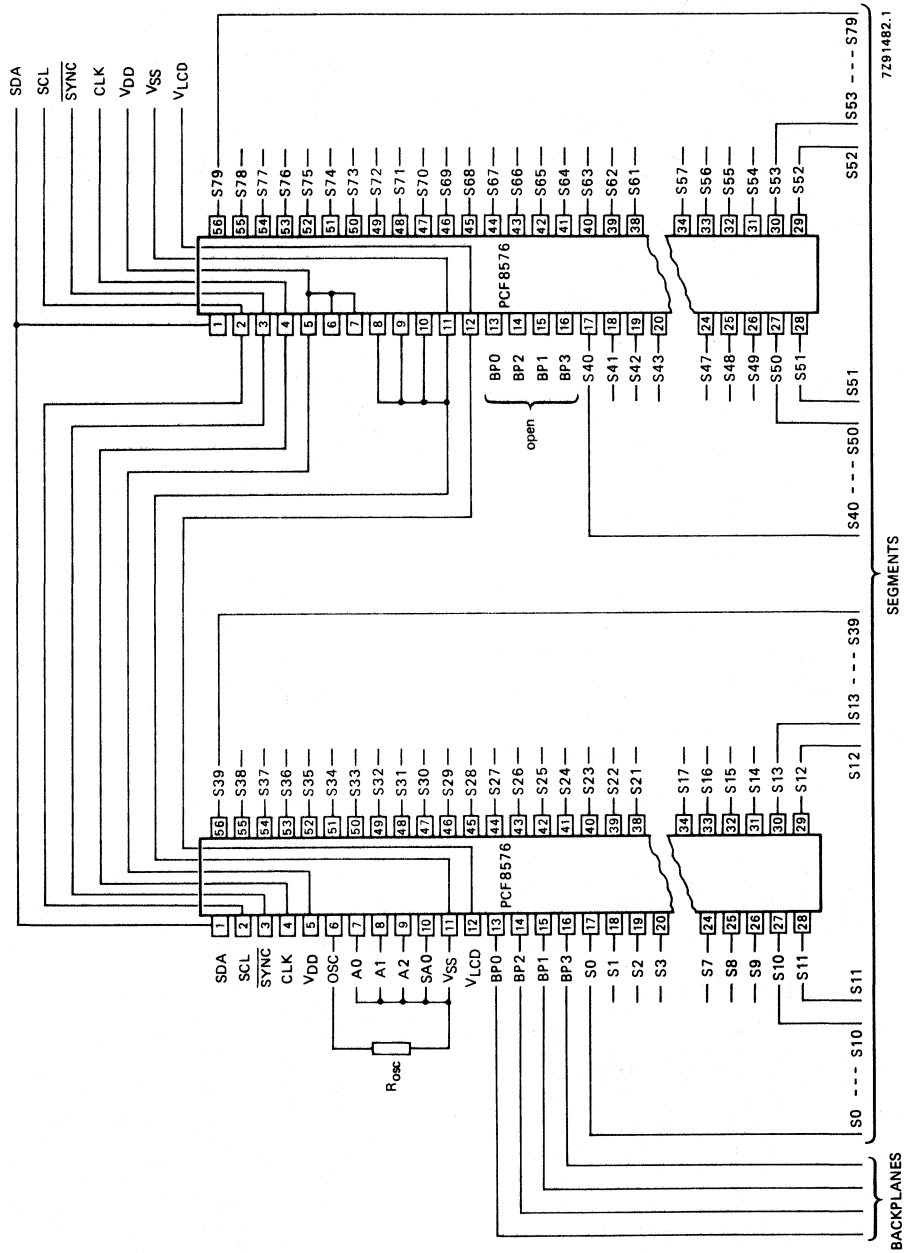


Fig. 25 Single plane wiring of packaged PCF8576s.

APPLICATION INFORMATION

Chip-on-glass cascadability in single plane

In chip-on-glass technology, where driver devices are bonded directly onto the glass of the LCD, it is important that the devices may be cascaded without the crossing of conductors, but the paths of conductors can be continued on the glass under the chip. All of this is facilitated by the PCF8576 bonding pad layout (Fig. 26). Pads needing bus interconnection between all PCF8576s of the cascade are V_{DD}, V_{SS}, V_{LCD}, CLK, SCL, SDA and $\overline{SYNC}$. These lines may be led to the corresponding pads of the next PCF8576 through the wide opening between the V_{LCD} pad and the backplane output pads. The only bussed line that does not require a second opening to lead through to the next PCF8576 is V_{LCD}, being the cascade centre. The placing of V_{LCD} adjacent to V_{SS} allows the two supplies to be tied together.

Fig. 27 shows the connection diagram for a cascaded PCF8576 application with single plane wiring. Note the use of the open space between the V_{LCD} pad and the backplane output pads to route V_{DD}, V_{SS}, CLK, SCL, SDA and $\overline{SYNC}$. The external connections may be made to either end of the cascade, wherever most convenient for the connector.

When an external clocking source is to be used, OSC of all devices should be tied to V_{DD}. The pads OSC, A0, A1, A2 and SA0 have been placed between V_{SS} and V_{DD} to facilitate wiring of oscillator, hardware subaddress and slave address.

APPLICATION INFORMATION (continued)

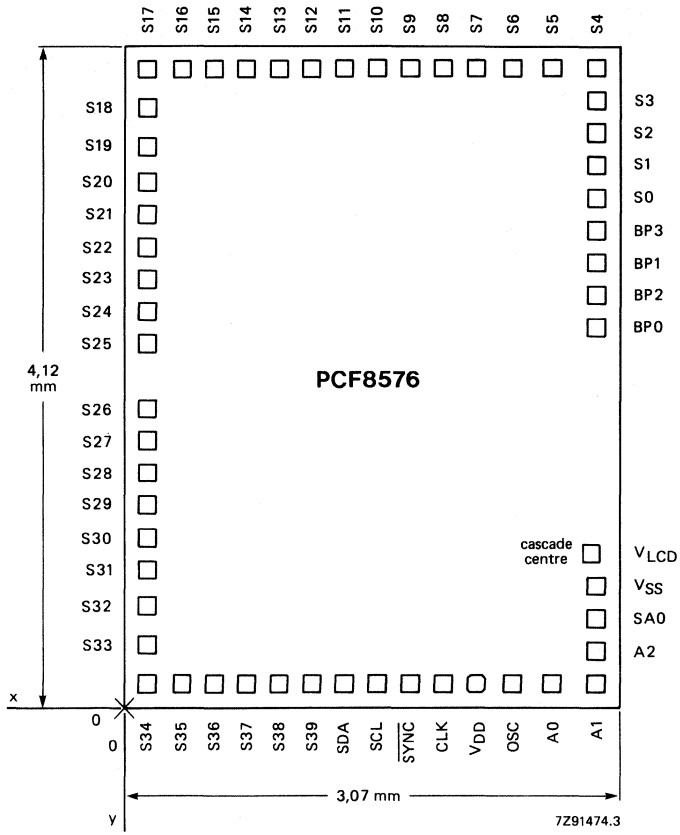


Fig. 26 PCF8576 bonding pad locations.

Bonding pad locations

All x/y coordinates are referenced to left-hand bottom corner (0/0, Fig. 26).

Dimensions in μm

pad	x	y	
S34	160	160	bottom
S35	380	↑	↑
S36	580		
S37	780		
S38	980		
S39	1180		
SDA	1380		
SCL	1580		
$\overline{SYNC}$	1780		
CLK	1980		
V_{DD}	2180		
OSC	2400		
A0	2640		
A1	2910	160	bottom
S17	160	3960	top
S16	380	↑	↑
S15	580		
S14	780		
S13	980		
S12	1180		
S11	1380		
S10	1580		
S9	1780		
S8	1980		
S7	2180		
S6	2400		
S5	2640		
S4	2910	3960	top

pad	x	y	
S33	160	400	left
S32	↑	640	↑
S31		860	
S30		1060	
S29		1260	
S28		1460	
S27		1660	
S26		1860	
S25		2260	
S24		2460	
S23		2660	
S22		2860	
S21		3060	
S20		3260	
S19		3480	
S18	160	3720	left
A2	2910	360	right
SA0	↕	560	↑
V_{SS}	2910	760	
V_{LCD}	2880	960	
BP0	2910	2360	
BP2	↑	2560	
BP1		2760	
BP3		2960	
S0		3160	
S1		3360	
S2		3560	
S3	2910	3760	right

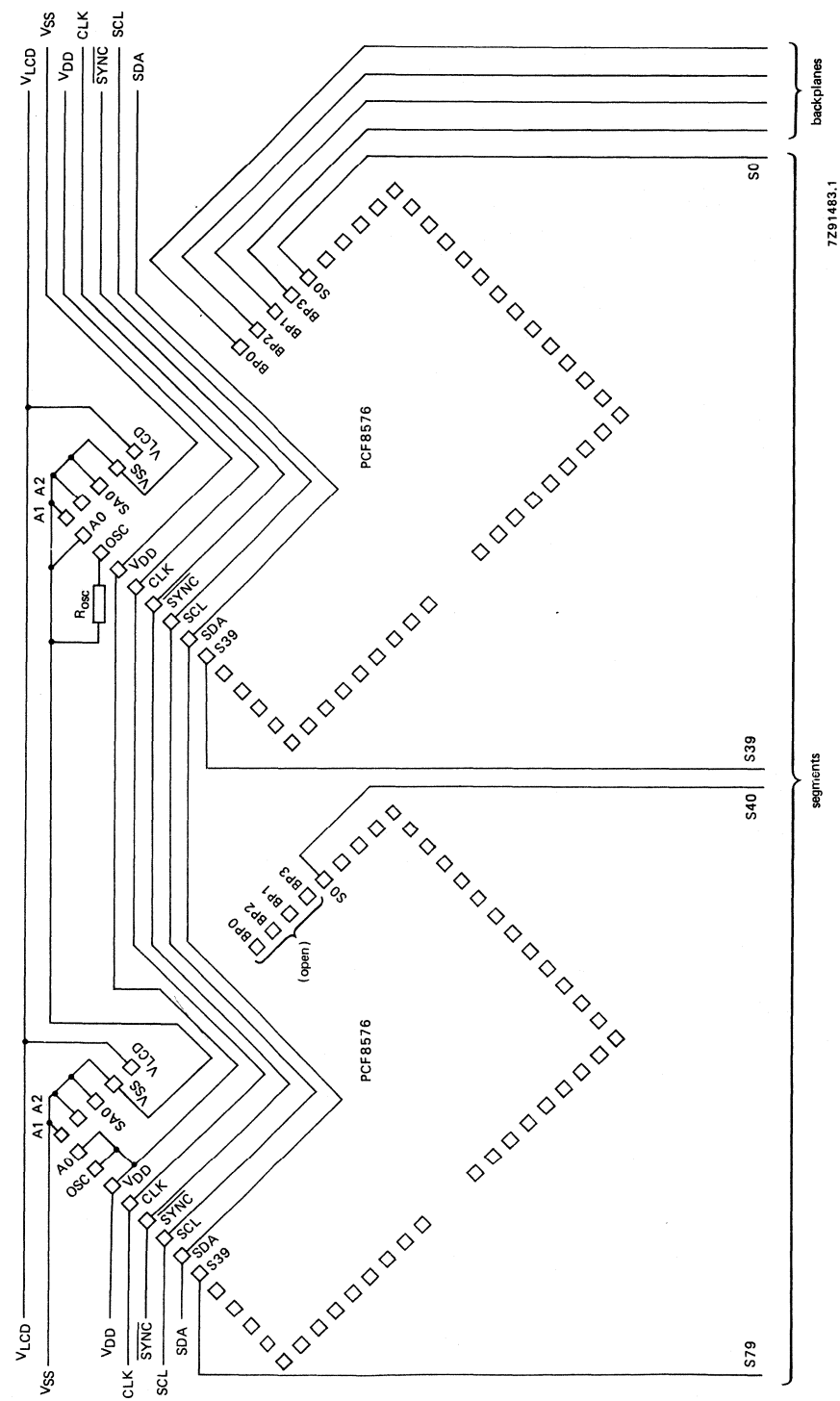


Fig. 27 Chip-on-glass application; cascaded PCF8576s with single-plane wiring (viewed from back of chip).

LCD DIRECT/DUPLEX DRIVER WITH I²C BUS INTERFACE

GENERAL DESCRIPTION

The PCF8577 is a single chip, silicon gate CMOS circuit. It is designed to drive liquid crystal displays with up to 32 segments directly, or 64 segments in a duplex manner.

The two-line I²C bus interface substantially reduces wiring overheads in remote display applications. Bus traffic is minimized in multiple IC applications by automatic address incrementing, hardware sub-addressing and display memory switching (direct drive mode).

The PCF8577 and PCF8577A differ only in their slave address.

Features

- Direct/duplex drive modes with up to 32/64 LCD-segment drive capability per device
- Operating supply voltage: 2,5 to 9 V
- Low power consumption
- I²C bus interface
- Optimized pinning for single plane wiring
- Single-pin built-in oscillator
- Auto-incremented loading across device sub-address boundaries
- Display memory switching in direct drive mode
- May be used for I²C bus output expander
- System expansion up to 256 segments (512 segments with PCF8577A)
- Power-on-reset sets all segments off (to blank)

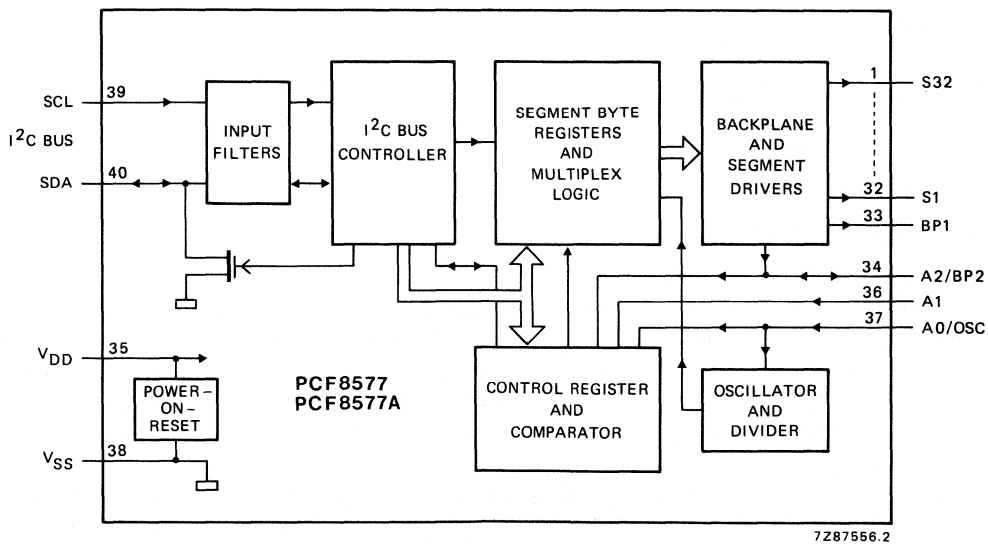


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8577P, PCF8577AP: 40-lead DIL; plastic (SOT129).
PCF8577T, PCF8577AT: 40-lead mini-pack; plastic (VSO40; SOT158A).

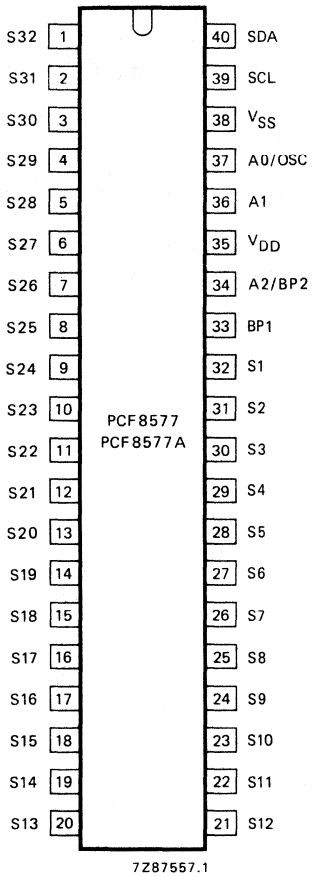


Fig. 2 Pinning diagram.

PINNING

Supply

35	V_{DD}	positive supply
38	V_{SS}	negative supply

I^2C bus

40	SDA	I^2C bus data line
39	SCL	I^2C bus clock line

Inputs

36	A1	hardware address line
37	A0/OSC	hardware address line/oscillator pin

Outputs

1 – 32	S1 – S32	segment outputs

Input – Output

34	A2/BP2	harware address line/cascade sync input/backplane output
33	BP1	cascade sync input/backplane output

FUNCTIONAL DESCRIPTION

Hardware sub-address A0, A1, A2

The hardware sub-address lines A0, A1, A2 are used to program the device sub-address for each PCF8577 on the bus. Lines A0 and A2 are shared with OSC and BP2 respectively to reduce pin-out requirements.

A0/OSC Line A0 is defined as LOW (logic 0) when this pin is used for the local oscillator or when connected to V_{SS}. Line A0 is defined as HIGH (logic 1) when connected to V_{DD}.

A1 Line A1 must be defined as LOW (logic 0) or as HIGH (logic 1) by connection to V_{SS} or V_{DD} respectively.

A2/BP2 In the direct drive mode the second backplane signal BP2 is not used and the A2/BP2 pin is exclusively the A2 input. Line A2 is defined as LOW (logic 0) when connected to V_{SS} or, if this is not possible, by leaving it unconnected (internal pull-down). Line A2 is defined as HIGH (logic 1) when connected to V_{DD}.

In the duplex drive mode the second backplane signal BP2 is required and the A2 signal is undefined. In this mode device selection is made exclusively from lines A0 and A1.

Oscillator A0/OSC

The PCF8577 has a single-pin built-in oscillator which provides the modulation for the LCD segment driver outputs. One external resistor and one external capacitor are connected to the A0/OSC pin to form the oscillator. In an expanded system containing more than one PCF8577 the backplane signals are usually common to all devices and only one oscillator is needed. The devices which are not used for the oscillator are put into the expansion mode by connecting the A0/OSC pin to either V_{DD} or V_{SS} depending on the required state for A0. In the expansion mode each PCF8577 is synchronized from the backplane signal(s).

User-accessible registers

There are nine user-accesible 1-byte registers. The first is a control register which is used to control the loading of data into the segment byte registers and to select display options. The other eight are segment byte registers, split into two banks of storage, which store the segment data. The set of even numbered segment byte registers is called BANK A. Odd numbered segment byte registers are called BANK B.

There are two slave addresses, one for PCF8577, and one for PCF8577A (see Fig. 14). All addressed devices load the second byte into the control register and each device maintains an identical copy of the control byte in the control register at all times (see I²C bus protocol Fig. 15).

The control register is shown in more detail in Fig. 3. The least-significant bits select which device and which segment byte register are loaded next. This part of the register is therefore called the Segment Byte Vector (SBV).

The upper three bits of the SBV (V5 to V3) are compared with the hardware sub-address input signals A2, A1 and A0. If they are the same then the device is enabled for loading, if not the device ignores incoming data but remains active.

The three least-significant bits of the SBV (V2 to V0) address one of the segment byte registers within the enabled chip for loading segment data.

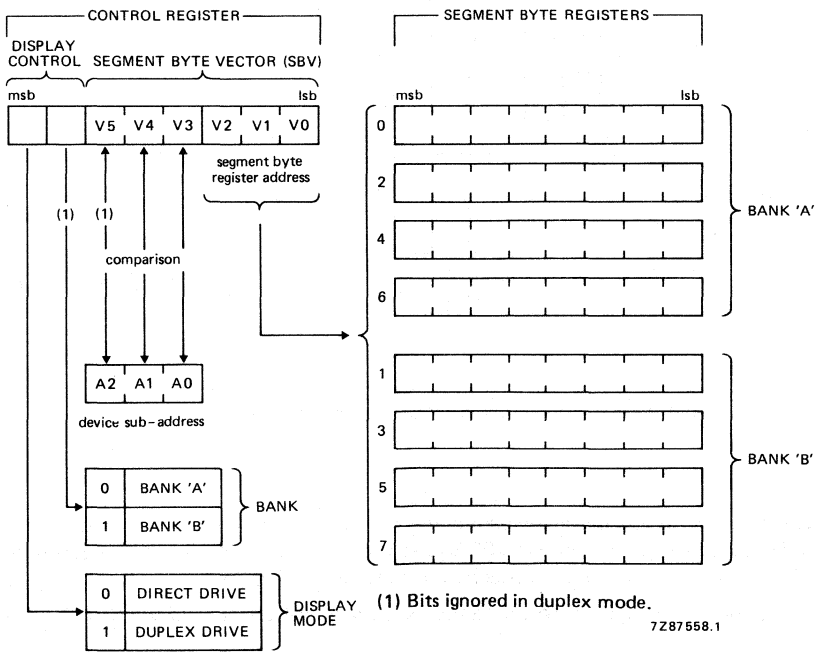


Fig. 3 PCF8577 register organization.

FUNCTIONAL DESCRIPTION (continued)

The control register also has two display control bits. These bits are named MODE and BANK. The MODE bit selects whether the display outputs are configured for direct or duplex drive displays. The BANK bit allows the user to display BANK A or BANK B.

Auto-incremented loading

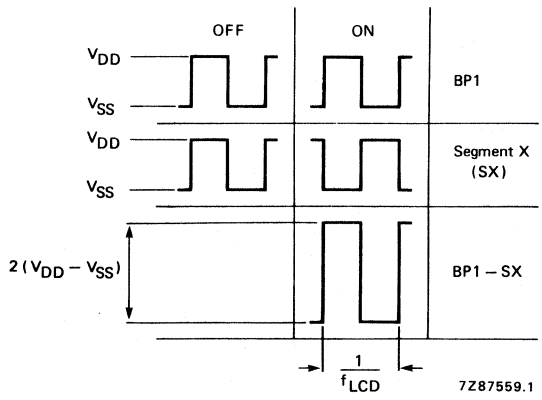
After each segment byte is loaded the SBV is incremented automatically, thus auto-incremented loading occurs if more than one segment byte is received in a data transfer.

Since the SBV addresses both device and segment registers, auto-incremented loading may proceed across device boundaries provided that the hardware sub-addresses are arranged contiguously.

Direct drive mode

The PCF8577 is set to the direct drive mode by loading the MODE control bit with logic 0. In this mode only four bytes are needed to store the data for the 32 segment drivers. Setting the BANK bit to logic 0 selects even bytes (BANK A); setting the BANK bit to logic 1 selects odd bytes (BANK B).

In the direct drive mode the SBV is auto-incremented by two after the loading of each segment byte register. This means that auto-incremented loading of BANK A or BANK B is possible. Either bank may be completely or partially loaded irrespective of which bank is being displayed. Direct drive output waveforms are shown in Fig. 4.



$V_{ON} = V_{DD} - V_{SS}$
$V_{OFF} = 0$

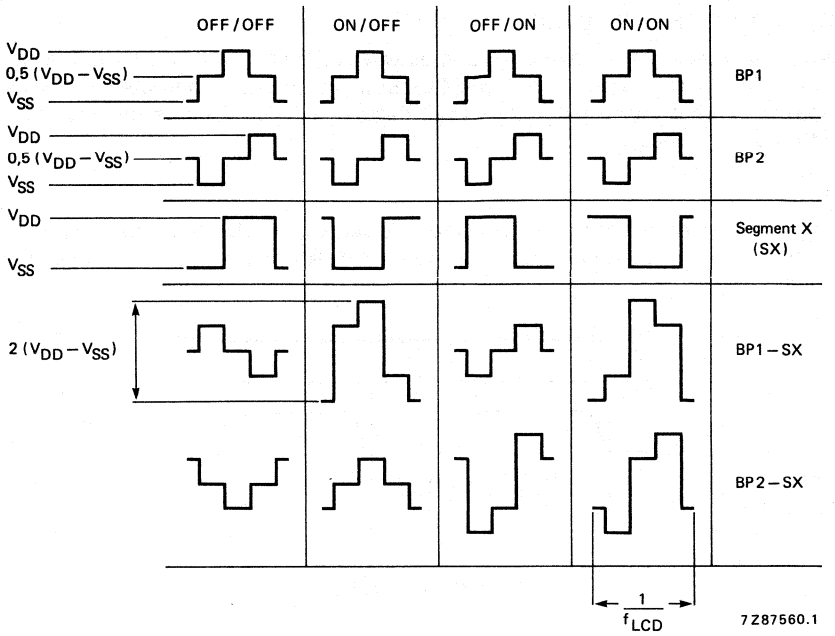
Fig. 4 Direct drive mode display output waveforms.

Duplex mode

The PCF8577 is set to the duplex mode by loading the MODE bit with logic 1. In this mode a second backplane signal (BP2) is needed and pin A2/BP2 is used for this; therefore A2 and its equivalent SBV bit V5 are undefined. The SBV auto-increments by one between loaded bytes.

All of the segment bytes are needed to store data for the 32 segment drivers and the BANK bit is ignored.

Duplex mode output waveforms are shown in Fig. 5.



$$V_{ON} = 0{,}79\ (V_{DD} - V_{SS})$$

$$V_{OFF} = 0{,}35\ (V_{DD} - V_{SS})$$

$$\frac{V_{ON}}{V_{OFF}} = 2{,}26$$

Fig. 5 Duplex mode display output waveforms.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

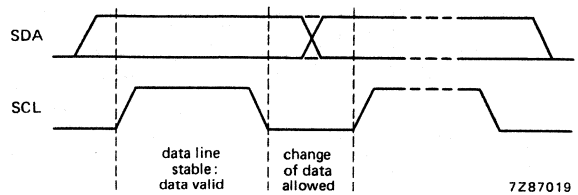


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

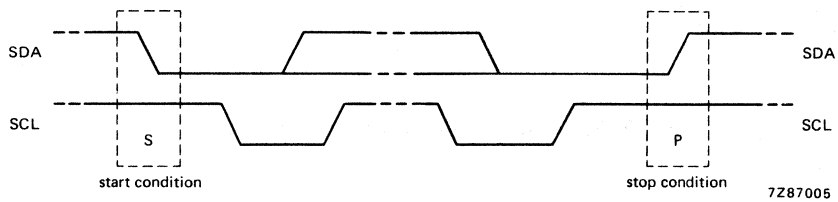


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

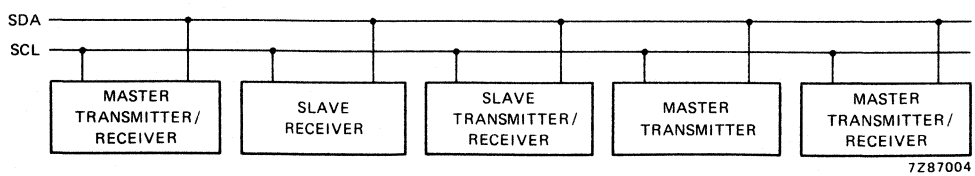


Fig. 8 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

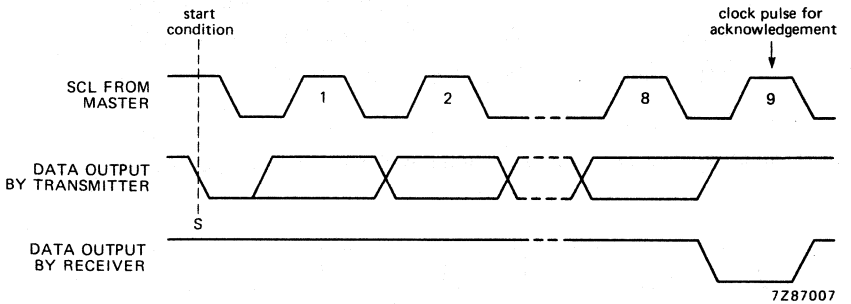


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Within the I²C bus specifications a high-speed mode and a low-speed mode are defined. The PCF8577 operates in both modes and the timing requirements are as follows:

High-speed mode

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

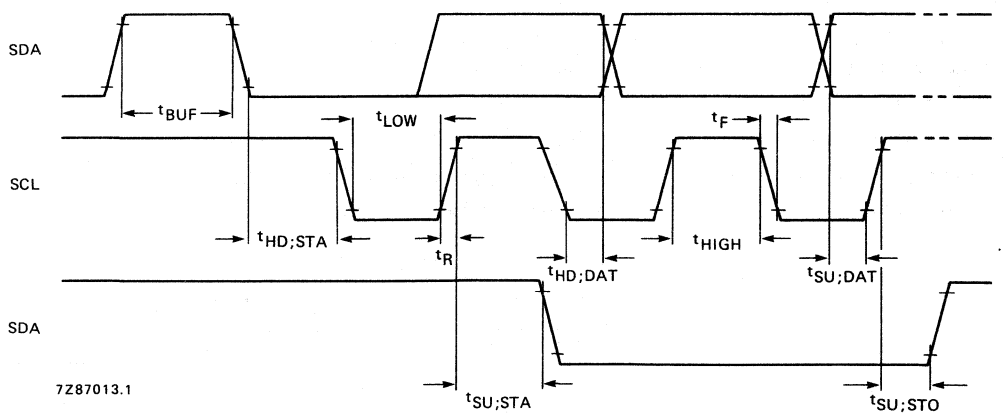


Fig. 10 Timing of the high-speed mode.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_R	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_F	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}.

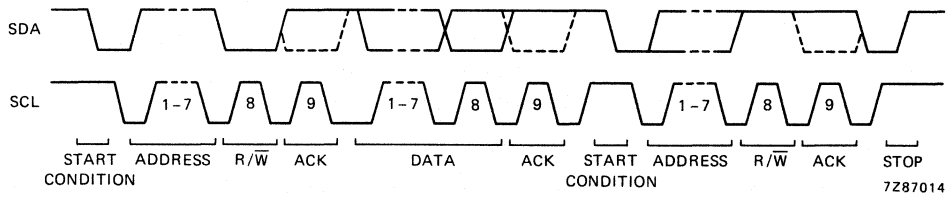


Fig. 11 Complete data transfer in the high-speed mode.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Mark-to-space ratio	1 : 1 (LOW-to-HIGH)
Max. number of bytes	unrestricted
Premature termination of transfer	allowed by generation of STOP condition
Acknowledge clock bit	must be provided by the master

Low-speed mode

Masters generate a bus clock with a maximum frequency of 2 kHz; a minimum LOW period of 105 μs and a minimum HIGH period of 365 μs. The mark-to-space ratio is 1 : 3 LOW-to-HIGH. Detailed timing is shown in Fig. 12.

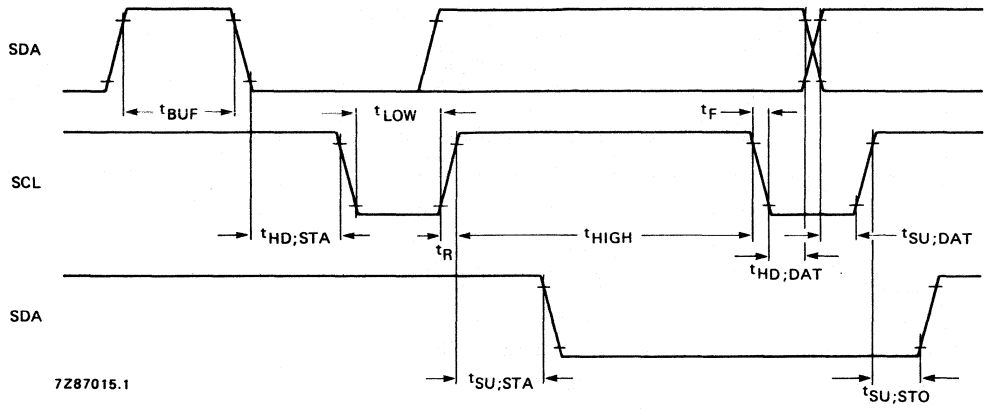


Fig. 12 Timing of the low-speed mode.

Where:

t_{BUF}	$t \geqslant 105\ \mu s\ (t_{LOWmin})$
$t_{HD;STA}$	$t \geqslant 365\ \mu s\ (t_{HIGHmin})$
t_{LOW}	130 μs ± 25 μs
t_{HIGH}	390 μs ± 25 μs
$t_{SU;STA}$	130 μs ± 25 μs*
$t_{HD;DAT}$	$t \geqslant 0\ \mu s$
$t_{SU;DAT}$	$t \geqslant 250$ ns
t_R	$t \leqslant 1\ \mu s$
t_F	$t \leqslant 300$ ns
$t_{SU;STO}$	130 μs ± 25 μs

Note

All the timing values referred to V_{IH} and V_{IL} levels with a voltage swing of V_{SS} to V_{DD}, for definitions see high-speed mode.

* Only valid for repeated start code.

CHARACTERISTICS OF THE I²C BUS (continued)

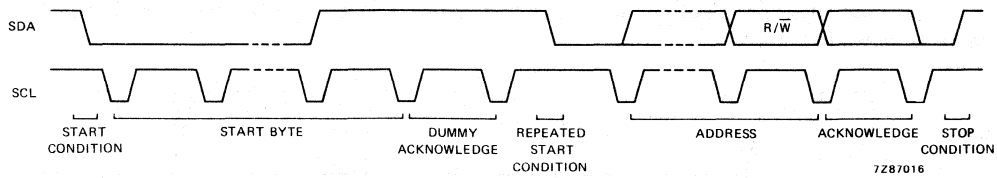


Fig. 13 Complete data transfer in the low-speed mode.

Where:

Clock t_{LOWmin}	130 μs ± 25 μs
$t_{HIGHmin}$	390 μs ± 25 μs
Mark-to-space ratio	1 : 3 (LOW-to-HIGH)
Start byte	0000 0001
Maximum number of bytes	6
Premature termination of transfer	not allowed
Acknowledge clock bit	must be provided by master

Note

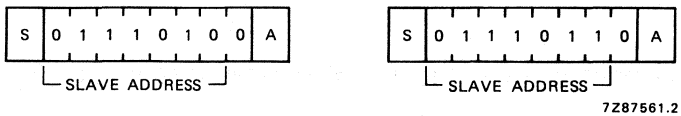
The general characteristics and detailed specification of the I²C bus are described in a separate data sheet (serial data buses) in handbook: ICs for digital systems in radio, audio and video equipment.

ADDRESSING

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure.

Slave address

The slave address for PCF8577 and PCF8577A are shown in Fig. 14.



(a) PCF8577. (b) PCF8577A.

Fig. 14 PCF8577 and PCF8577A slave addresses.

I²C bus protocol

The PCF8577 I²C bus protocol is shown in Fig. 15.

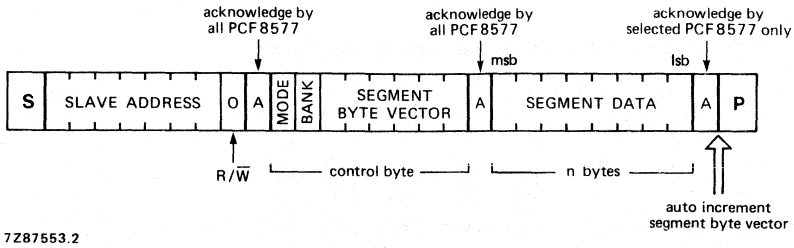


Fig. 15 I²C bus protocol.

The PCF8577 is a slave receiver and has a fixed slave address (Fig. 14). All PCF8577 on the same bus acknowledge the slave address in parallel. The second byte is always the control byte and is loaded into the control register of each PCF8577 on the bus. Subsequent data bytes are loaded into the segment registers of the selected device. Any number of data bytes may be loaded in one transfer and in an expanded system rollover of the SBV from 111 111 to 000 000 is allowed. If a stop (P) condition is given after the control byte acknowledge the segment data remains unchanged. This allows the BANK bit to be toggled without changing the segment register contents. During loading of segment data only the selected PCF8577 gives an acknowledge. Loading is terminated by generating a stop (P) condition.

DEVELOPMENT DATA

DISPLAY MEMORY MAPPING

The mapping between the eight segment registers and the segment outputs S1 to S32 is shown in Tables 1 and 2.

Since only one register bit per segment is needed in the direct drive mode, the BANK bit allows swapping of display information. If BANK is set to logic 0 even bytes (BANK A) are displayed; if BANK is set to logic 1 odd bytes (BANK B) are displayed. BP1 is always used for the backplane output in the direct drive mode.

Table 1 Segment byte — segment driver mapping in the direct drive mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
0	0	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	1	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP1
0	0	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	1	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP1
0	0	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	1	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP1
0	0	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
0	1	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP1

Mapping example: bit 0 of register 7 controls the LCD segment S25 if BANK bit is a logic 1.

DISPLAY MEMORY MAPPING (continued)

Even bytes (BANK A) correspond to backplane 1 (BP1) and odd bytes (BANK B) correspond to backplane 2 (BP2).

Table 2 Segment byte — segment driver mapping in the duplex mode.

MODE	BANK	V2	V1	V0	SEGMENT REGISTER / BIT	MSB 7	6	5	4	3	2	1	LSB 0	BACKPLANE
1	x	0	0	0	0	S8	S7	S6	S5	S4	S3	S2	S1	BP1
1	x	0	0	1	1	S8	S7	S6	S5	S4	S3	S2	S1	BP2
1	x	0	1	0	2	S16	S15	S14	S13	S12	S11	S10	S9	BP1
1	x	0	1	1	3	S16	S15	S14	S13	S12	S11	S10	S9	BP2
1	x	1	0	0	4	S24	S23	S22	S21	S20	S19	S18	S17	BP1
1	x	1	0	1	5	S24	S23	S22	S21	S20	S19	S18	S17	BP2
1	x	1	1	0	6	S32	S31	S30	S29	S28	S27	S26	S25	BP1
1	x	1	1	1	7	S32	S31	S30	S29	S28	S27	S26	S25	BP2

X = don't care.

Mapping example: bit 7 of register 5 controls the LCD segment S24/BP2.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}	−0,5 to 11	V
Voltage on any pin	V_I	V_{SS} − 0,8 to V_{DD} + 0,8	V
D.C. input current	$\pm I_I$	max. 20	mA
D.C. output current	$\pm I_O$	max. 25	mA
V_{DD} or V_{SS} current	$\pm I_{DD}$, I_{SS}	max. 50	mA
Power dissipation per package	P_{tot}	max. 500*	mW
Power dissipation per output	P	max. 100	mW
Operating ambient temperature range	T_{amb}	−40 to +85	°C
Storage temperature range	T_{stg}	−65 to +150	°C

* Derate 7,7 mW/K when $T_{amb} > 60$ °C.

DEVELOPMENT DATA

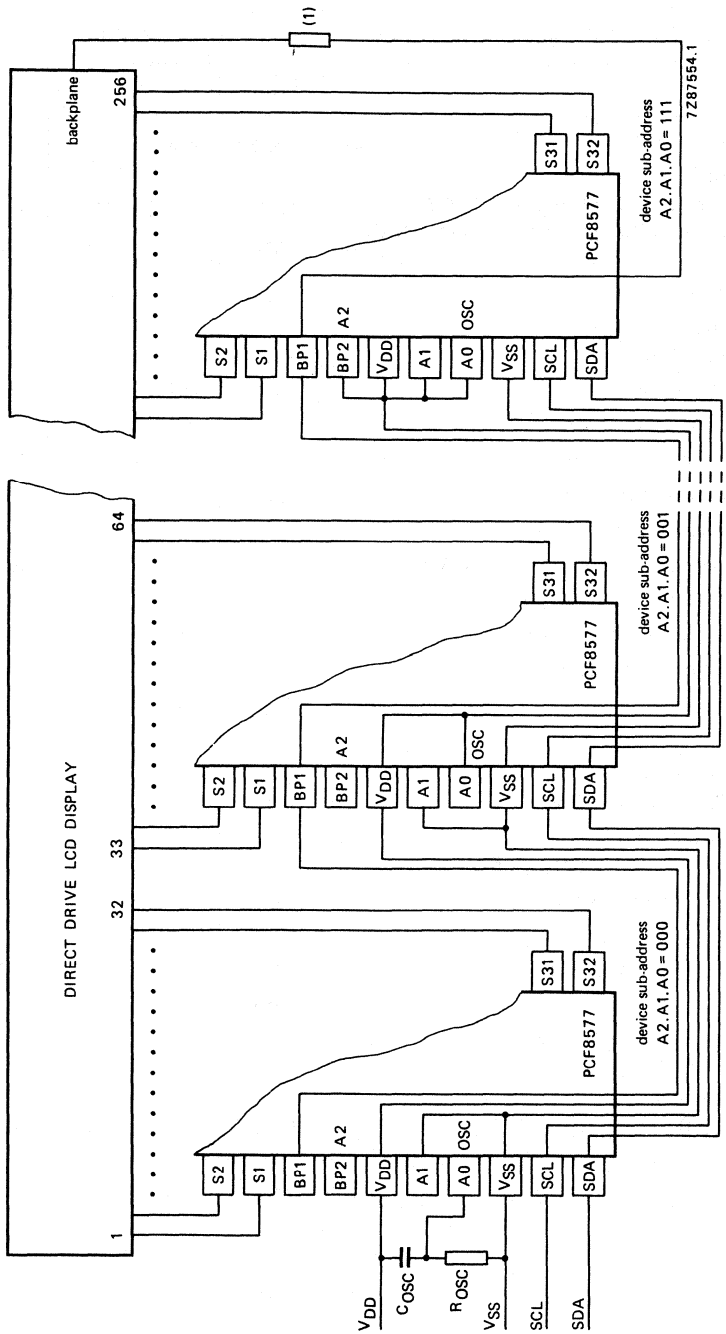
CHARACTERISTICS

V_{DD} = 2,5 to 9 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.*	max.	unit
Supply voltage	V_{DD}	2,5	–	9,0	V
Supply current					
f_{SCL} = 100 kHz; no load; R_{OSC} = 1 MΩ	I_{DD}	–	80	250	μA
f_{SCL} = 0; no load; R_{OSC} = 1 MΩ; V_{DD} = 5 V; T_{amb} = 25 °C	I_{DD}	–	35	50	μA
Power-on-reset level**	V_{REF}	–	1,1	2,0	V
Input SCL; input/output SDA					
input voltage LOW	V_{IL}	0	–	0,8	V
input voltage HIGH	V_{IH}	2,0	–	9,0	V
output current LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA
output leakage current HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
tolerable spike width on bus	t_{sw}	–	–	100	ns
input capacitance at $V_I = V_{SS}$	C_I	–	–	7	pF
A1 input leakage current at $V_I = V_{SS}$ or V_{DD}	I_I	–	–	250	nA
A2/BP2 input current at $V_I = V_{DD}$	I_I	–	2,0	–	μA
A0/OSC input current at $V_I = V_{SS}$ or V_{DD}	$\pm I_I$	–	5,0	–	μA
DC component of LCD driver	$\pm V_{BP}$	–	20	–	mV
Segment loads	C_{SX}	–	–	5	nF
	R_{SX}	1	–	–	MΩ
Segment output current at V_{OL} = 0,4 V; V_{DD} = 5 V	I_{OL}	0,3	–	–	mA
Segment output current at $V_{OH} = V_{DD} - 0,4$ V; V_{DD} = 5 V	$-I_{OH}$	0,3	–	–	mA
Backplane load (direct drive)	C_{BP}	–	–	50	nF
	R_{BP}	100	–	–	kΩ
Backplane loads (duplex drive)	C_{BP}	–	–	35	nF
	R_{BP}	100	–	–	kΩ
Rise and fall times ($V_{BP} - V_{SX}$) at maximum load	t_r, t_f	–	–	200	μs
Display frequency at C_{OSC} = 680 pF; R_{OSC} = 1 MΩ	f_{LCD}	65	90	120	Hz

* V_{DD} = 5 V; T_{amb} = 25 °C.

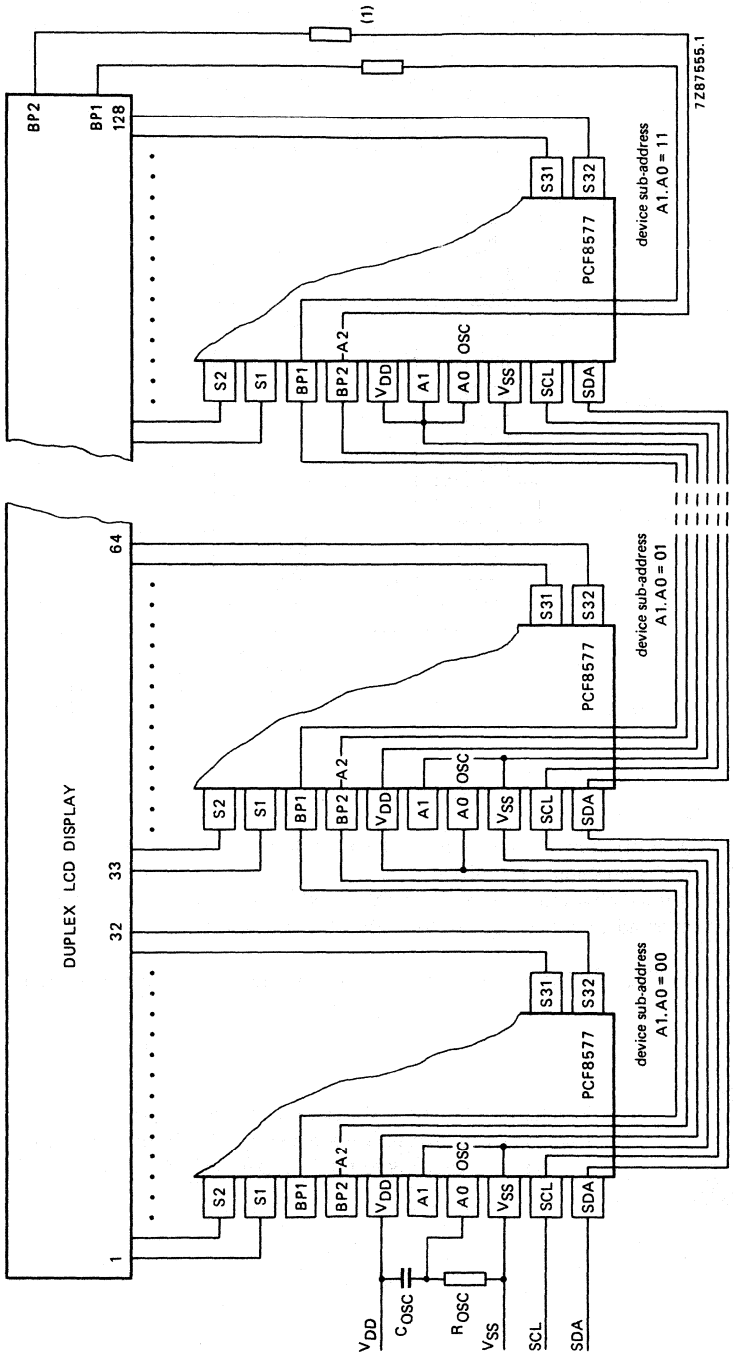
** The power-on-reset circuit resets the I²C bus logic with $V_{DD} < V_{REF}$.



(1) The series resistance of the display backplane must be greater than 1 Ω.

Fig. 16 Direct drive display; expansion to 256 segments using eight PCF8577.

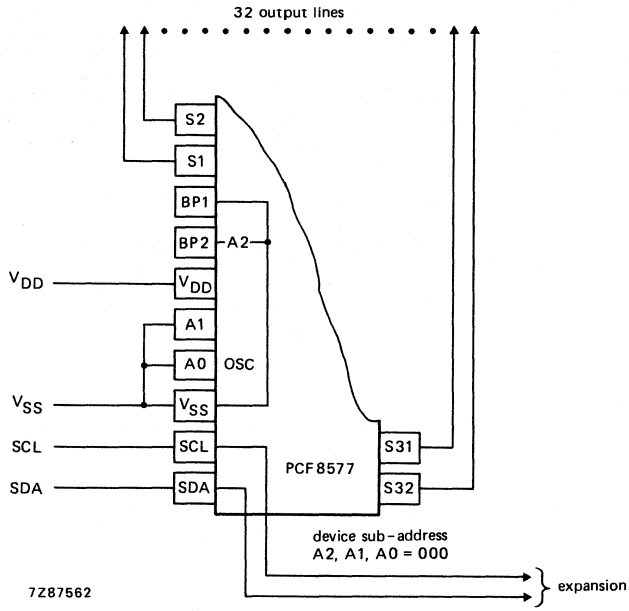
DEVELOPMENT DATA



(1) The series resistances of the display backplanes must be greater than 1 kΩ.

Fig. 17 Duplex display; expansion to 2 x 128 segments using four PCF8577.

APPLICATION INFORMATION (continued)



Notes

1. MODE bit must always be set to 0 (direct drive)
2. BANK switching is permitted
3. BP1 must always be connected to V_{SS} and A0/OSC must be connected to either V_{DD} or V_{SS} (no LCD modulation)

Fig. 18 Use of PCF8577 as 32-bit output expander in I²C bus application.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

LCD ROW/COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or, for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots.
The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (possible 40,960 dots)
- 40 driver outputs, configurable as 32/8, 24/16, 16/24 or 8/32 rows/columns
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8578T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8578U: uncased chip-in-tray.

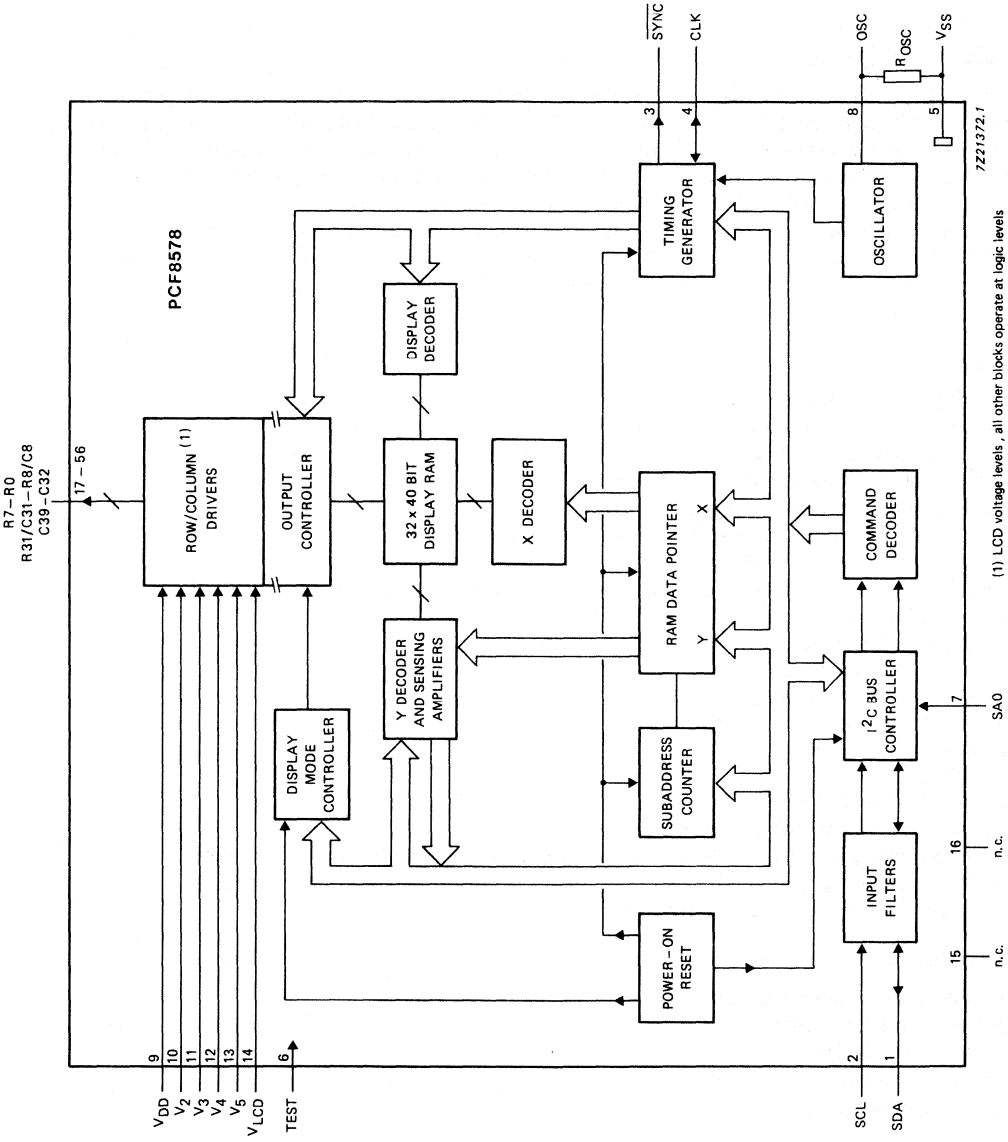


Fig. 1 Block diagram.

DEVELOPMENT DATA

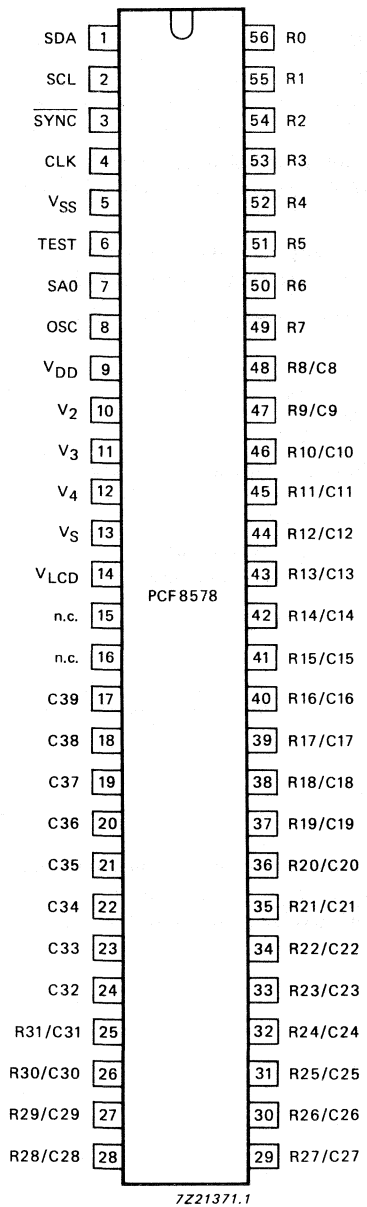


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output	I^2C bus
2	SCL	Clock input	I^2C bus
3	$\overline{SYNC}$	Cascade synchronization output	
4	CLK	External clock input/output	
5	V_{SS}	Ground (logic)	
6	TEST	Test pin (connect to V_{SS})	
7	SA0	I^2C bus slave address input (bit 0)	
8	OSC	Oscillator input	
9	V_{DD}	Positive supply voltage	
10	V_2	LCD bias voltage inputs	
11	V_3	LCD bias voltage inputs	
12	V_4	LCD bias voltage inputs	
13	V_5	LCD bias voltage inputs	
14	V_{LCD}	LCD supply voltage	
15	n.c.	Not connected	
16	n.c.	Not connected	
17 to 24	C39 to C32	LCD column driver outputs	
25 to 48	R31/C31 to R8/C8	LCD row/column driver outputs	
49 to 56	R7 to R0	LCD row driver outputs	

FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (row mode)

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications or for larger displays with up to 15 PCF8579s (31 when two slave addresses are used). See Table 1 for common display configurations.

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Table 1 Common display configurations

application	multiplex rate	mixed mode		row mode		typical applications
		rows	columns	rows	columns	
stand-alone	1 : 8	8	32	–	–	small digital or alphanumeric displays
	1 : 16	16	24	–	–	
	1 : 24	24	16	–	–	
	1 : 32	32	8	–	–	
with PCF8579	1 : 8	8	632	8 x 4	640	alphanumeric displays and dot matrix graphic displays
	1 : 16	16	624	16 x 2	640	
	1 : 24	24	616	24	640	
	1 : 32	32	608	32	640	
		using 15 PCF8579s		using 16 PCF8579s		

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays bias sources with high driver capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig. 3 (a stand-alone system would be identical but without PCF8579).

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leqslant 9$	$n \geqslant 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

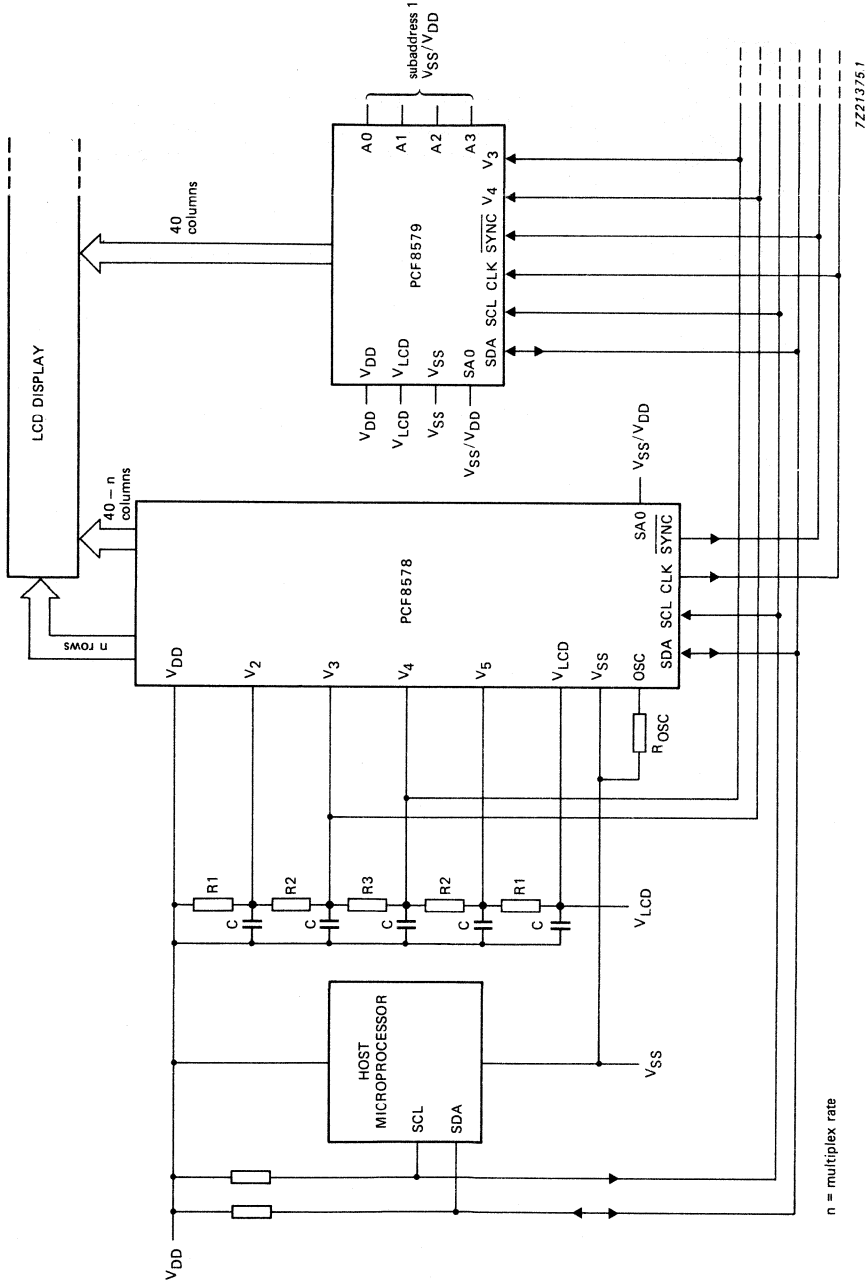


Fig. 3 Typical mixed mode configuration.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

LCD COLUMN DRIVER FOR DOT MATRIX GRAPHIC DISPLAYS

GENERAL DESCRIPTION

The PCF8579 is a low power CMOS LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs and can drive 32 x 40 dots in a 32 row multiplexed LCD. The device is optimized for use with the PCF8578 LCD row/column driver. Up to 32 PCF8579s can be cascaded and used on the same I^2C bus (using the two slave addresses). Together these two devices form a general LCD dot matrix driver chip set, capable of driving displays of up to 40,960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40,960 dots
- 40 column outputs
- Selectable row multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries
- Power-on reset blanks display
- Logic voltage supply range 2,5 V to 6,0 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications
- Space saving 56-lead plastic mini-pack
- Compatible with chip-on-glass technology

APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation

PACKAGE OUTLINES

PCF8579T: 56-lead mini-pack; plastic (VSO56; SOT190).
PCF8579U: uncased chip-in-tray.

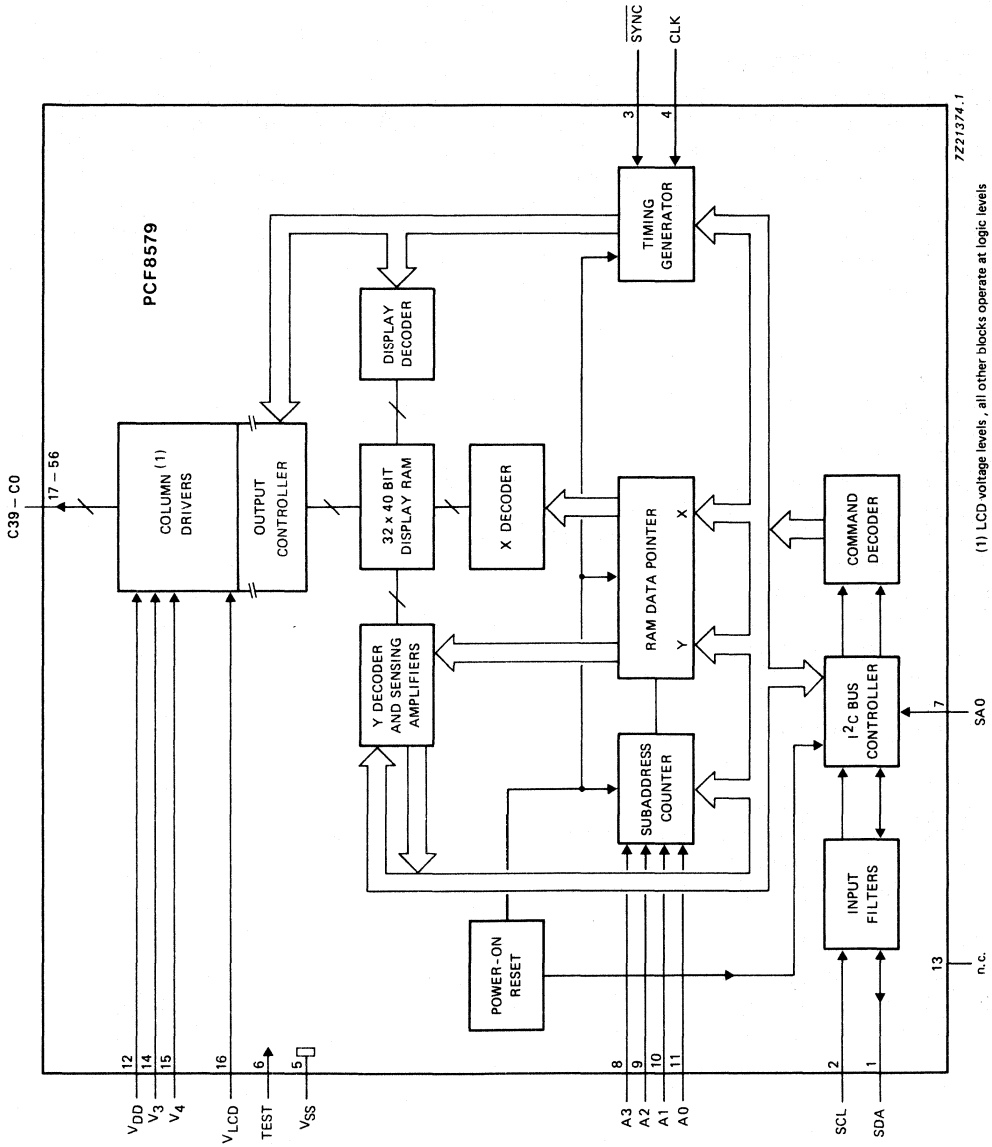


Fig. 1 Block diagram.

DEVELOPMENT DATA

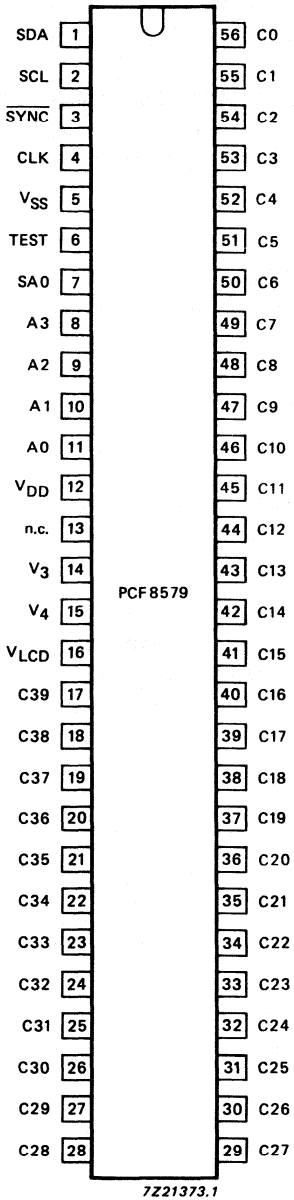


Fig. 2 Pinning diagram.

PINNING

1	SDA	Data input/output	I²C bus
2	SCL	Clock input	I²C bus
3	$\overline{SYNC}$	Cascade synchronization input	
4	CLK	External clock input	
5	V_{SS}	Ground (logic)	
6	TEST	Test pin (connect to V_{SS})	
7	SA0	I²C bus slave address input (bit 0)	
8	A3	I²C bus subaddress inputs	
9	A2	I²C bus subaddress inputs	
10	A1	I²C bus subaddress inputs	
11	A0	I²C bus subaddress inputs	
12	V_{DD}	Positive supply voltage	
13	n.c.	Not connected	
14	V_3	LCD bias voltage inputs	
15	V_4	LCD bias voltage inputs	
16	V_{LCD}	LCD supply voltage	
17 to 56	C39 to C0	LCD column driver outputs	

FUNCTIONAL DESCRIPTION

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

The PCF8578 typically operates with up to 16 PCF8579s. Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s. This is achieved by setting the LSB of the I^2C bus slave address to 1 (V_{DD}) or 0 (V_{SS}) using input SA0.

Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. 1 : 32 multiplex rate
2. Display bank 0
3. Data pointer is set to X, Y address 0
4. Character mode
5. Subaddress counter is cleared
6. I^2C bus interface is initialized
7. Display blanked (by PCF8578)

Data transfers on the I^2C bus should be avoided for 1 ms following power-on to allow completion of the reset action.

Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the threshold voltage (V_{th}). V_{th} is typically defined as the r.m.s. voltage at which the LCD exhibits 10% contrast. Table 1 shows the optimum voltage bias levels for the PCF8578/PCF8579 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}.

Table 1 Optimum LCD bias voltages

multiplex rate	$\frac{V_1}{V_{op}}$	$\frac{V_2}{V_{op}}$	$\frac{V_3}{V_{op}}$	$\frac{V_4}{V_{op}}$	$\frac{V_{off}}{V_{op}}$	$\frac{V_{on}}{V_{op}}$	$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	$\frac{V_{op}}{V_{th}}$
1 : 8	0,739	0,522	0,478	0,261	0,297	0,430	1,477	3,37
1 : 16	0,800	0,600	0,400	0,200	0,245	0,316	1,291	4,08
1 : 24	0,830	0,661	0,339	0,170	0,214	0,263	1,230	4,68
1 : 32	0,850	0,700	0,300	0,150	0,193	0,230	1,196	5,19

Table 2 Multiplex rates (see Fig. 3)

resistor	multiplex rate (n)	
	$n \leqslant 9$	$n \geqslant 9$
R1	R	R
R2	$(\sqrt{n}-2)$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n}-3)$ R

DEVELOPMENT DATA

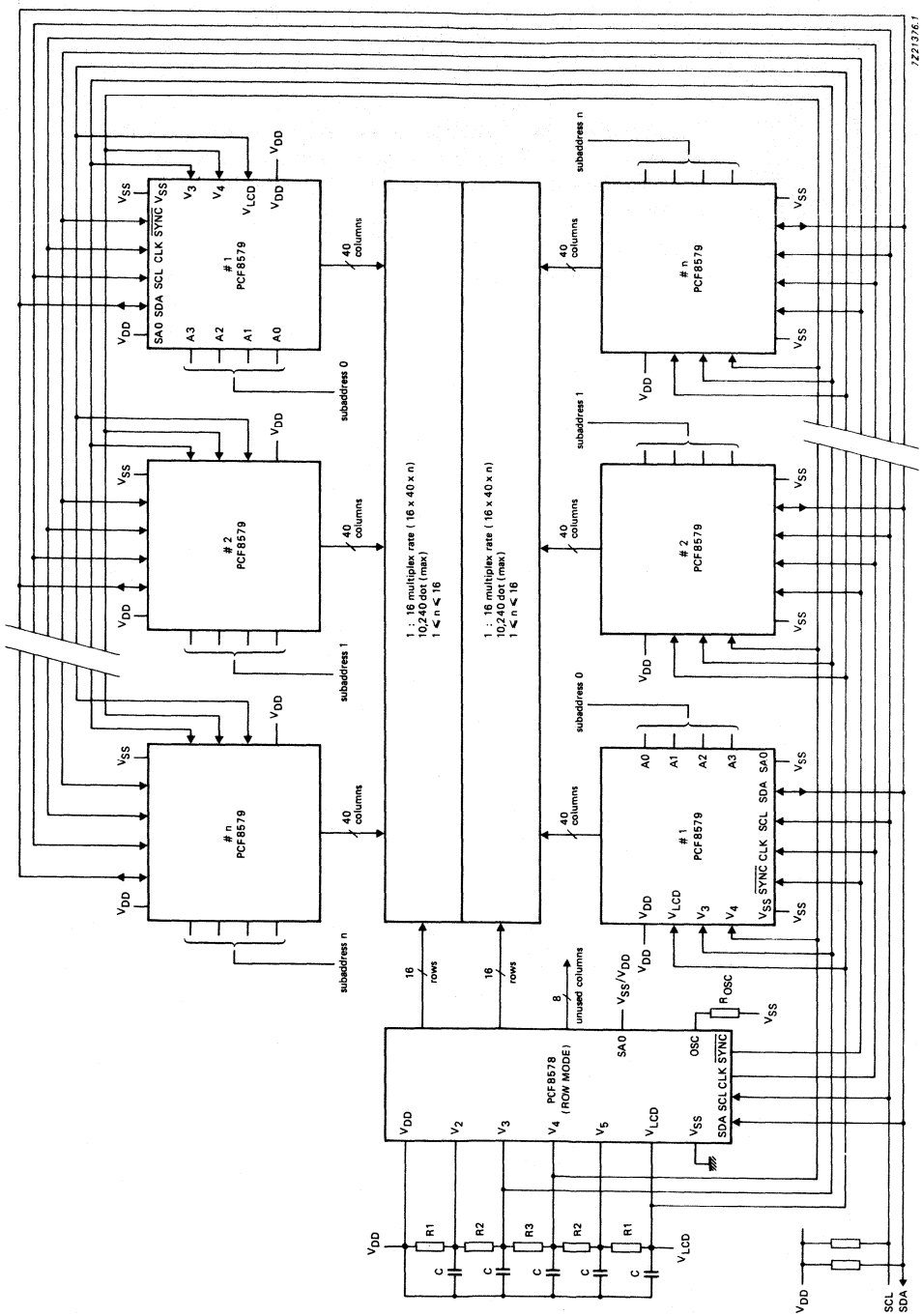


Fig. 3 Example of split screen application with 1 : 16 multiplex rate for improved contrast.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

256 × 8-bit STATIC CMOS EEPROM WITH I²C-BUS INTERFACE

GENERAL DESCRIPTION

The PCF8582A is a 2 Kbits 5 Volt electrically erasable programmable read only memory (EEPROM) organized as 256 by 8-bits. It is designed in a floating gate CMOS technology.

As data bytes are received and transmitted via the serial I²C-bus, an eight pin DIL package is sufficient. Up to eight PCF8582A devices may be connected to the I²C-bus.

Chip select is accomplished by three address inputs.

Timing of the Erase/Write cycle can be done in two different ways; either by connecting an external clock to the "Programming Timing Control", pin (7 or 13), or by using an internal oscillator. If the latter is used an RC time constant must be connected to pin 7 or 13.

FEATURES

- Non-volatile storage of 2 Kbits organized as 256 x 8
- Only one power supply required (5 V)
- On chip voltage multiplier for erase/write
- Serial input/output bus (I²C)
- Automatic word address incrementing
- Low power consumption
- One point erase/write timer
- power on reset
- 10,000 erase/write cycles per byte
- 10 years non-volatile data retention
- Infinite number of read cycles
- Pin and address compatible to PCF8570, PCF8571, PCF8582 and PCD8572
- External clock signal possible.

PACKAGE OUTLINE

PCF8582AP; 8-lead dual in line; plastic (SOT97).
PCF8582AT; 16-lead mini-pack; plastic (SO16L; SOT162A).

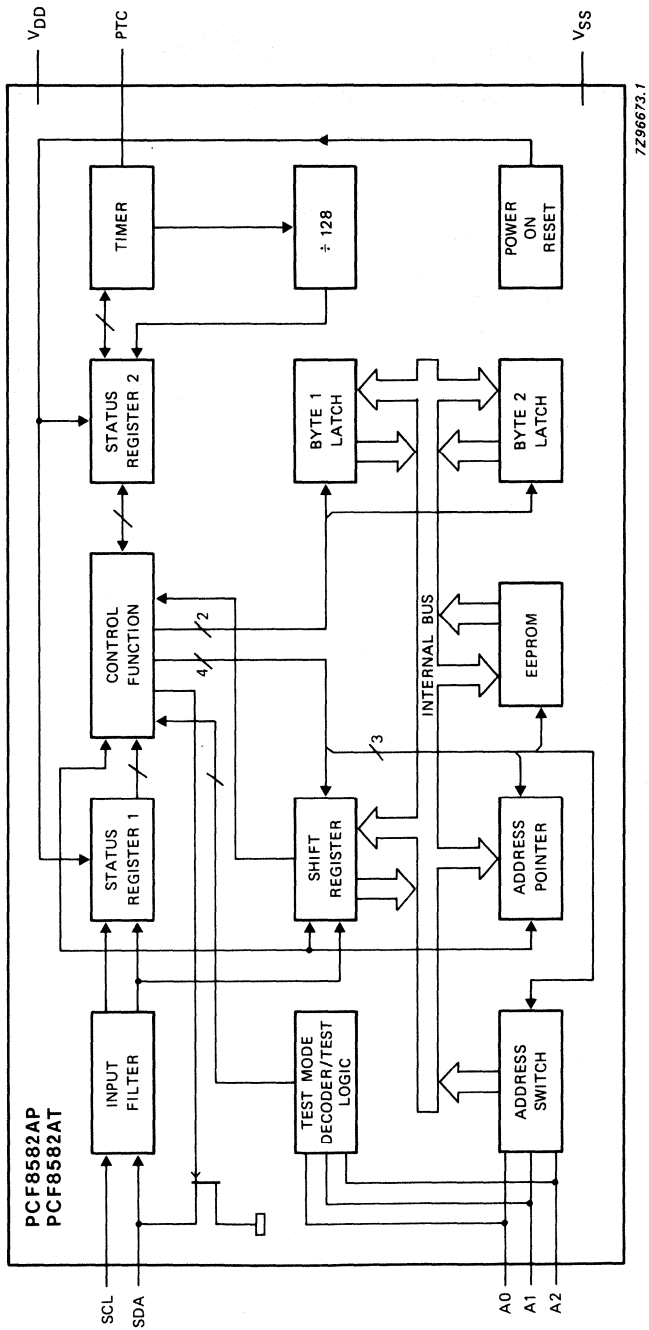
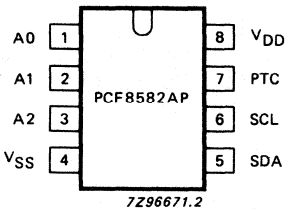
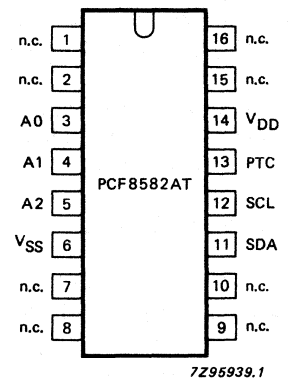


Fig. 1 Block diagram.



1	A0	address inputs/test mode select
2	A1	
3	A2	
4	V_{SS}	ground
5	SDA	I^2C-bus lines
6	SCL	
7	PTC	programming time control
8	V_{DD}	positive supply

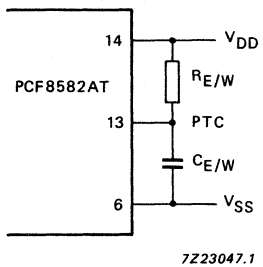
Fig. 2 (a) Pinning diagram.

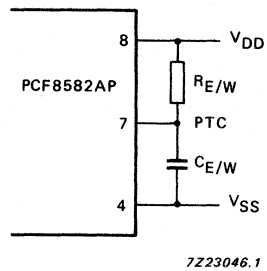


1	n.c.	
2	n.c.	
3	A0	address inputs/test mode select
4	A1	
5	A2	
6	V_{SS}	ground
7	n.c.	
8	n.c.	
9	n.c.	
10	n.c.	
11	SDA	I^2C-bus lines
12	SCL	
13	PTC	programming time control
14	V_{DD}	positive supply
15	n.c.	
16	n.c.	

Fig. 2 (b) Pinning diagram.

DEVELOPMENT DATA





Figs. 3 (a) and (b) RC circuit connections to PCF8582AP and PCF8582AT when using the internal oscillator

FUNCTIONAL DESCRIPTION

Characteristics of the I²C-bus

The I²C-bus is intended for communication between different ICs. The serial bus consists of two bi-directional lines, one for data signals (SDA), and one for clock signals (SCL). Both the SDA and the SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

Data transfer may be initiated only when the bus is not busy.
During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

The following bus conditions have been defined:

Bus not busy; both data and clock lines remain HIGH.
Start data transfer; a change in the state of the data line, from HIGH to LOW, while the clock is HIGH defines the start condition. Stop data transfer; a change in the state of the data line, from LOW to HIGH, while the clock is HIGH, defines the stop condition.
Data valid; the state of the data line represents valid data when, after a start condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition; the number of the data bytes, transferred between the start and stop conditions is limited to two bytes in the ERASE/WRITE mode and unlimited in the READ mode. The information is transmitted in bytes and each receiver acknowledges with a ninth bit.

Within the I²C-bus specifications a low speed mode (2 kHz clock rate) and a high speed mode (100 kHz clock rate) are defined. The PCF8582A operates in both modes.

By definition a device that sends a signal is called a "transmitter", and the device which receives the signal is called a "receiver". The device which controls the signal is called the "master". The devices that are controlled by the master are called "slaves".

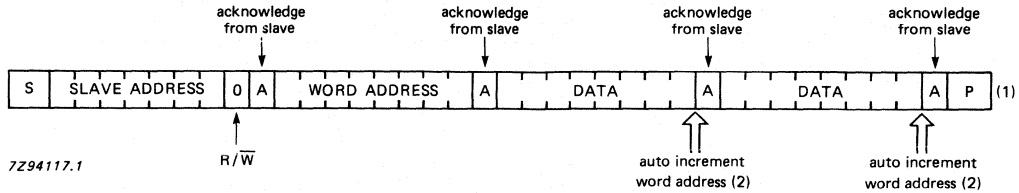
Each word of eight bits is followed by one acknowledge bit. This acknowledge bit is a HIGH level put on the bus by the transmitter. The master generates an extra acknowledge related clock pulse.
The slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte.
The master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse in clock pulse.
Set-up and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this condition the transmitter must leave the data line HIGH to enable the master generation of the stop condition.

Note

Detailed specifications of the I²C-bus are available on request.

I²C-Bus Protocol

The I²C-bus configurations for different READ and WRITE cycles of the PCF8582A are shown in Fig. 4, (a), (b) and (c).



(1) After this stop condition the erase/write cycle starts and the bus is free for another transmission. The duration of the erase/write cycle is approximately 30 ms if only one byte is written and 60 ms if two bytes are written. During the erase/write cycle the slave receiver does not send an acknowledge bit if addressed via the I²C-bus.

(2) The second data byte is voluntary. It is not allowed to erase/write more than two types.

Fig. 4(a) Master transmitter transmits to PCF8582A slave receiver (ERASE/WRITE mode).

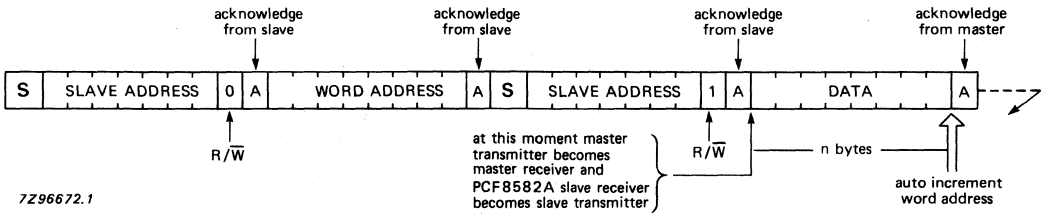
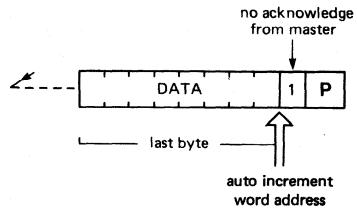


Fig. 4(b) Master reads PCF8582A slave after setting word address (write word address; READ data).



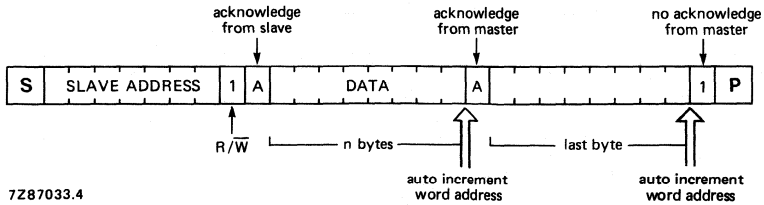


Fig. 4(c) Master reads PCF8582A slave immediately after first byte (READ mode).*

Note: the slave address is defined in accordance with the I²C-bus specification as:

1	0	1	0	A2	A1	A0	R/$\overline{W}$

* The device can be used as read only without the programming clock.

DEVELOPMENT DATA

I²C-bus timing

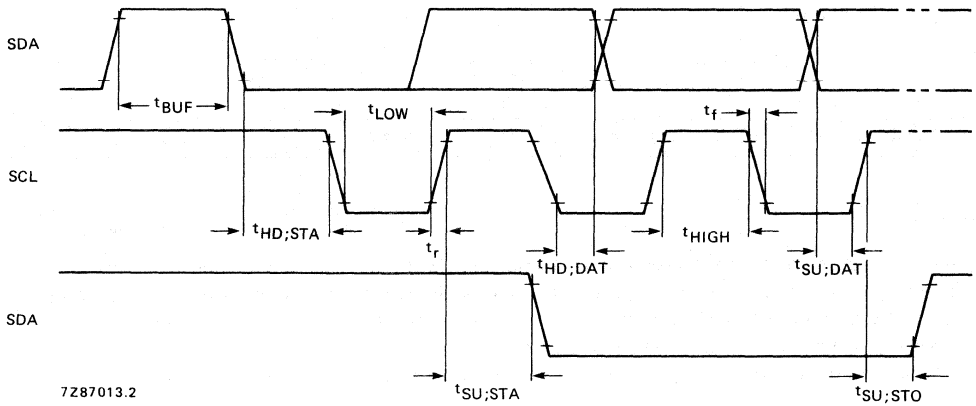
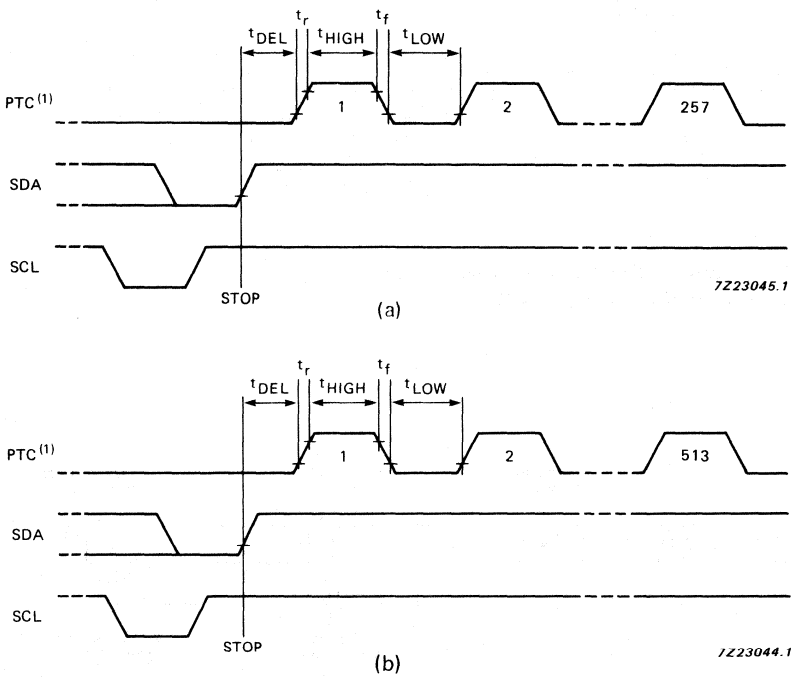


Fig. 5 I²C-bus timing.



(1) If external clock for PTC is chosen, this information is latched internally by leaving pin 7 LOW after transmission of the eight bit of the word address (negative edge of SCL). The state of PTC then, may be previously undefined.

Fig. 6 (a) One-byte ERASE/WRITE cycle; (b) two-byte ERASE/WRITE cycle.

Ratings

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_{DD}	−0.3	+7	V
Voltage on any input pin input impedance 500 Ω	V_I	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
Operating temperature range	T_{amb}	−40	+85	°C
Storage temperature range	T_{stg}	−65	+150	°C
Current into any input pin	$\|I_I\|$	–	1	mA
Output current	$\|I_O\|$	–	10	mA

DEVELOPMENT DATA

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

CHARACTERISTICS

V_{DD} = 5 V; V_{SS} = 0 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Operating supply voltage		V_{DD}	4.5	5.0	5.5	V
Operating supply current READ	V_{DD} max. f_{SCL} = 100 kHz	I_{DD}	–	–	0.4	mA
Operating supply current WRITE/ERASE	V_{DD} max.	I_{DDW}	–	–	2.0	mA
Standby supply current	V_{DD} max.	I_{DDO}	–	–	10	μA
Input PTC						
Input voltage HIGH			V_{DD} − 0.3	–	–	V
Input voltage LOW			–	–	V_{SS} + 0.3	V
Input SCL and input/output SDA						
Input voltage LOW		V_{IL}	−0.3	–	1.5	V
Input voltage HIGH		V_{IH}	3.0	–	V_{DD} + 0.8	V
Output voltage LOW	I_{OL} = 3 mA V_{DD} = 4.5 V	V_{OL}	–	–	0.4	V
Output leakage current HIGH	$V_{OH} = V_{DD}$	I_{LO}	–	–	1	μA
Input leakage current (SCL)	$V_I = V_{DD}$ or V_{SS}	I_{LI}	–	–	1	μA
Clock frequency		f_{SCL}	0	–	100	kHz
Input capacitance (SCL; SDA)		C_I	–	–	7	pF
Time the bus must be free before new transmission can start		t_{BUF}	4.7	–	–	μs
Start condition hold time after which first clock pulse is generated		$T_{HD;STA}$	4	–	–	μs

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
The LOW period of the clock		t_{LOW}	4.7	–	–	μs
The HIGH period of the clock		t_{HIGH}	4.0	–	–	μs
Set-up time for start condition	repeated start only	$t_{SU;STA}$	4.7	–	–	μs
Data hold time for I²C bus compatible masters		$t_{HD;DAT}$	5.0	–	–	μs
Data hold time for I²C devices	note 1.	$t_{HD;DAT}$	0	–	–	ns
Date set up time		$t_{SU;DAT}$	250	–	–	ns
Rise time for SDA and SCL lines		t_r	–	–	1	μs
Fall time for SDA and SCL lines		t_f	–	–	300	ns
Set-up time for stop condition		$T_{SU;STO}$	4.7	–	–	μs
Programming time control						
Erase/write cycle time		$t_{E/W}$	20	–	100	ms
Capacitor used for E/W cycle of 30 ms	max. tolerance ±10%; using internal oscillator (Fig. 3)	$C_{E/W}$	–	3.3	–	nF
Resistor used for E/W cycle of 30 ms	max. tolerance ±5%; using internal oscillator (Fig. 3)	$R_{E/W}$	–	56.0	–	kΩ
Programming frequency using external clock						
Frequency		f_p	2.57	–	12.85	kHz
Period LOW		t_{LOW}	10.0	–	–	μs
Period HIGH		t_{HIGH}	10.0	–	–	μs
Rise-time		t_r	–	–	300	ns
Fall-time		t_f	–	–	300	ns
Delay-time		t_d	0	–		ns
Data retention time	T_{amb} = 55 °C	t_S	10	–	–	years

Note to the characteristics

1. The hold time required to bridge the undefined region of the falling edge of SCL must be internally provided by a transmitter. It is not greater than 300 ns.

CLOCK CALENDAR WITH 256 × 8-BIT STATIC RAM

GENERAL DESCRIPTION

The PCF8583 is a low power 2048-bit static CMOS RAM organized as 256 words by 8-bits. Addresses and data are transferred serially via a two-line bidirectional bus (I^2C). The built-in word address register is incremented automatically after each written or read data byte. One address pin A0 is used for programming the hardware address, allowing the connection of two devices to the bus without additional hardware. The built-in 32,768 kHz oscillator circuit and the first 8 bytes of the RAM are used for the clock/calendar and counter functions. The next 8 bytes may be programmed as alarm registers or used as free RAM space.

Features

- I^2C bus interface operating supply voltage: 2,5 V to 6 V
- Clock operating supply voltage (0 to 70 °C): 1,0 V to 6 V
- Data retention voltage: 1,0 V to 6 V
- Operating current (f_{SCL} = 0 Hz): max. 50 μA
- Clock function with four year calendar
- 24 or 12 hour format
- 32,768 kHz or 50 Hz time base
- Serial input/output bus (I^2C)
- Automatic word address incrementing
- Programmable alarm, timer and interrupt function

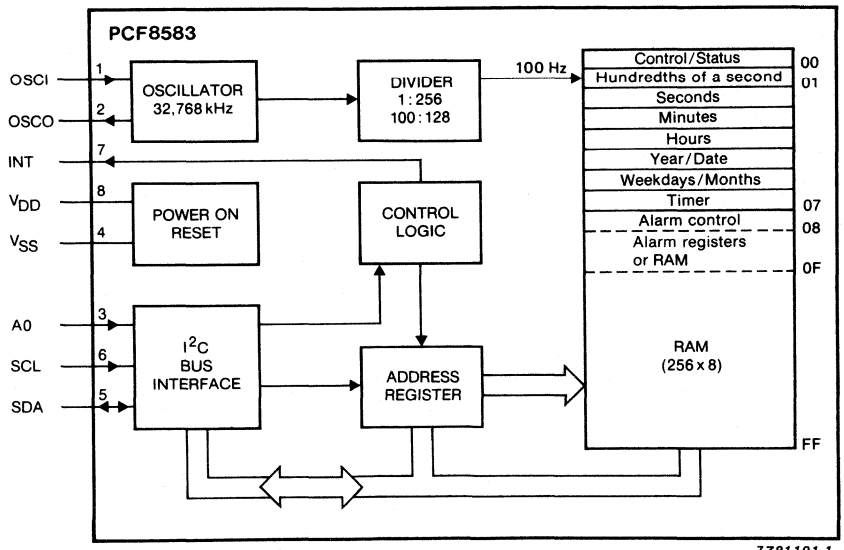


Fig. 1 Block diagram.

PACKAGE OUTLINES

PCF8583P: 8-lead DIL; plastic (SOT97).
PCF8583T: 8-lead mini-pack; plastic (SO8L; SOT176).

PINNING

1	OSCI	oscillator input, 50 Hz or event-pulse input	
2	OSCO	oscillator output	
3	A0	address input	
4	V_{SS}	negative supply	
5	SDA	serial data line	I^2C bus
6	SCL	serial clock line	I^2C bus
7	INT	open drain interrupt output (active low)	
8	V_{DD}	positive supply	

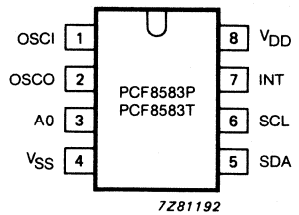


Fig. 2 Pinning diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range (pin 8); note 1	V_{DD}		−0,8 to 8,0	V
Voltage range on any input	V_I		−0,8 to V_{DD} + 0,8	V
DC input current (any input)	I_I	max.	10	mA
DC output current (any output)	I_O	max.	10	mA
Supply current (pin 4 or pin 8)	I_{DD}; I_{SS}	max.	50	mA
Power dissipation per package	P_{tot}	max.	300	mW
Power dissipation per output	P	max.	50	mW
Storage temperature range	T_{stg}		−65 to + 150	°C
Operating ambient temperature range	T_{amb}		−40 to + 85	°C

Note

1. Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

FUNCTIONAL DESCRIPTION

The PCF8583 contains a 256 by 8-bit RAM with an 8-bit auto-increment address register, an on-chip 32,768 kHz oscillator circuit, a frequency divider, a serial two-line bidirectional I^2C bus interface and a power-on reset circuit.

The first 8 bytes of the RAM (memory addresses 00 to 07) are designed as addressable 8-bit parallel registers. The first register (memory address 00) is used as a control/status register. The memory addresses 01 to 07 are used as counters for the clock function. The memory addresses 08 to 0F are free RAM locations or may be programmed as alarm registers.

Counter function modes

When the control/status register is set a 32,768 kHz clock mode, a 50 Hz clock mode or an event-counter mode can be selected.

In the clock modes the hundredths of a second, seconds, minutes, hours, date, month (four year calendar) and weekdays are stored in a BCD format. The timer register stores up to 99 days. The event-counter mode is used to count pulses applied to the oscillator input (OSCO left open). The event counter stores up to 6 digits of data.

When one of the counters is read (memory locations 01 to 07), the contents of all counters are strobed into capture latches at the beginning of a read cycle. Therefore faulty reading of the count during a carry condition is prevented.

DEVELOPMENT DATA

Alarm function modes

By setting the alarm enable bit of the control/status register the alarm control register (address 08) is activated.

By setting the alarm control register a dated alarm, a daily alarm, a weekday alarm or a timer alarm may be programmed. In the clock modes, the timer register (address 07) may be programmed to count hundredths of a second, seconds, minutes, hours or days. Days are counted when an alarm is not programmed.

Whenever an alarm event occurs the alarm flag of the control/status register is set. A timer alarm event will set the alarm flag and an overflow condition of the timer will set the timer flag. The open drain interrupt output is switched on (active LOW) when the alarm or timer flag is set (enabled).

When a timer function without any alarm function is programmed the remaining alarm registers (addresses 09 to 0F) may be used as free RAM space.

Control/status register

The control/status register is defined as the memory location 00 with free access for reading and writing via the I^2C bus. All functions and options are controlled by the contents of the control/status register (see Fig. 3).

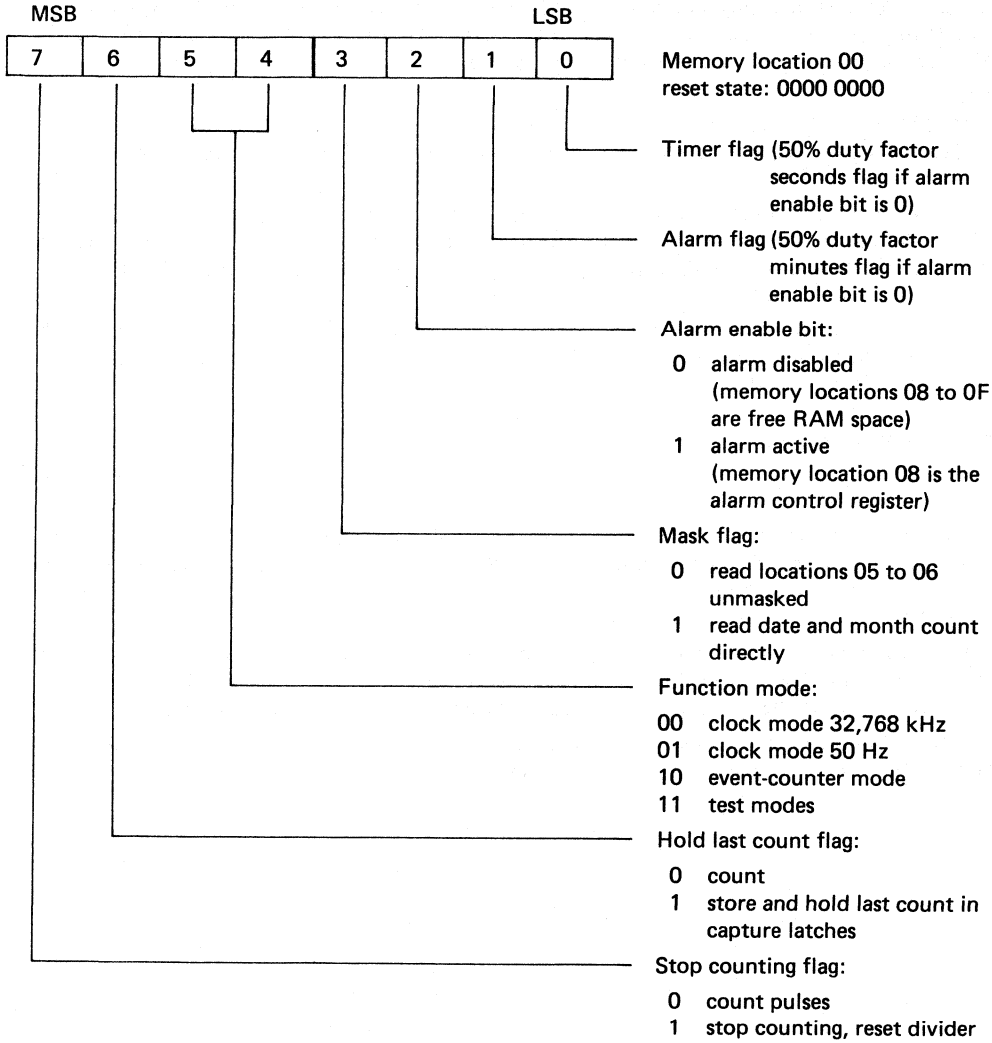


Fig. 3 Control/status register.

DEVELOPMENT DATA

Counter registers

In the different modes the counter registers are programmed and arranged as shown in Fig. 4. Counter cycles are listed in Table 1.

In the clock modes 24 h or 12 h format can be selected by setting the most significant bit of the hours counter register. The format of the hours counter is shown in Fig. 5.

The year and date are packed into memory location 05 (see Fig. 6). The weekdays and months are packed into memory location 06 (see Fig. 7). When reading these memory locations the year and weekdays are masked out when the mask flag of the control/status register is set. This allows the user to read the date and month count directly.

In the event-counter mode events are stored in BCD format. D5 is the most significant and D0 the least significant digit. The divider is by-passed.

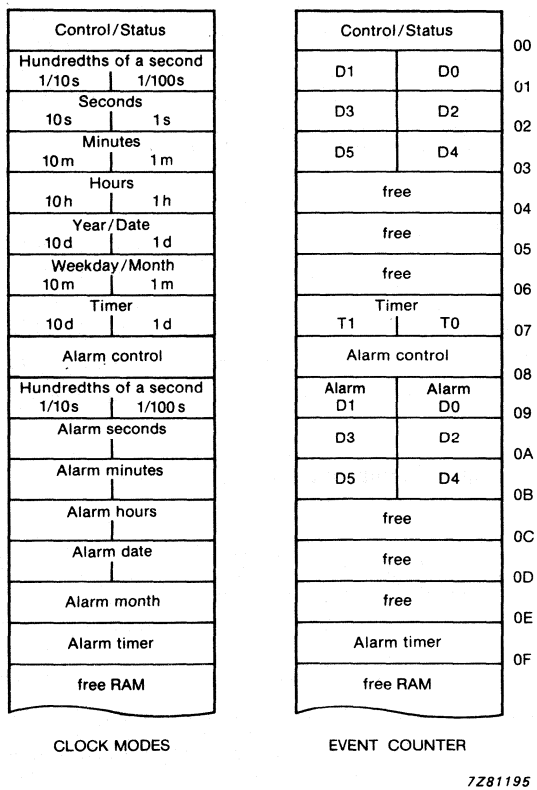
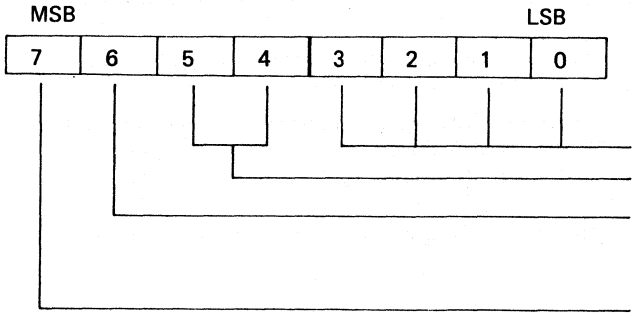


Fig. 4 Register arrangement.

Counter registers (continued)



Memory location 04 (hours counter)
reset state: 0000 0000

Unit hours BCD

Ten hours (0 to 2 binary)

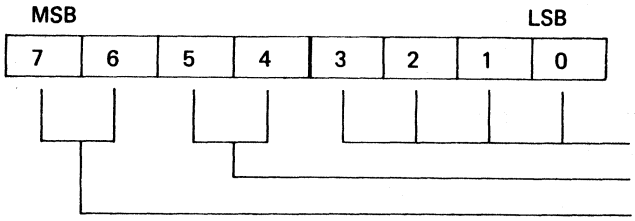
AM/PM flag:

0 AM
1 PM

Format:

0 24 h format, AM/PM flag remains unchanged
1 12 h format, AM/PM flag will be updated

Fig. 5 Format of the hours counter.



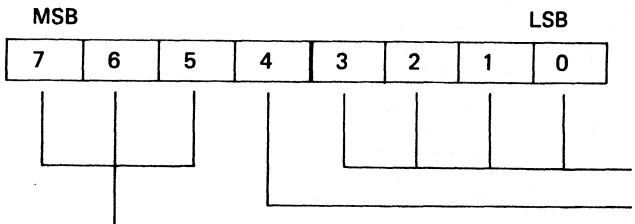
Memory location 05 (year/date)
reset state: 0000 0001

Unit days BCD

Ten days (0 to 3 binary)

Year (0 to 3 binary, read as 0 if the mask flag is set)

Fig. 6 Format of the year/date counter.



Memory location 06 (weekdays/months)
reset state: 0000 0001

Unit months BCD

Ten months

Weekdays (0 to 6 binary, read as 0 if the mask flag is set)

Fig. 7 Format of the weekdays/months counter.

Table 1 Cycle length of the time counters, clock modes

unit	counting cycle	carry to the next unit	contents of the month counter
hundredths of a second	00 to 99	99 to 00	
seconds	00 to 59	59 to 00	
minutes	00 to 59	59 to 00	
hours (24 h)	00 to 23	23 to 00	
hours (12 h)	12 AM, 01 AM to 11 AM, 12 PM, 01 PM to 11 PM	11 PM to 12 AM	
date	01 to 31	31 to 01	1, 3, 5, 7, 8, 10, 12
	01 to 30	30 to 01	4, 6, 9, 11
	01 to 29	29 to 01	2, year = 0
	01 to 28	28 to 01	2, year = 1, 2, 3
months	01 to 12	12 to 01	
year	0 to 3		
weekdays	0 to 6	6 to 0	
timer/days	00 to 99	no carry	

DEVELOPMENT DATA

Alarm control register

When the alarm enable bit of the control/status register is set the alarm control register (address 08) is activated. All alarm, timer and interrupt output functions are controlled by the contents of the alarm control register (see Figs 8a and 8b).

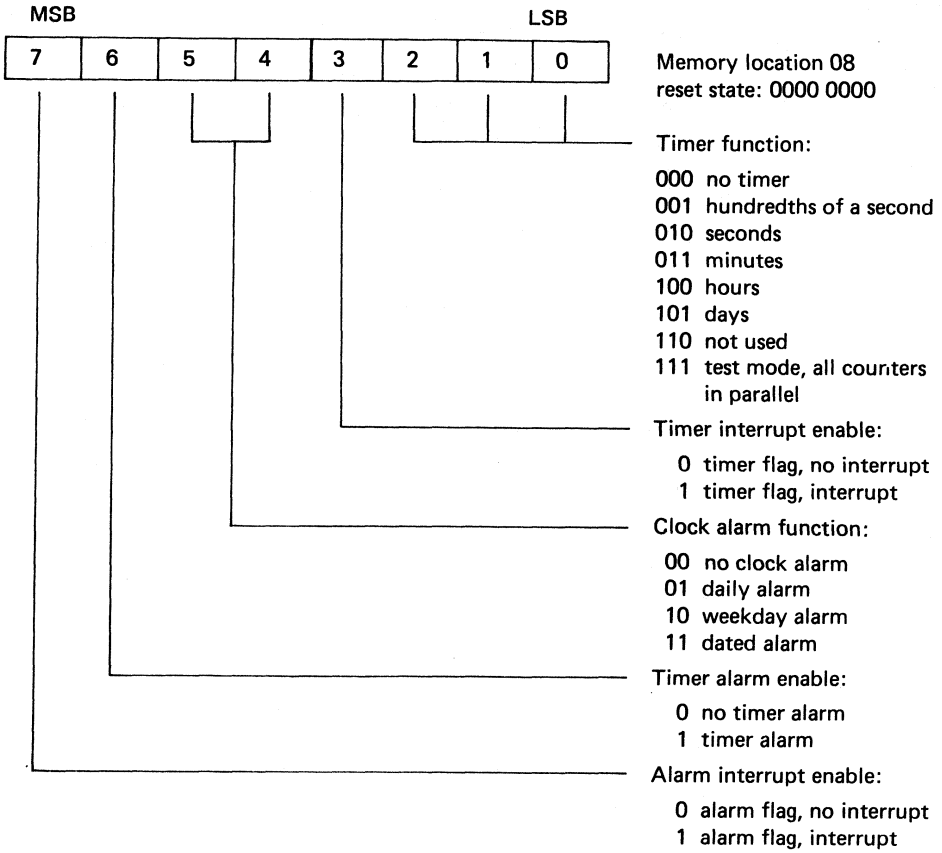
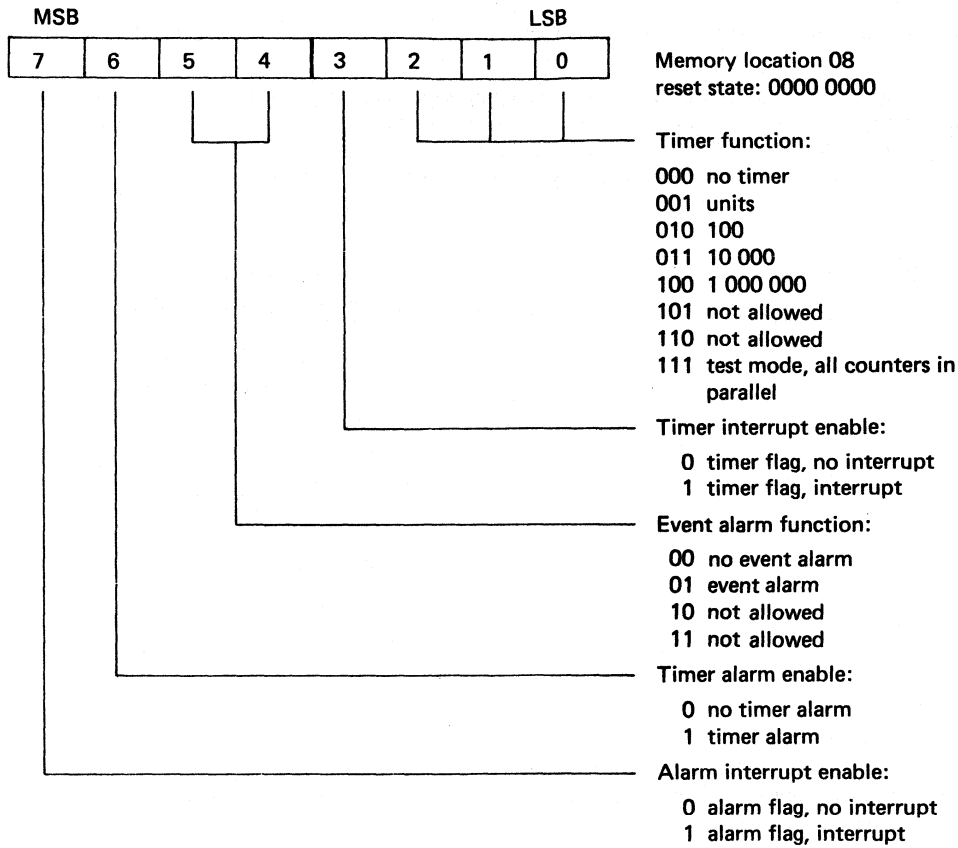


Fig. 8a Alarm control register, clock modes.



DEVELOPMENT DATA

Fig. 8b Alarm control register, event-counter mode.

Alarm registers

All alarm registers are allocated with a constant address offset of hex 08 to the corresponding counter registers.

An alarm goes off when the contents of the alarm registers matches bit-by-bit the contents of the involved counter registers. The year and weekday bits are ignored in a dated alarm. A daily alarm ignores the month and date bits. When a weekday alarm is selected, the contents of the alarm weekday/month register will select the weekdays on which an alarm is activated (see Fig. 9).

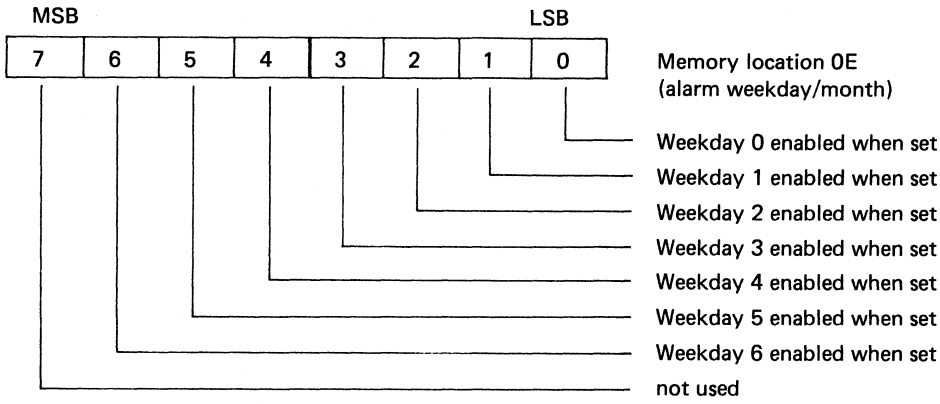


Fig. 9 Selection of alarm weekdays.

Interrupt output

The open-drain n-channel interrupt output is programmed by setting the alarm control register. It is switched on (active LOW) when the alarm flag or the timer flag is set. In the clock mode without alarm the output sequence is controlled by the timer flag. The OFF voltage of the interrupt output may exceed the supply voltage.

Oscillator and divider

A 32,768 kHz quartz crystal has to be connected to OSCI (pin 1) and OSCO (pin 2). A trimmer capacitor between OSCI and V_{DD} is used for tuning the oscillator. The oscillator frequency is scaled down to 128 Hz by the divider. A 100 Hz clock signal is derived from this signal.

In the 50 Hz clock mode or event-counter mode the oscillator is disabled and the oscillator input is switched to a high impedance state. This allows the user to feed the 50 Hz reference frequency or an external high speed event signal into the input OSCI.

Initialization

When power-up occurs the I^2C bus interface, the control/status register and all clock counters are reset. The device starts time keeping in the 32,768 kHz clock mode with the 24 h format on the first of January at 0.00.00: 00.

A second level-sensitive reset signal to the I^2C bus interface is generated as soon as the supply voltage drops below the interface reset level. This reset signal does not affect the control/status or clock counter registers.

It is recommended to set the stop counting flag of the control/status register before loading the actual time into the counters. Loading of illegal states will lead to a clock malfunction but will not latch-up the device.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

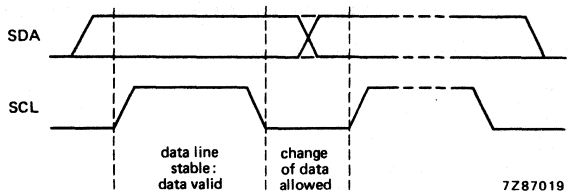


Fig. 10 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

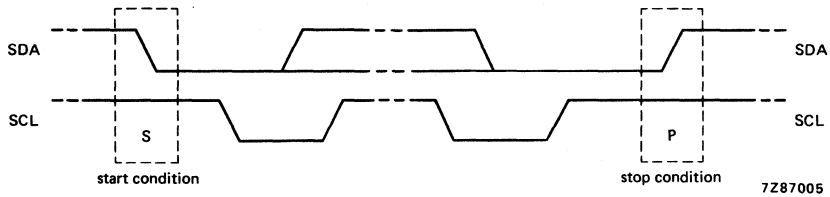


Fig. 11 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

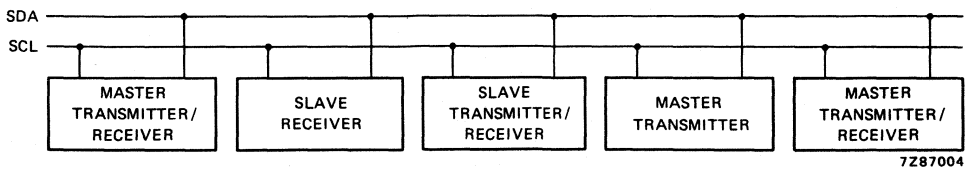


Fig. 12 System configuration.

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledge has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

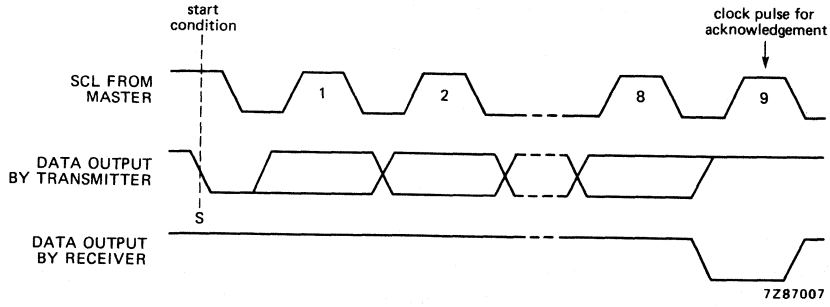


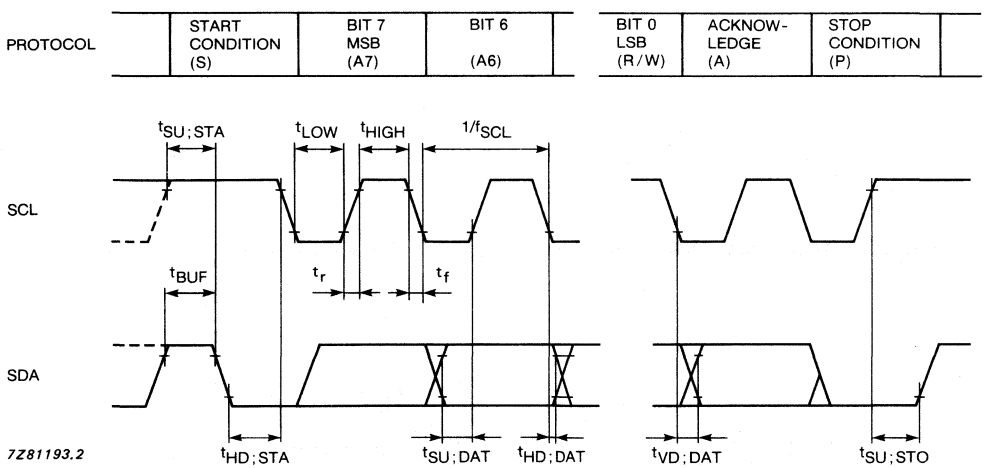
Fig. 13 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_r	–	–	1,0	μs
SCL and SDA fall time	t_f	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs



I²C bus protocol

Before any data is transmitted on the I²C bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The I²C bus configuration for the different PCF8583 READ and WRITE cycles is shown in Fig. 15.

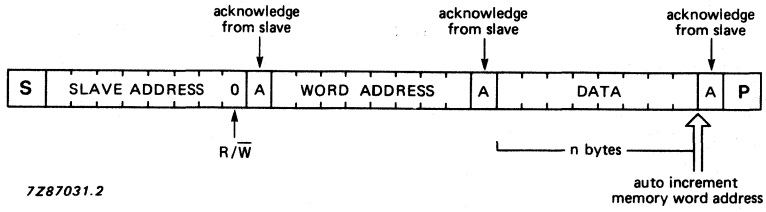


Fig. 15a Master transmits to slave receiver (WRITE mode).

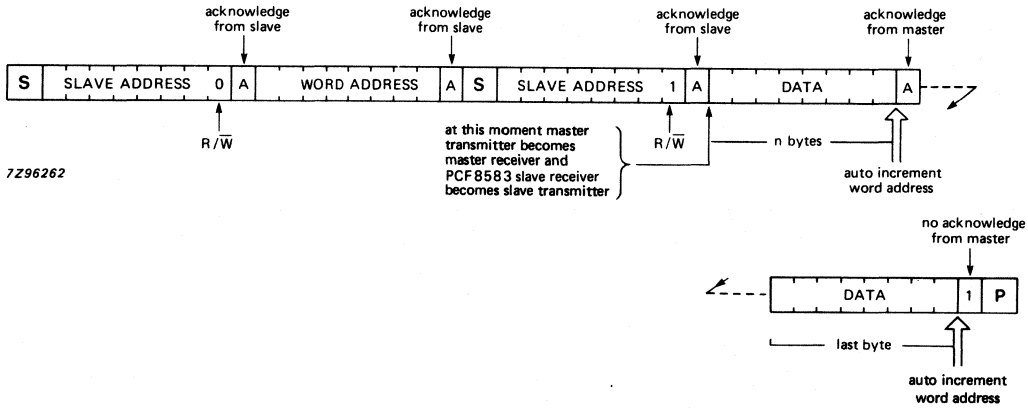


Fig. 15b Master reads after setting word address (WRITE word address; READ data).

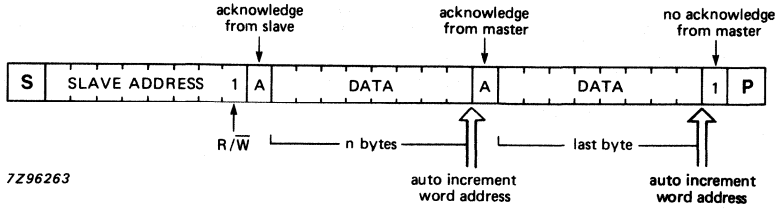


Fig. 15c Master reads slave immediately after first byte (READ mode).

DEVELOPMENT DATA

CHARACTERISTICS

V_{DD} = 2,0 to 6,0 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage (operating)	V_{DD}	2,5	–	6	V
Supply voltage (clock)	V_{DD}	1,0	–	6	V
Supply current T_{amb} = 0 to 70 °C operating at f_{SCL} = 100 kHz	I_{DD}	–	–	200	μA
Clock at V_{DD} = 5 V	I_{DDO}	–	10	50	μA
Clock at V_{DD} = 1 V	I_{DDO}	–	2	10	μA
Power-on reset voltage level (note 1)	V_{POR}	1,5	1,9	2,3	V
Inputs; input/output SDA					
Input voltage LOW (note 2)	V_{IL}	−0,8	–	0,3 x V_{DD}	V
Input voltage HIGH (note 2)	V_{IH}	0,7 x V_{DD}	–	V_{DD} + 0,8	V
Output current LOW at V_{OL} = 0,4 V	I_{OL}	3	–	–	mA
Output leakage current HIGH at V_{OH} = V_{DD}	I_{OH}	–	–	250	nA
Input leakage current at V_I = V_{DD} or V_{SS}	$\pm I_I$	–	–	250	nA
Input capacitance (SCL, SDA) at V_I = V_{SS}	C_I	–	–	7	pF
LOW V_{DD} data retention					
Supply voltage for data retention	V_{DDR}	1	–	6	V
Supply current at V_{DDR} = 1 V (note 3)	I_{DDR}	–	–	5	μA
Supply current at V_{DDR} = 1 V; T_{amb} = −25 to + 70 °C (note 3)	I_{DDR}	–	–	2	μA
Oscillator					
Integrated oscillator capacitance	C_{OSC}	–	40	–	pF
Oscillator stability for: ΔV_{DD} = 100 mV at V_{DD} = 1,5 V; T_{amb} = 25 °C	f/f_{OSC}	–	2×10^{-6}	–	–

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Quartz crystal parameters					
Frequency = 32,768 kHz					
Series resistance	R_S	–	–	40	KΩ
Parallel capacitance	C_L	–	9	–	pF
Trimmer capacitance	C_T	5	–	25	pF

Notes to characteristics

1. The power-on reset circuit resets the I^2C bus logic when $V_{DD} < V_{POR}$.
2. When the voltages are a diode voltage above or below the supply voltage V_{DD} or V_{SS} an input current will flow; this current must not exceed ± 0,5 mA.
3. Event or 50 Hz mode only (no Quartz).

APPLICATION INFORMATION

The PCF8583 slave address has a fixed combination 1010 as group 1.

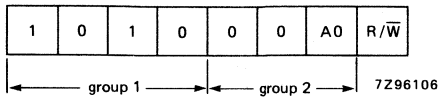


Fig. 16 PCF8583 address.

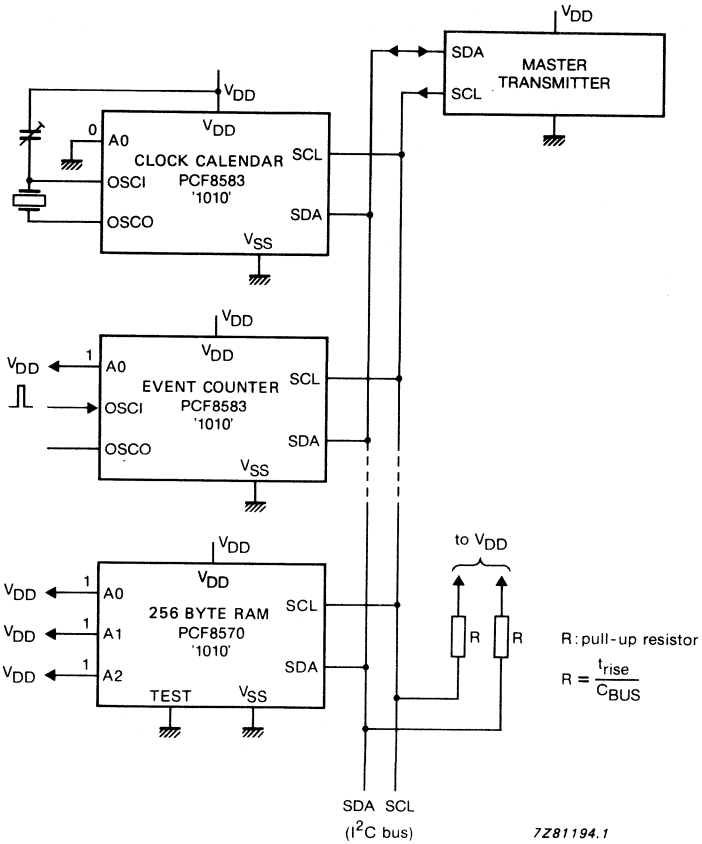


Fig. 17 PCF8583 application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specifications defined by Philips.

8-BIT A/D AND D/A CONVERTER

GENERAL DESCRIPTION

The PCF8591 is a single chip, single supply low power 8-bit CMOS data acquisition device with four analogue inputs, one analogue output and a serial I^2C bus interface. Three address pins A0, A1 and A2 are used for programming the hardware address, allowing the use of up to eight devices connected to the I^2C bus without additional hardware. Address, control and data to and from the device are transferred serially via the two-line bidirectional bus (I^2C).

The functions of the device include analogue input multiplexing, on-chip track and hold function, 8-bit analogue-to-digital conversion and an 8-bit digital-to-analogue conversion. The maximum conversion rate is given by the maximum speed of the I^2C bus.

FEATURES

- Single power supply
- Operating supply voltage 2,5 V to 6 V
- Low standby current
- Serial input/output via I^2C bus
- Address by 3 hardware address pins
- Sampling rate given by I^2C bus speed
- 4 analogue inputs programmable as single-ended or differential inputs
- Auto-incremented channel selection
- Analogue voltage range from V_{SS} to V_{DD}
- On-chip track and hold circuit
- 8-bit successive approximation A/D conversion
- Multiplying DAC with one analogue output

APPLICATIONS

Closed loop control systems; low power converter for remote data acquisition; battery operated equipment; acquisition of analogue values in automotive, audio and TV applications.

PACKAGE OUTLINES

PCF8591P:16-lead DIL; plastic (SOT38).
PCF8591T:16-lead mini-pack; plastic (SO16L; SOT162A).

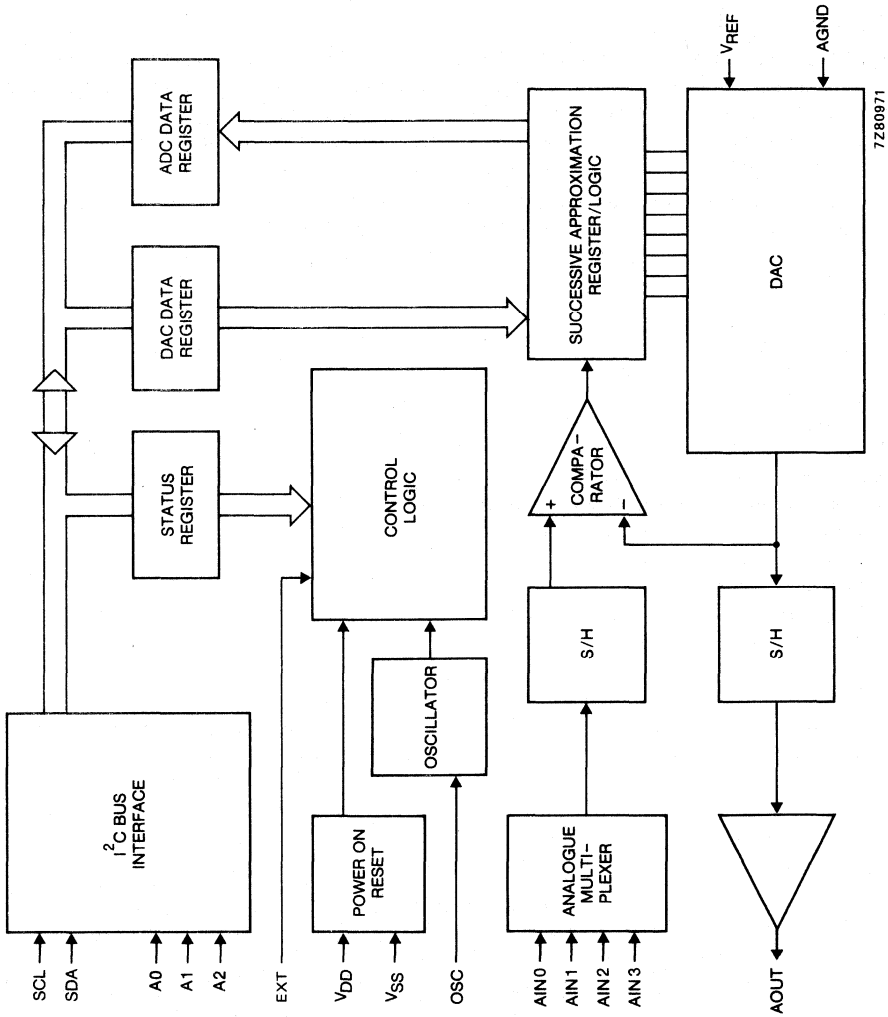


Fig. 1 Block diagram.

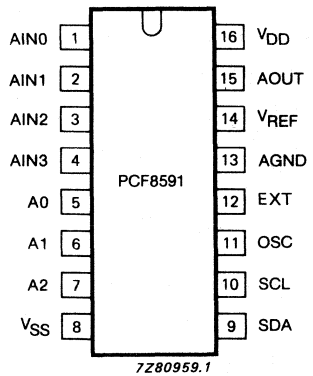


Fig. 2 Pinning diagram.

PINNING

1.	AIN0	analogue inputs (A/D converter)
2.	AIN1	
3.	AIN2	
4.	AIN3	
5.	A0	hardware address
6.	A1	
7.	A2	
8.	V_{SS}	negative supply voltage
9.	SDA	I^2C bus data input/output
10.	SCL	I^2C bus clock input/output
11.	OSC	oscillator input/output
12.	EXT	external/internal switch for oscillator input
13.	AGND	analogue ground
14.	V_{REF}	voltage reference input
15.	AOUT	analogue output (D/A converter)
16	V_{DD}	positive supply voltage

FUNCTIONAL DESCRIPTION

DEVELOPMENT DATA

Adressing

Each PCF8591 device in an I^2C bus system is activated by sending a valid address to the device. The address consists of a fixed part and a programmable part. The programmable part must be set according to the address pins A0, A1 and A2. The address always has to be sent as the first byte after the start condition in the I^2C bus protocol. The last bit of the address byte is the read/write-bit which sets the direction of the following data transfer (see Figs 3 and 10).

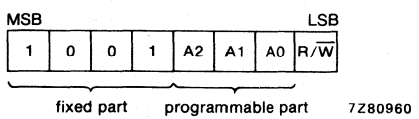


Fig. 3 Address byte.

Control byte

The second byte sent to a PCF8591 device will be stored in its control register and is required to control the device function.

The upper nibble of the control register is used for enabling the analogue output, and for programming the analogue inputs as single-ended or differential inputs. The lower nibble selects one of the analogue input channels defined by the upper nibble (see Fig. 4). If the auto-increment flag is set the channel number is incremented automatically after each A/D conversion.

The selection of a non-existing input channel results in the highest available channel number being allocated. Therefore, if the auto-increment flag is set, the next selected channel will be always channel 0. The most significant bits of both nibbles are reserved for future functions and have to be set to 0. After a power-on reset condition all bits of the control register are reset to 0. The D/A converter and the oscillator are disabled for power saving. The analogue output is switched to a high impedance state.

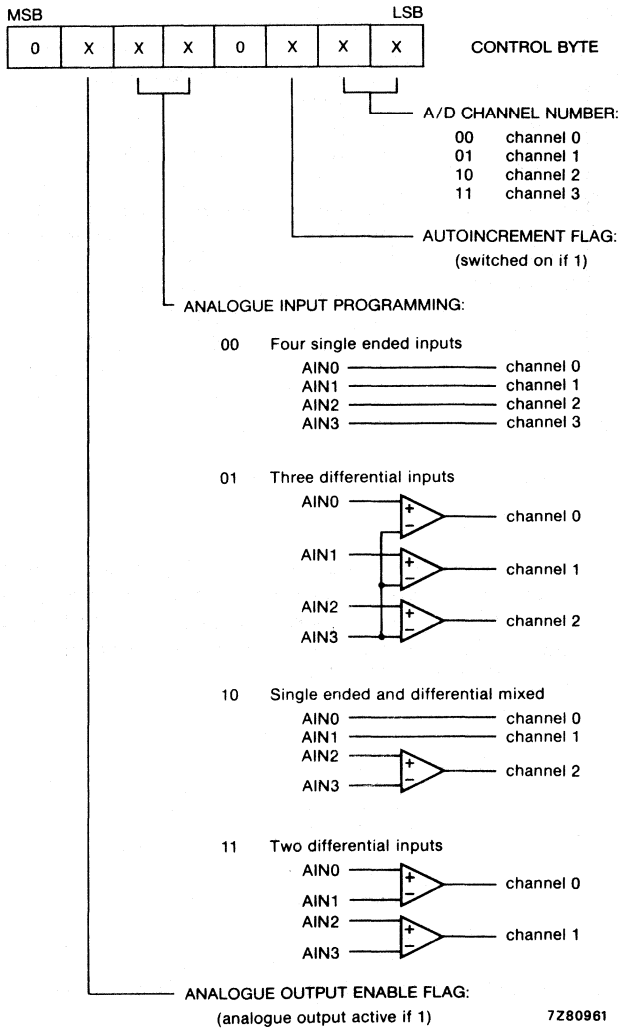


Fig. 4 Control byte.

D/A conversion

The third byte sent to a PCF8591 device is stored in the DAC data register and is converted to the corresponding analogue voltage using the on-chip D/A converter. This D/A converter consists of a resistor divider chain connected to the external reference voltage with 256 taps and selection switches. The tap-decoder switches one of these taps to the DAC output line (see Fig. 5).

The analogue output voltage is buffered by an auto-zeroed unity gain amplifier. This buffer amplifier may be switched on or off by setting the analogue output enable flag of the control register. In the active state the output voltage is held until a further data byte is sent.

The on-chip D/A converter is also used for successive approximation A/D conversion. In order to release the DAC for an A/D conversion cycle the unity gain amplifier is equipped with a track and hold circuit. This circuit holds the output voltage while executing the A/D conversion.

The output voltage supplied to the analogue output AOUT is given by the formula shown in Fig. 6. The waveforms of a D/A conversion sequence are shown in Fig. 7.

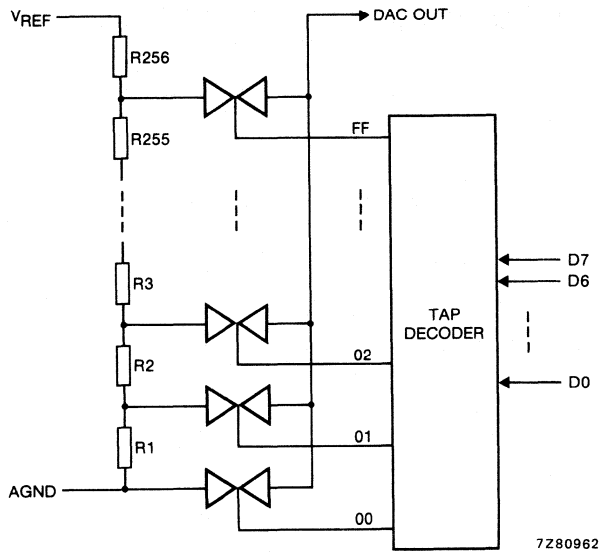


Fig. 5 DAC resistor divider chain.

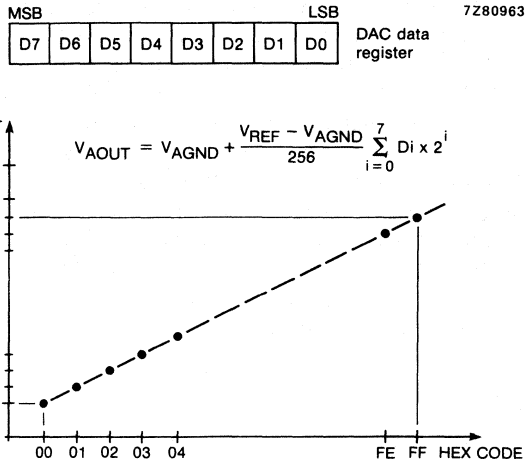


Fig. 6 DAC data and d.c. conversion characteristics.

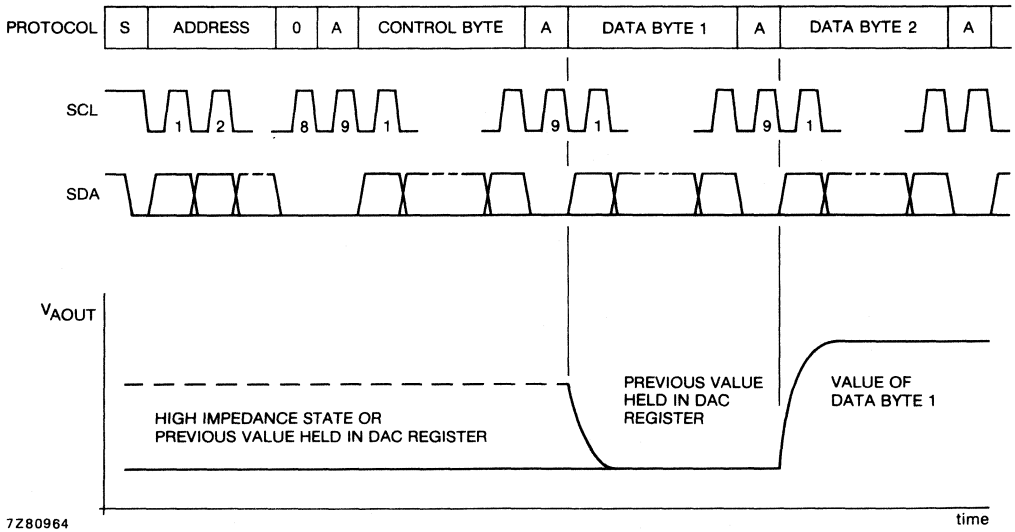


Fig. 7 D/A conversion sequence.

A/D conversion

The A/D converter makes use of the successive approximation conversion technique. The on-chip D/A converter and a high gain comparator are used temporarily during an A/D conversion cycle.

An A/D conversion cycle is always started after sending a valid read mode address to a PCF8591 device. The A/D conversion cycle is triggered at the trailing edge of the acknowledge clock pulse and is executed while transmitting the result of the previous conversion (see Fig. 8).

Once a conversion cycle is triggered an input voltage sample of the selected channel is stored on the chip and is converted to the corresponding 8-bit binary code. Samples picked up from differential inputs are converted to an 8-bit two's complement code (see Fig. 9). The conversion result is stored in the ADC data register and awaits transmission. If the auto-increment flag is set the next channel is selected.

The first byte transmitted in a read cycle contains the conversion result code of the previous read cycle. After a power-on reset condition the first byte read is a hexadecimal 80. The protocol of an I^2C bus read cycle is shown in Fig. 10.

The maximum A/D conversion rate is given by the actual speed of the I^2C bus.

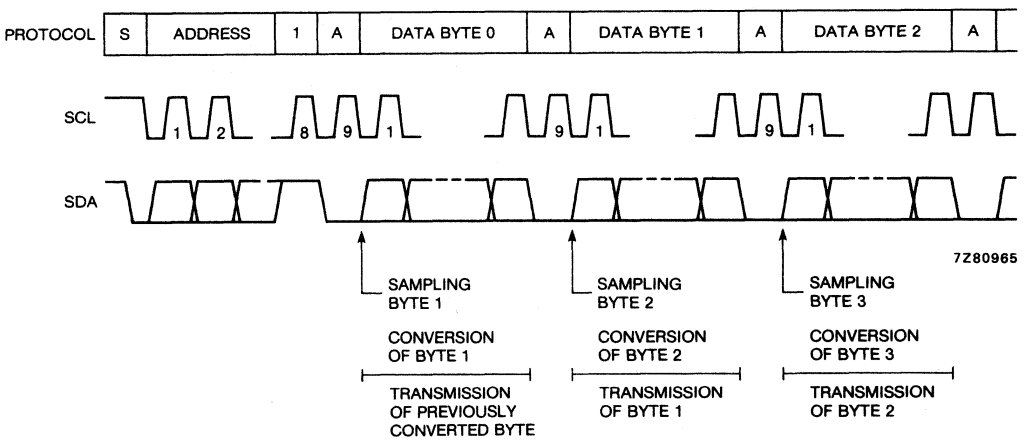


Fig. 8 A/D conversion sequence.

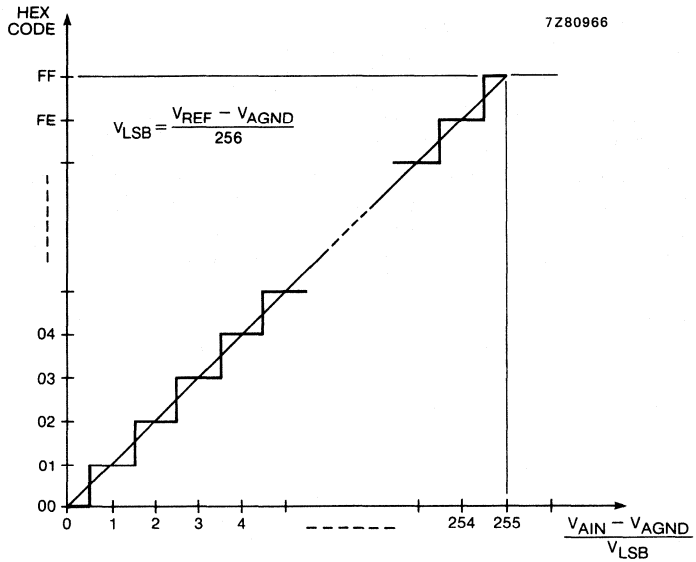


Fig. 9a A/D conversion characteristics of single-ended inputs.

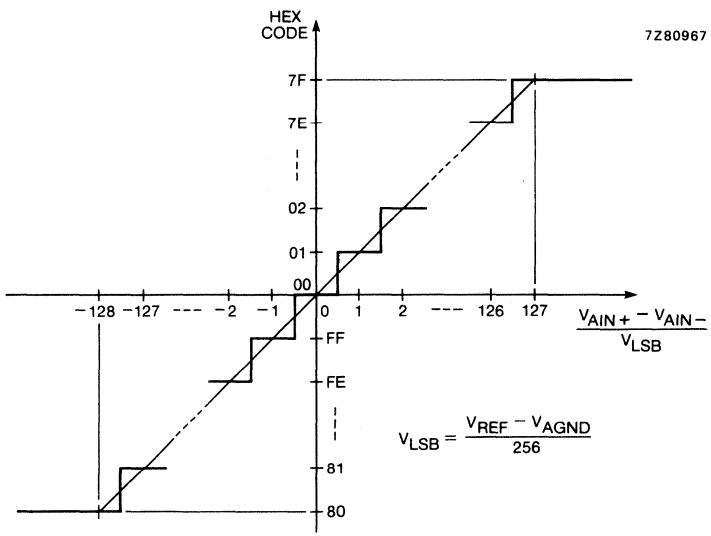


Fig. 9b A/D conversion characteristics of differential inputs.

Reference voltage

For the D/A and A/D conversion either a stable external voltage reference or the supply voltage has to be applied to the resistor divider chain (pins V_{REF} and AGND). The AGND pin has to be connected to the system analogue ground and may have a d.c. off-set with reference to V_{SS}.

A low frequency may be applied to the V_{REF} and AGND pins. This allows the use of the D/A converter as a one-quadrant multiplier; see Application Information and Fig. 6.

The A/D converter may also be used as a one or two quadrant analogue divider. The analogue input voltage is divided by the reference voltage. The result is converted to a binary code. In this application the user has to keep the reference voltage stable during the conversion cycle.

Oscillator

An on-chip oscillator generates the clock signal required for the A/D conversion cycle and for refreshing the auto-zeroed buffer amplifier. When using this oscillator the EXT pin has to be connected to V_{SS}. At the OSC pin the oscillator frequency is available.

If the EXT pin is connected to V_{DD} the oscillator output OSC is switched to a high impedance state allowing the user to feed an external clock signal to OSC.

Bus protocol

After a start condition a valid hardware address has to be sent to a PCF8591 device. The read/write bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the start condition (S), the stop condition (P) and the acknowledge bit (A) refer to the I^2C bus characteristics. In the write mode a data transfer is terminated by sending either a stop condition or the start condition of the next data transfer.

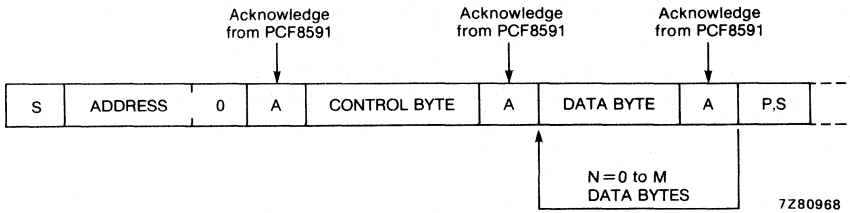


Fig. 10a Bus protocol for write mode, D/A conversion.

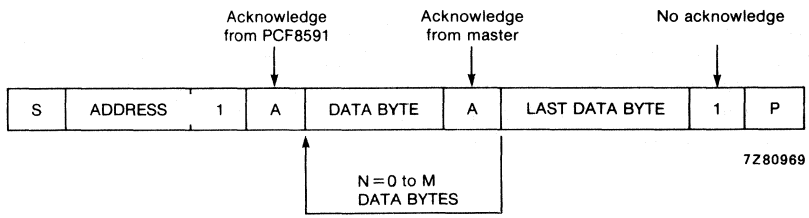


Fig. 10b Bus protocol for read mode, A/D conversion.

CHARACTERICS OF THE I²C BUS

The I²C bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transfered during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

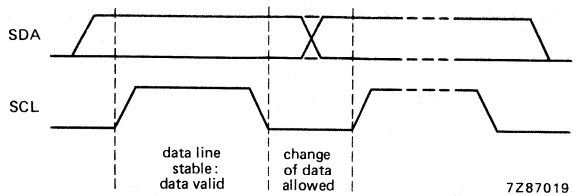


Fig. 11 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the stop condition (P).

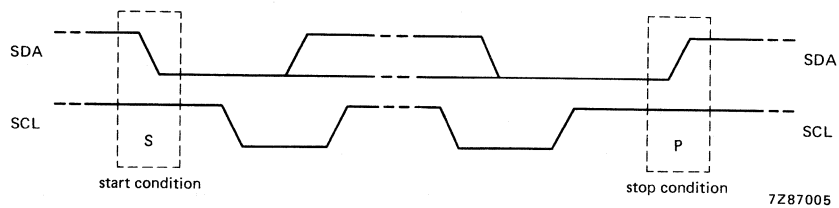


Fig. 12 Definition of start and stop condition.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

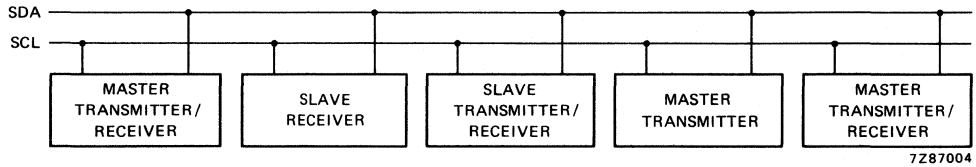


Fig. 13 System configuration.

Acknowledge.

The number of data bytes transfered between the start and stop conditions from transmitter to receiver is not limited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master also generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

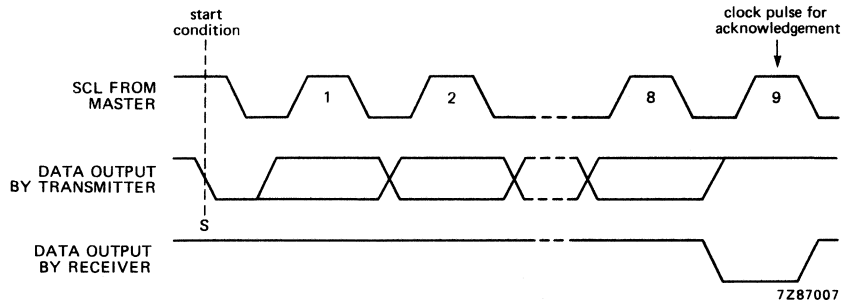


Fig. 14 Acknowledgement on the I^2C bus.

DEVELOPMENT DATA

Timing specifications

All the timing values are valid within the operating supply voltage and ambient temperature range and refer to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

parameter	symbol	min.	typ.	max.	unit
SCL clock frequency	f_{SCL}	–	–	100	kHz
Tolerable spike width on bus	t_{SW}	–	–	100	ns
Bus free time	t_{BUF}	4,0	–	–	μs
Start condition set-up time	$t_{SU;STA}$	4,0	–	–	μs
Start condition hold time	$t_{HD;STA}$	4,7	–	–	μs
SCL LOW time	t_{LOW}	4,7	–	–	μs
SCL HIGH time	t_{HIGH}	4,0	–	–	μs
SCL and SDA rise time	t_R	–	–	1,0	μs
SCL and SDA fall time	t_F	–	–	0,3	μs
Data set-up time	$t_{SU;DAT}$	250	–	–	ns
Data hold time	$t_{HD;DAT}$	0	–	–	ns
SCL LOW to data out valid	$t_{VD;DAT}$	–	–	3,4	μs
Stop condition set-up time	$t_{SU;STO}$	4,0	–	–	μs

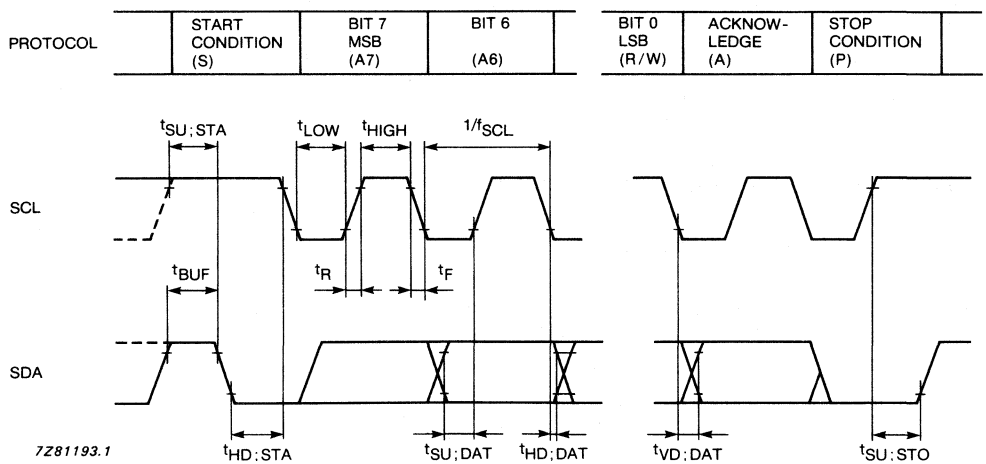


Fig. 15 I²C bus timing diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage range	V_{DD}		−0,5 to +8,0 V
Voltage on any pin	V_I		−0,5 to V_{DD} +0,5 V
Input current d.c.	I_I	max.	10 mA
Output current d.c.	I_O	max.	20 mA
V_{DD} or V_{SS} current	I_{DD}, I_{SS}	max.	50 mA
Power dissipation per package	P_{tot}	max.	300 mW
Power dissipation per output	P	max.	100 mW
Storage temperature range	T_{stg}		−65 to +150 °C
Operating ambient temperature range	T_{amb}		−40 to +85 °C

Note:

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is advised to take handling precautions appropriate to handling MOS devices (see 'Handling MOS devices').

CHARACTERISTICS

V_{DD} = 2,5 V to 6 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage	operating	V_{DD}	2,5	–	6,0	V
Supply current	standby $V_I = V_{SS}$ or V_{DD}; no load	I_{DD0}	–	1	15	μA
Supply current	operating; AOUT off; f_{SCL} = 100 kHz	I_{DD1}	–	125	250	μA
Supply current	AOUT active; f_{SCL} = 100 kHz	I_{DD2}	–	0,45	1,0	mA
Power-on reset level	note 1	V_{POR}	0,8	–	2,0	V
Digital inputs/output	SCL, SDA, A0, A1, A2					
Input voltage	LOW	V_{IL}	0	–	0,3 x V_{DD}	V
Input voltage	HIGH	V_{IH}	0,7 x V_{DD}	–	V_{DD}	V
Input current	leakage; $V_I = V_{SS}$ to V_{DD}	I_I	–	–	250	nA
Input capacitance		C_I	–	–	5	pF
SDA output current	leakage; HIGH at $V_{OH} = V_{DD}$	I_{OH}	–	–	250	nA
SDA output current	LOW at V_{OL} = 0,4 V	I_{OL}	3,0	–	–	mA

parameter	conditions	symbol	min.	typ.	max.	unit
Reference voltage inputs	V_{REF}, AGND					
Voltage range	reference	V_{REF}	V_{AGND}	–	V_{DD}	V
Voltage range	analogue ground	V_{AGND}	V_{SS}	–	V_{REF}	V
Input current	leakage	I_I	–	–	250	nA
Input resistance	V_{REF} to AGND	R_{REF}	–	100	–	kΩ
Oscillator	OSC, EXT					
Input current	leakage	I_I	–	–	250	nA
Oscillator frequency		f_{OSC}	0,75	–	1,25	MHz

D/A CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{load} = 10 kΩ; C_{load} = 100 pF; T_{amb} = −40 °C to +85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Analogue output						
Output voltage range	no resistive load	V_{OA}	V_{SS}	–	V_{DD}	V
Output voltage range	R_{load} = 10 kΩ	V_{OA}	V_{SS}	–	0,9xV_{DD}	V
Output current	leakage; AOUT disabled	I_{LO}	–	–	250	nA
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	50	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error	no resistive load	G_e	–	–	1	%
Settling time	to ½ LSB full scale step	t_{DAC}	–	–	90	μs
Conversion rate		f_{DAC}	–	–	11,1	kHz
Supply noise rejection	at f = 100 Hz; V_{DD} = 0,1 V_{PP}	SNRR	–	40	–	dB

DEVELOPMENT DATA

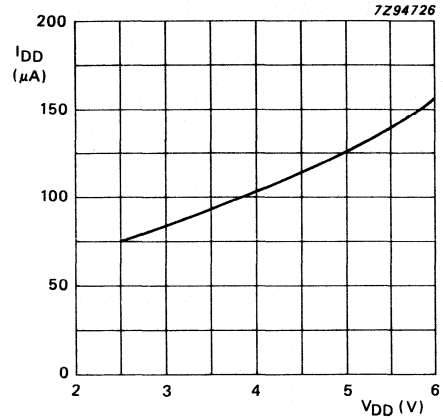
A/D CHARACTERISTICS

V_{DD} = 5,0 V; V_{SS} = 0 V; V_{REF} = 5,0 V; V_{AGND} = 0 V; R_{source} = 10 kΩ; T_{amb} = −40 °C to +85 °C unless otherwise specified

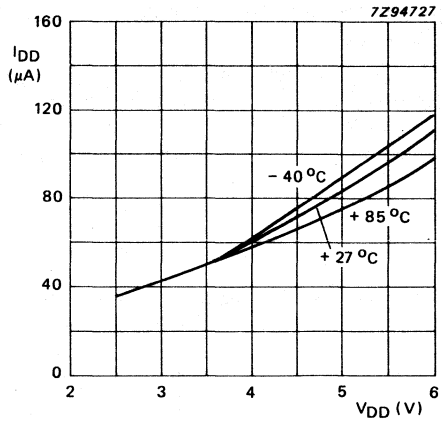
parameter	conditions	symbol	min.	typ.	max.	unit
Analogue inputs						
Input voltage range		V_{IA}	V_{SS}	–	V_{DD}	V
Input current	leakage	I_{IA}	–	–	100	nA
Input capacitance		C_{IA}	–	10	–	pF
Input capacitance	differential	C_{ID}	–	10	–	pF
Single-ended voltage	measuring range	V_{IS}	V_{AGND}	–	V_{REF}	V
Differential voltage	measuring range; $V_{FS} = V_{REF} - V_{AGND}$	V_{ID}	$\frac{-V_{FS}}{2}$	–	$\frac{+V_{FS}}{2}$	V
Accuracy						
Offset error	T_{amb} = 25 °C	OS_e	–	–	20	mV
Linearity error		L_e	–	–	±1,5	LSB
Gain error		G_e	–	–	1	%
Gain error	small-signal; ΔV_{IN} = 16 LSB	GS_e	–	–	5	%
Rejection ratio	common-mode	CMRR	–	60	–	dB
Supply noise rejection	at f = 100 Hz; V_{DDN} = 0,1xV_{PP}	SNRR	–	40	–	dB
Conversion time		t_{ADC}	–	–	90	μs
Sampling/conversion rate		f_{ADC}	–	–	11,1	kHz

Note

1. The power on reset circuit resets the I^2C bus logic when V_{DD} is less than V_{POR}.



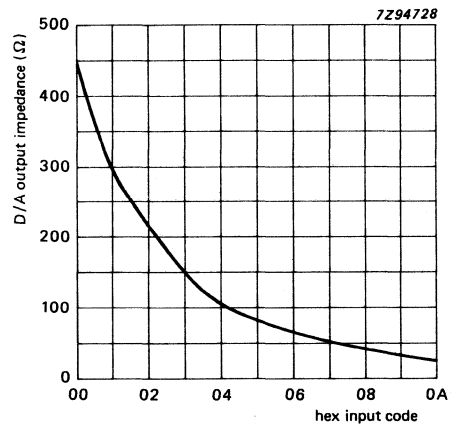
(a) internal oscillator; T_{amb} = + 27 °C.



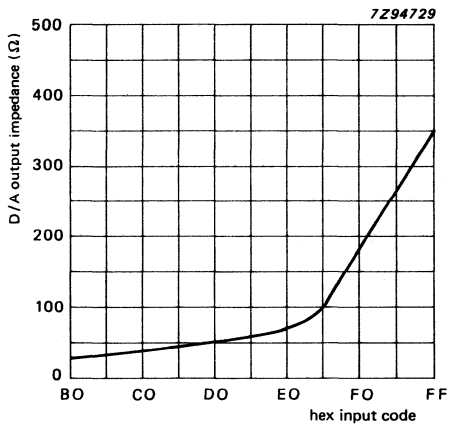
(b) external oscillator.

Fig. 16 Operating supply current against supply voltage (analogue output disabled).

DEVELOPMENT DATA



(a) output impedance near negative power rail; T_{amb} = + 27 °C.



(b) output impedance near positive power rail; T_{amb} = + 27 °C.

Fig. 17 Output impedance of analogue output buffer (near power rails).

The x-axis represents the hex input-code equivalent of the output voltage.

APPLICATION INFORMATION

Inputs must be connected to V_{SS} or V_{DD} when not in use. Analogue inputs may also be connected to AGND or V_{REF}.

In order to prevent excessive ground and supply noise and to minimize cross-talk of the digital to analogue signal paths the user has to design the printed-circuit board layout very carefully. Supply lines common to a PCF8591 device and noisy digital circuits and ground loops should be avoided. Decoupling capacitors ($> 10\ \mu F$) are recommended for power supply and reference voltage inputs.

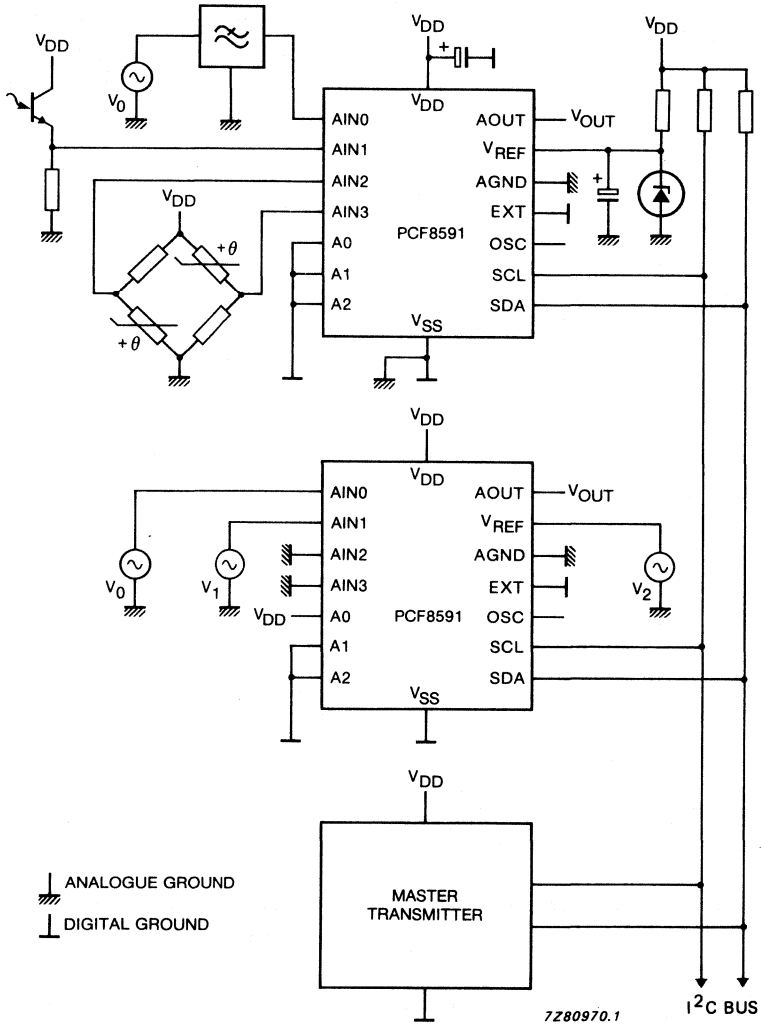


Fig. 18 Application diagram.

Purchase of Philips' I²C components conveys a license under the Philips' I²C patent to use the components in the I²C-system provided the system conforms to the I²C specification defined by Philips.

FOR DETAILED INFORMATION SEE RELEVANT DATA BOOK OR DATA SHEET

16/32-BIT MICROPROCESSOR

GENERAL DESCRIPTION

The 68070 is a highly integrated 16/32-bit central processing unit for use in a large variety of applications and is fully software compatible with the 68000. Integrating standard as well as advanced peripheral functions on the 68070 (housed in an 84-pin package), dramatically reduces system cost.

This document gives an overview of the basic functions, internal structure, and d.c. and a.c. characteristics. For further detail on the features and operation of 68070, refer to "User manual SCC68070" (Hardware and Software).

FEATURES

- **CHMOS technology**
- **32-bit internal structure**
- **Enhanced bus error handling**
- **84-pin package**
- **4 decoded interrupt inputs**
- **2 programmable interrupt inputs**
- **Decoded interrupt acknowledge**
- **Built-in clock generator: max. 20 MHz crystal**
- **On-chip MMU, supporting virtual memory**
- **2-channel DMA controller**
- **I^2C serial bus interface**
- **UART serial interface**
- **16-bit timer/counter**
- **Two 16-bit match/count/capture registers**

- **Full 68000 software compatibility**
- **68000-compatible bus interface (10 MHz)**
- **56 powerful instruction types**
- **5 basic data types**
- **16 Mbyte addressing range**
- **14 addressing modes**
- **Memory mapped I/O**
- **Vectored and auto-vectored interrupts**
- **7 interrupt levels**
- **Maximum internal clock frequency: 10 MHz**

The internal architecture of the 68070 is built around a bus interconnecting the CPU and the various on-chip peripheral functions. Each function has several dedicated connections to the external circuitry. The 68070 includes powerful programmable interrupt processing circuitry for interrupts generated by internal and external sources. An on-chip clock generator provides a 10 MHz clock signal for CPU and peripheral interfaces.

If enabled, the on-chip MMU takes care of address translation and memory protection. Two DMA channels increase data throughput and the I^2C-bus interface allows easy and low-cost addition of peripherals (master and slave devices). The 68070 also includes a UART interface. A built-in Timer/counter with two independently programmable MATCH/COUNT/CAPTURE registers means that the 68070 can be programmed with two of the following options simultaneously:

- pulse generator;
- external event counter;
- reference timer.

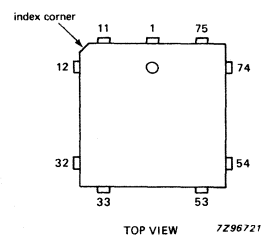


Fig.1 Pin configuration.

ORDERING INFORMATION

type number	temperature range	clock frequency	package
SCC68070CAA84	0 to 70°C	10 MHz	84-pin PLCC

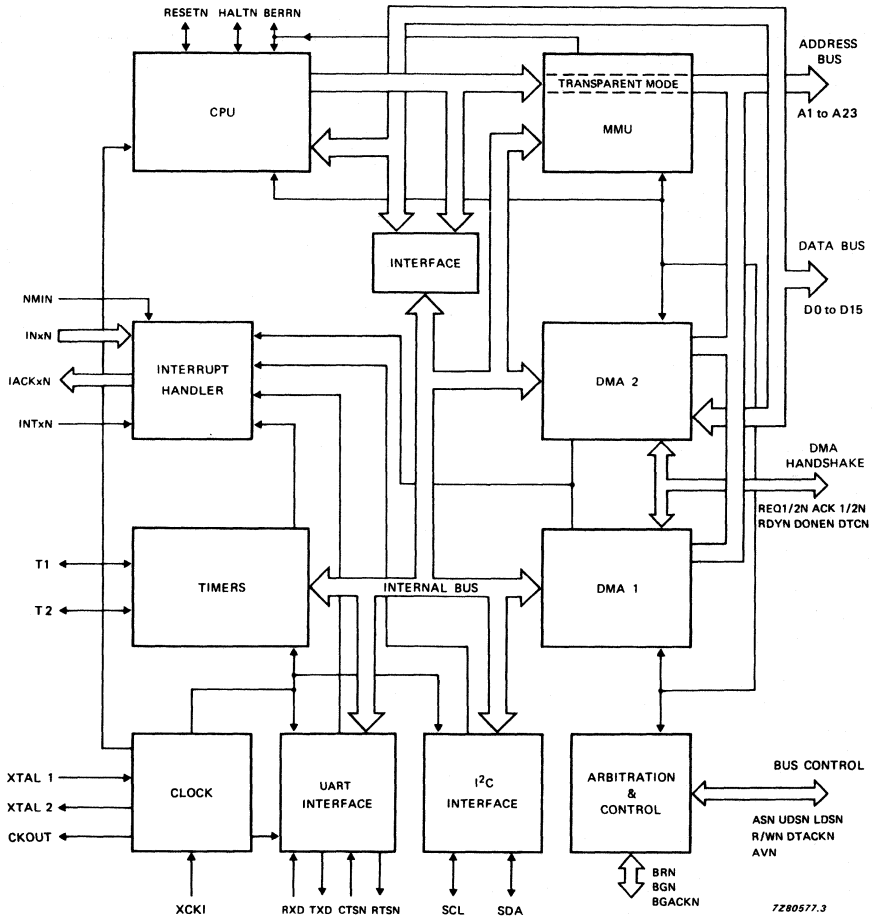


Fig.2 Block diagram.

FM/IF AMPLIFIER CIRCUIT

The TDA1576 is a monolithic integrated f.m./i.f. amplifier circuit provided with the following functions:

- symmetrical limiting i.f. amplifier
- symmetrical quadrature demodulator
- internal muting circuit
- symmetrical a.f.c. output
- field-strength indication output
- detune-detector
- reference voltage output
- electronic smoothing of the supply voltage
- standby on/off switching circuit.

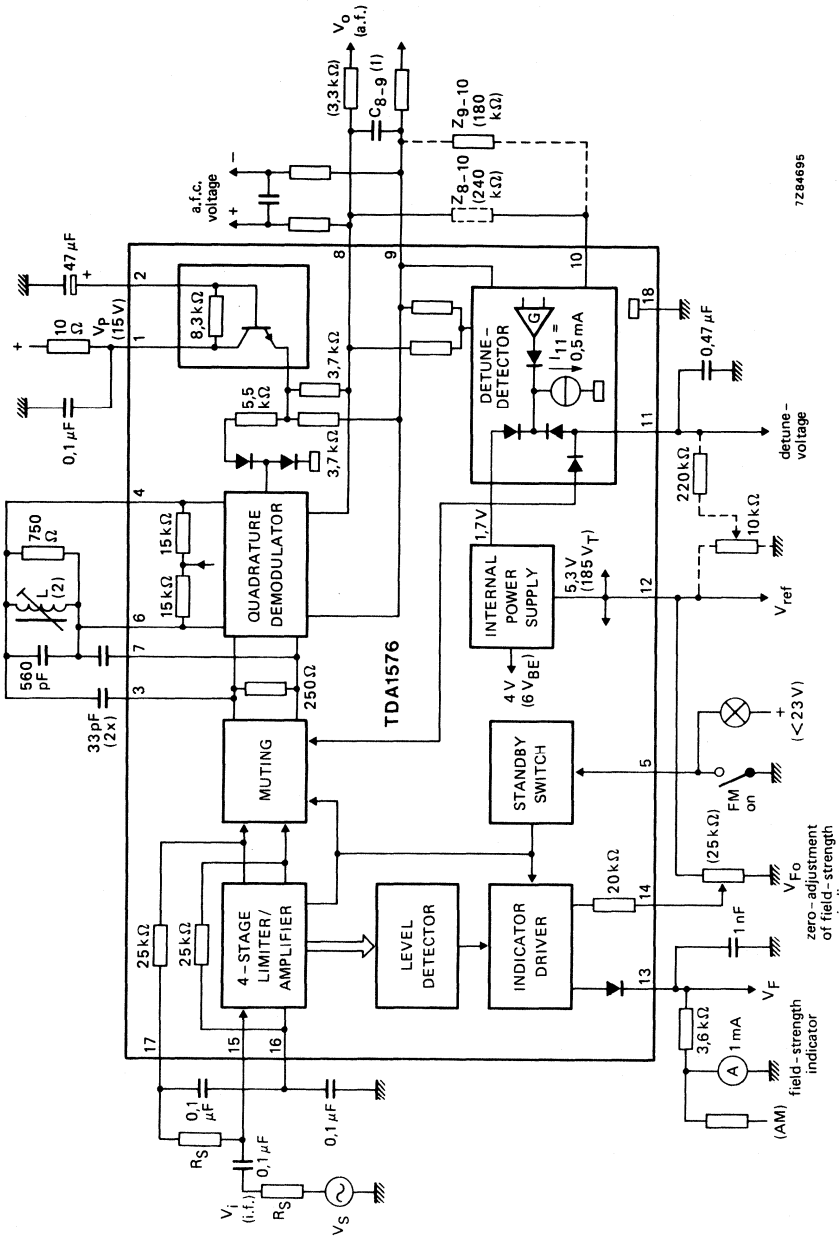
QUICK REFERENCE DATA

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; Q_L = 20; de-emphasis τ = 50 μs

Supply voltages (pin 1)	V_P		8,5	15	V
Supply current	I_P	typ.	16	18	mA
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
A.F. output voltage	V_o	typ.	67	135	mV
Total distortion					
single tuned circuit	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio; $V_i > 1$ mV	S + N/N	typ.	76	80	dB
A.M. rejection	α	typ.	50		dB
A.F.C. offset drift	$\pm \Delta f$	typ.	3		kHz
		<	6		kHz
Field-strength indication range	ΔV_i	typ.	90		dB
Permissible indicator (load) current	I_L	<	2		mA
Supply voltage range (pin 1)	V_P		7,5 to 20		V
Ambient temperature range	T_{amb}		−30 to +80		°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).



(1) For de-emphasis $\tau = 50\ \mu s$: $C_{8\text{-}9} = 6{,}8$ nF.
For stereo operation: $C_{8\text{-}9} = 56$ pF.

(2) $L = 0{,}38\ \mu H$; $Q_o = 70$; $Q_L = 20$; adjusted to minimum 2nd harmonic distortion (d_2); at $V_i = 1$ mV; coil: 6 turns CuL (0,25 mm) on coil former KAN (C).

Fig. 1 Block diagram and test circuit.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 1)	$V_P = V_{1-18}$	max.	23	V
Voltages				
at pin 2	V_{2-18}	max.	V_P	V
	$-V_{2-18}$	max.	0	V
at pin 5	V_{5-18}	max.	23	V
	$-V_{5-18}$	max.	0	V
at pin 12	V_{12-18}	max.	7	V
	$-V_{12-18}$	max.	0	V
at pin 13	V_{13-18}	max.	6	V
at pin 14	V_{14-18}	max.	23	V
	$-V_{14-18}$	max.	0	V
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−55 to + 150	°C
Operating ambient temperature range	T_{amb}		−30 to + 80	°C

THERMAL RESISTANCE

From crystal to ambient	$R_{th\ cr\text{-}a}$	=	80	K/W

CHARACTERISTICS

f_o = 10,7 MHz; Δf = ± 22,5 kHz; f_m = 400 Hz; R_S = 60 Ω; de-emphasis τ = 50 μs (C_{8-9} = 6,8 nF); T_{amb} = 25 °C; measured in Fig. 1, unless otherwise specified. The demodulator circuit is adjusted at minimum 2nd harmonic (d_2) distortion: V_i = 1 mV; Δf = ± 75 kHz.

Supply voltage range (pin 1)		V_P		7,5 to 20	V
		V_P = 8,5 V		V_P = 15 V	
Supply current; without load ($I_{12} = I_{13} = 0$)	I_P	typ.	16	18	mA
			10 to 23	12 to 25	mA
I.F. amplifier/detector					
Sensitivity at −3 dB before limiting	V_i	typ.	22		μV
		<	30		μV
I.F. sensitivity for					
S + N/N = 26 dB	V_i	typ.	8		μV
S + N/N = 46 dB	V_i	typ.	35		μV
I.F. output voltage (peak-to-peak value) V_i = 1 mV; $Z_{3-18} = Z_{7-18}$ = 1 MΩ in parallel with 10 pF	$V_{3-7(p-p)}$	typ.	680		mV
I.F. output resistance	R_{3-7}	typ.	250		Ω
Detector input impedance	R_{4-6}	typ.	30		kΩ
	C_{4-6}	typ.	1		pF
Output resistance	R_8; R_9	typ.	3,7		kΩ
D.C. output voltage	$V_{8-18} = V_{9-18}$	typ.	5,5	9,8	V
A.F. output voltage; Q_L = 20	V_o	typ.	67	135	mV
			60 to 75	120 to 150	mV
Total distortion					
single tuned circuit; Q_L = 20	d_{tot}	typ.	0,1		%
two tuned circuits	d_{tot}	typ.	0,02		%
Signal plus noise-to-noise ratio B = 250 Hz to 15 kHz; V_i > 1 mV	S + N/N	typ.	76	80	dB
A.M. rejection; V_i = 10 mV f.m.: f_m = 70 Hz; Δf = ± 22,5 kHz a.m.: f_m = 1 kHz; m = 0,3	α	typ.	54		dB*
I.F. input voltage range; α > 40 dB	V_i		0,5 to 500		mV
Hum suppression at f = 100 Hz $V_P = V_{1-18}$ = 100 mV r.m.s.; C_{2-18} = 47 μF	α_{100}	>	43		dB
		typ.	48		dB
A.F.C. tuning slope at Q_L = 20	$\frac{\Delta V_{8-9}}{\Delta f_o}$	typ.	8,5	17	mV/kHz
A.F.C. offset voltages; Q_L = 20 at V_i = 1 mV	$\pm \Delta V_{8-9}$	<	100	200	mV
at V_i = 30 μV to 500 mV (reference at 1 mV and muting)	$\pm \Delta V_{8-9}$	typ.	25	50	mV
		<	50	100	mV

* Simultaneously measured.

Field-strength indication

			V_P = 8,5 V	V_P = 15 V	
			20 μV to 600 mV		
Indicator sensitivity; I_{14} = 0	V_i				
Field-strength indicator voltage					
R_{13-18} = 3,6 kΩ; I_{14} = 0					
V_i = 0	$V_F = V_{13-18}$	typ.	0		mV
		<	200		mV
V_i = 250 mV	$V_F = V_{13-18}$	typ.	3,6		V
			3,2 to 4,1		V
Available output current	$-I_{13}$	>	2		mA
Reverse voltage at the output for FM 'off'; $V_{5-18} > 3,5$ V	V_{13-18}	>	5		V

Detune-detector

Quiescent input current; V_{10-9} = 0	I_{10}	typ.	20		nA
		<	100		nA
Output voltage range	V_{11-18}		1,8 to 5,0		V
Available output current	I_{11}	typ.	0,5		mA
			0,35 to 0,65		mA
Voltage gain: $\Delta V_{11}/\Delta(\pm V_{10-9})$ at I_{11} = 0,25 mA	G_v	typ.	–	3,3	
Input offset voltage (pin 10) at V_{11-18} = 2,5 V	V_{10-9}	typ.	20		mV

Reference voltage

Output voltage; $-I_{12}$ = 1 mA	$V_{ref} = V_{12-18}$	typ.	5,1	5,3	V
Available output current	$-I_{12}$	typ.	2,5		mA

Standby switch

Required control voltage within the rated ambient temperature and supply voltage ranges					
for FM 'on'	$V_{5\ on}$	<	2		V
for FM 'off'	$V_{5\ off}$	>	3,5		V
Input switching current for FM 'on'	$-I_5$	<	100		μA

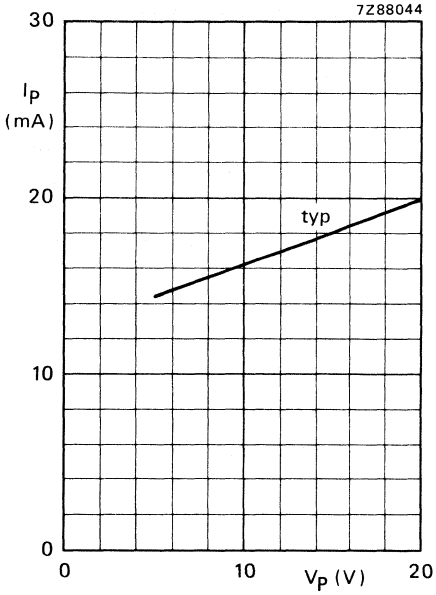


Fig. 2 Supply current consumption; without load.

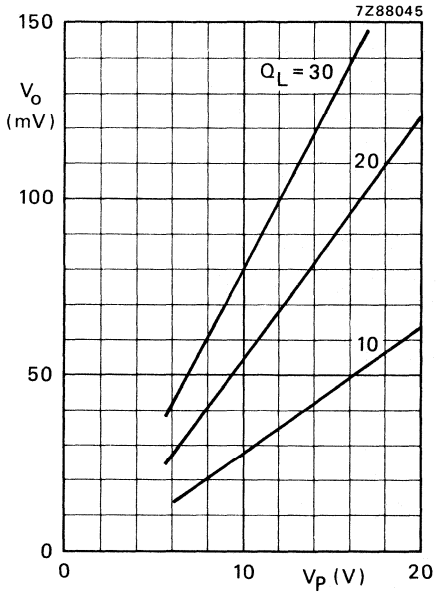


Fig. 3 A.F. output voltage; V_i = 1 mV (i.f.); $\Delta f = \pm$ 15 kHz; f_m = 400 Hz; typical values.

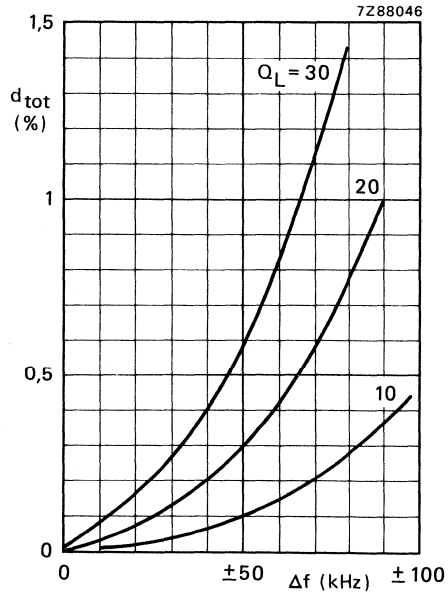


Fig. 4 Total distortion for single tuned circuit; V_i = 1 mV (i.f.); f_m = 400 Hz; adjusted at minimum 2nd harmonic distortion; typical values.

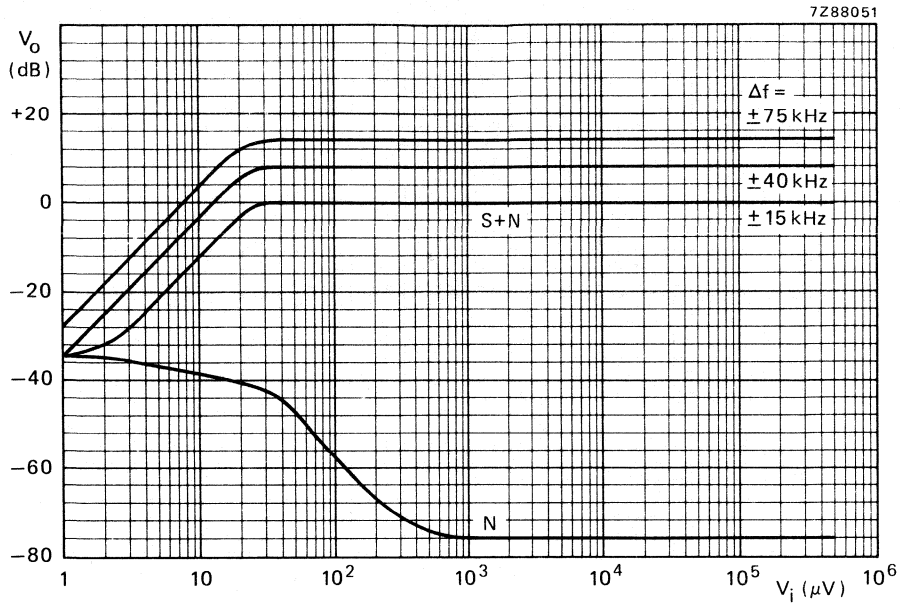


Fig. 5 A.F. output voltage level as a function of i.f. input voltage; S = signal voltage; N = noise voltage; V_P = 15 V; f_m = 400 Hz; B = 250 Hz to 16 kHz; Q_L = 20; $C_{8\text{-}9}$ = 6,8 nF; typical values.

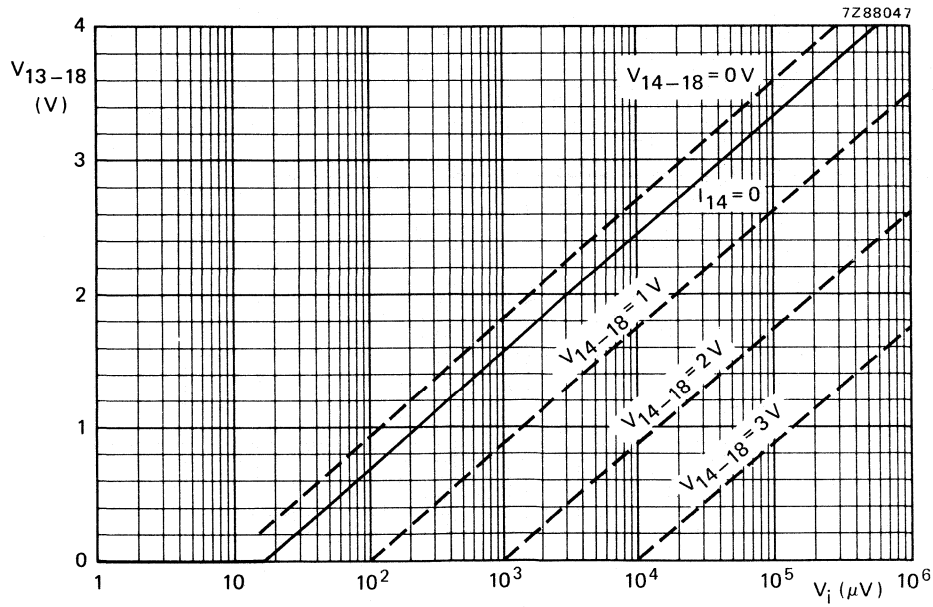


Fig. 6 Voltage at field-strength indicator output (proportional to $V_{12\text{-}18}$); $R_{13\text{-}18}$ = 3,6 kΩ.

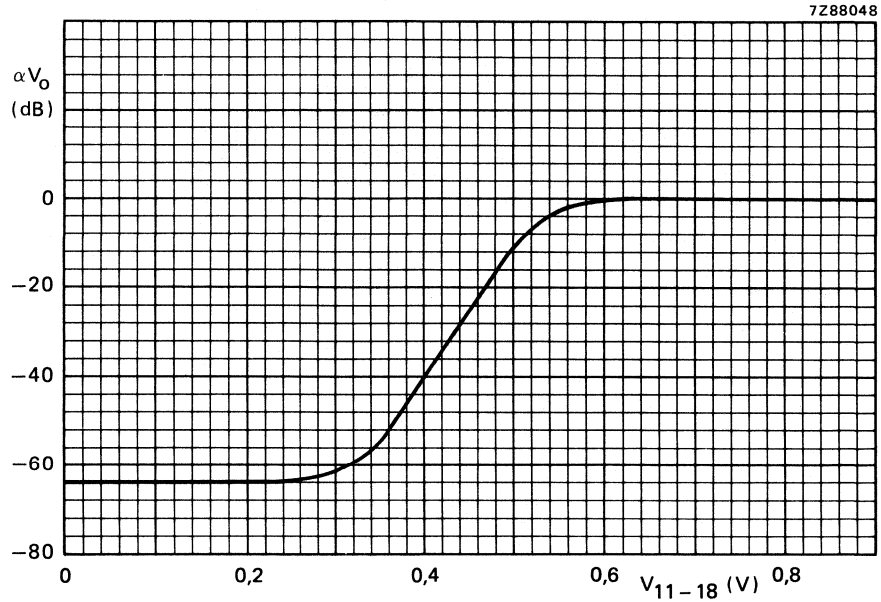


Fig. 7 Attenuation of output voltage (αV_o) as a function of the muting control voltage $V_{11\text{-}18}$.

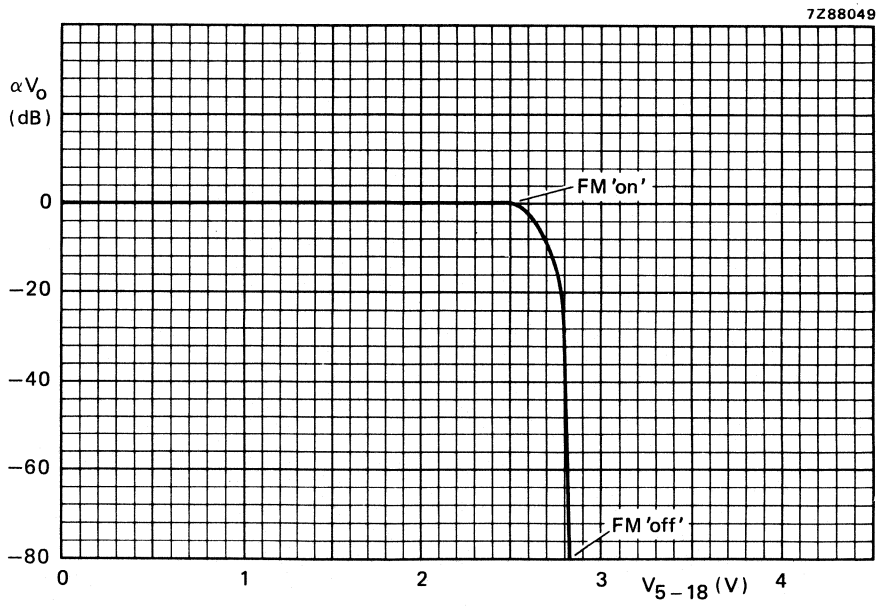
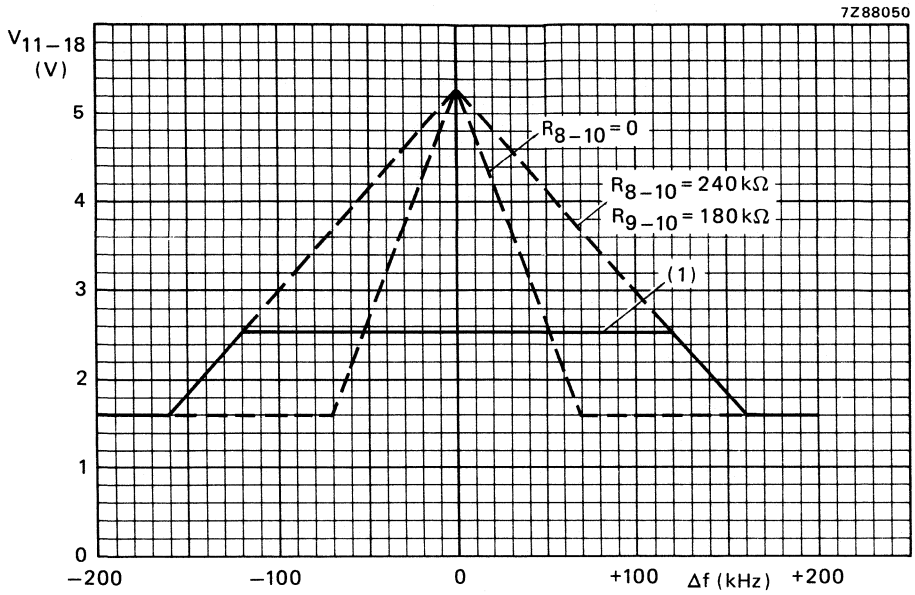


Fig. 8 FM 'on'/FM 'off' stand-by switch; attenuation of output voltage (αV_o) as a function of control voltage $V_{5\text{-}18}$.



(1) Limited by external preset ($\alpha \cdot V_{12\text{-}18}$).

Fig. 9 Detune-detector output voltage; V_P = 7,5 to 20 V; Q_L = 20.

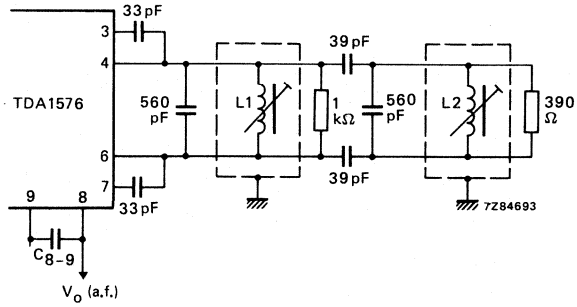


Fig. 10 Example of the TDA1576 when using a demodulator with two tuned circuits. Adjustment of the demodulator circuit is obtained with an i.f. signal which is higher than the 3 dB limiting level, L2 should be short-circuited or detuned, L1 should be adjusted to min. d_2 distortion, and then L2 to min. d_2 distortion. Coil data: L1 = L2 = 0,38 μH; Q_o = 70; coil former KAN (C).

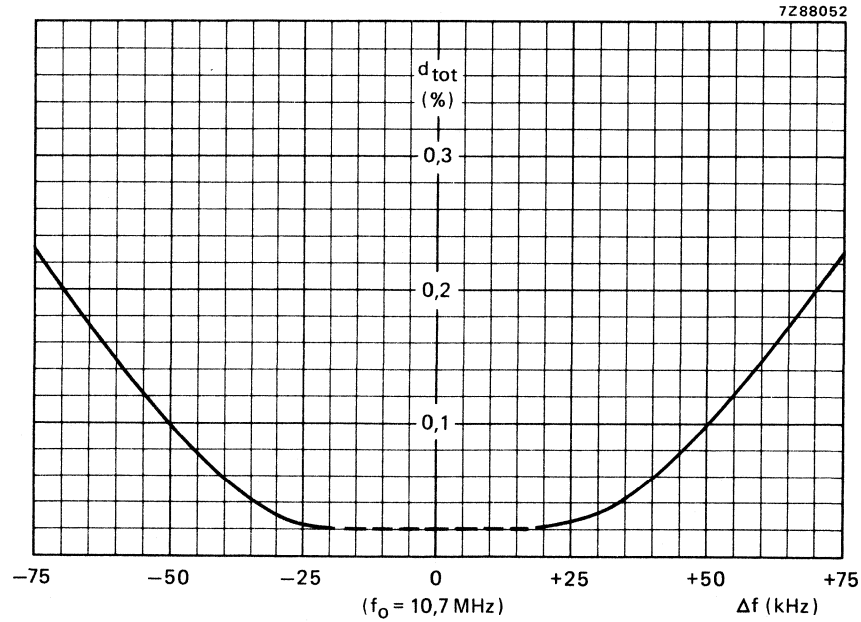
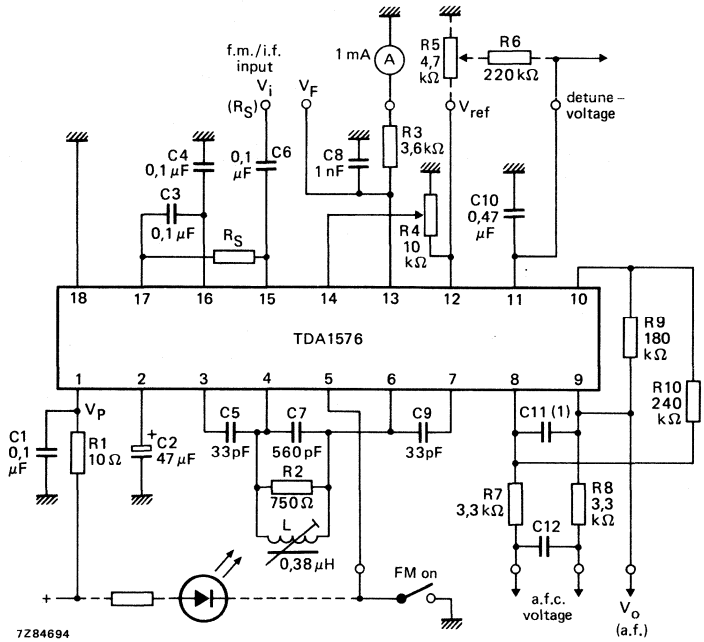


Fig. 11 Total distortion as a function of detuning; f_m = 400 Hz; C_{8-9} = 6,8 nF; $\Delta f = \pm$ 75 kHz; V_o = 330 mV for a frequency deviation $\Delta f = \pm$ 75 kHz.



(1) For mono: C11 = 6,8 nF; for stereo: C11 = 56 pF.

Fig. 12 Application example of using TDA1576.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0		V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ.	3,2	mA
Bridge tied load application (BTL)				
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ.	140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max.	70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	140	μV
Stereo application				
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ.	35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ.	75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ.	40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ.	100	μV

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6 V
Peak output current	I_{OM}	max.	150 mA
Total power dissipation	see derating curve Fig. 1		
Storage temperature range	T_{stg}	−55 to + 150	°C
Crystal temperature	T_c	max.	100 °C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5 s

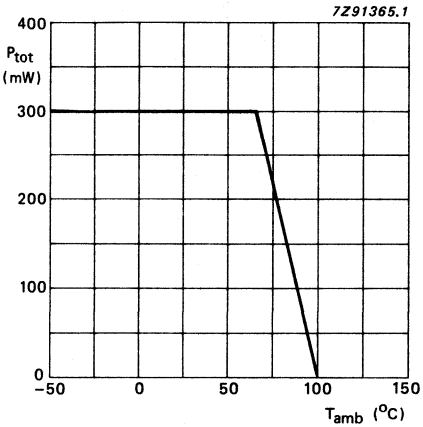


Fig. 1 Power derating curve.

THERMAL RESISTANCE

From junction to ambient R_{thj-a} = 110 K/W

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	–	26	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

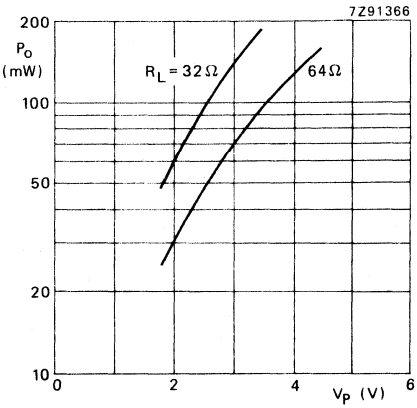


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

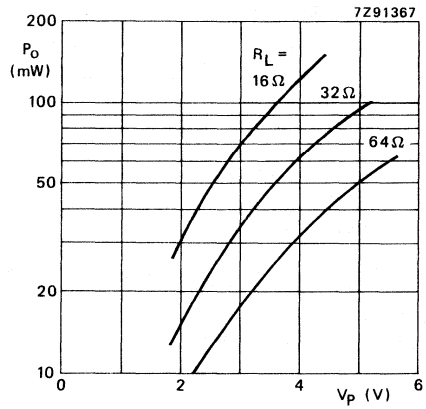


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

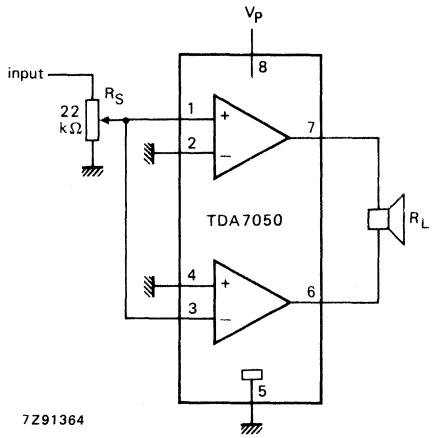


Fig. 4 Application diagram (BTL); also used as test circuit.

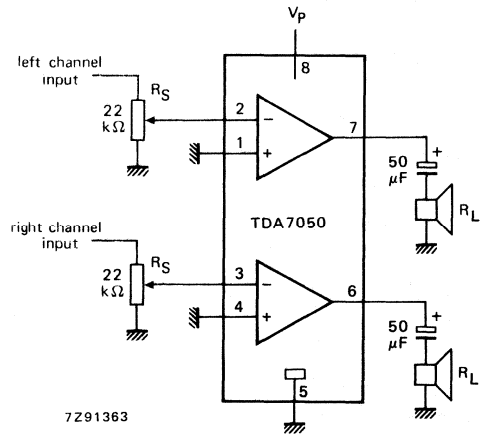


Fig. 5 Application diagram (stereo); also used as test circuit.

LOW VOLTAGE MONO/STEREO POWER AMPLIFIER

GENERAL DESCRIPTION

The TDA7050T is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

Features

- Limited to battery supply application only (typ. 3 and 4 V)
- Operates with supply voltage down to 1,6 V
- No external components required
- Very low quiescent current
- Fixed integrated gain of 26 dB, floating differential input
- Flexibility in use – mono BTL as well as stereo
- Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	V_P	1,6 to 6,0	V
Total quiescent current (at V_P = 3 V)	I_{tot}	typ. 3,2	mA
Bridge tied load application (BTL)			
Output power at R_L = 32 Ω V_P = 3 V; d_{tot} = 10%	P_o	typ. 140	mW
D.C. output offset voltage between the outputs	$\|\Delta V\|$	max. 70	mV
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 140	μV
Stereo application			
Output power at R_L = 32 Ω d_{tot} = 10%; V_P = 3 V	P_o	typ. 35	mW
d_{tot} = 10%; V_P = 4,5 V	P_o	typ. 75	mW
Channel separation at R_S = 0 Ω; f = 1 kHz	α	typ. 40	dB
Noise output voltage (r.m.s. value) at f = 1 kHz; R_S = 5 kΩ	$V_{no(rms)}$	typ. 100	μV

PACKAGE OUTLINE

8-lead mini-pack; plastic (SO8; SOT96A).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	6	V
Peak output current	I_{OM}	max.	150	mA
Total power dissipation	see derating curve Fig. 1			
Storage temperature range	T_{stg}	−55 to +	150	°C
Crystal temperature	T_c	max.	100	°C
A.C. and d.c. short-circuit duration at V_P = 3,0 V (during mishandling)	t_{sc}	max.	5	s

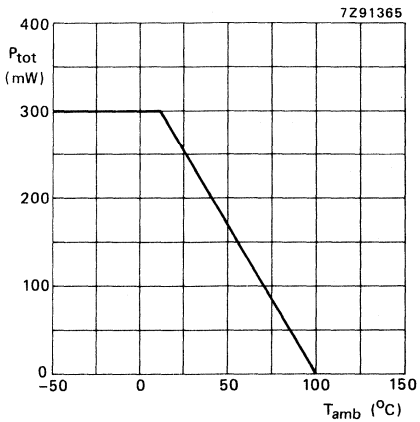


Fig. 1 Power derating curve.

SO PACKAGE DESIGN EXAMPLE

To achieve the small dimension of the encapsulation the SO package is preferred with only 8 pins. Because a heatsink is not applicable, the dissipation is limited by the thermal resistance of the 8-pin SO encapsulation until:

$$\frac{T_{j\ max} - T_{amb}}{R_{th\ j\text{-}a}} = \frac{100-60}{300} = 0{,}1\ W.$$

DEVELOPMENT DATA

CHARACTERISTICS

V_P = 3 V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage	V_P	1,6	–	6,0	V
Total quiescent current	I_{tot}	–	3,2	4	mA
Bridge-tied load application (BTL); see Fig. 4					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	140	–	mW
V_P = 4,5 V; d_{tot} = 10% (R_L = 64 Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	140	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
D.C. output offset voltage (at R_S = 5 kΩ)	$\lvert\Delta V\rvert$	–	–	70	mV
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	1	–	–	MΩ
Input bias current	I_i	–	40	–	nA
Stereo application; see Fig. 5					
Output power*					
V_P = 3,0 V; d_{tot} = 10%	P_o	–	35	–	mW
V_P = 4,5 V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	–	26	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5 kΩ; f = 1 kHz	$V_{no(rms)}$	–	100	–	μV
R_S = 0 Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	μV
Channel separation					
R_S = 0 Ω; f = 1 kHz	α	30	40	–	dB
Input impedance (at R_S = ∞)	$\lvert Z_i\rvert$	2	–	–	MΩ
Input bias current	I_i	–	20	–	nA

* Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

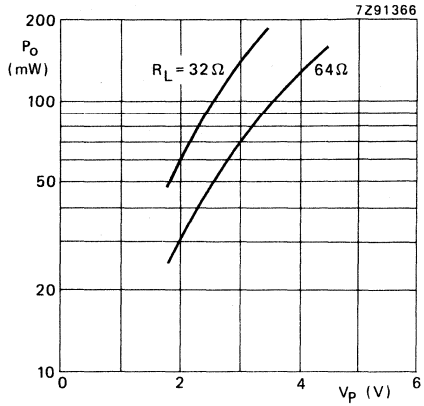


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

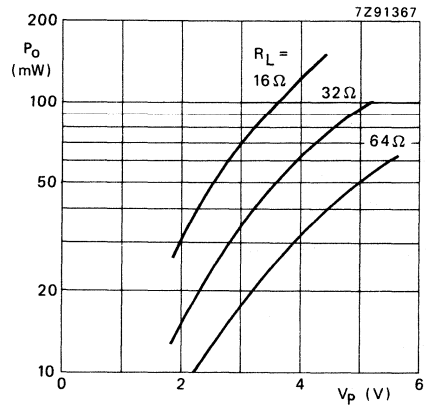


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25 °C.

APPLICATION INFORMATION

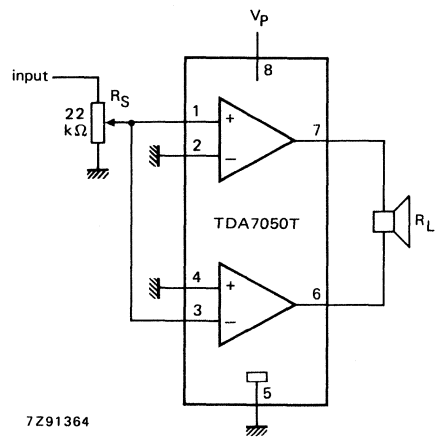


Fig. 4 Application diagram (BTL); also used as test circuit.

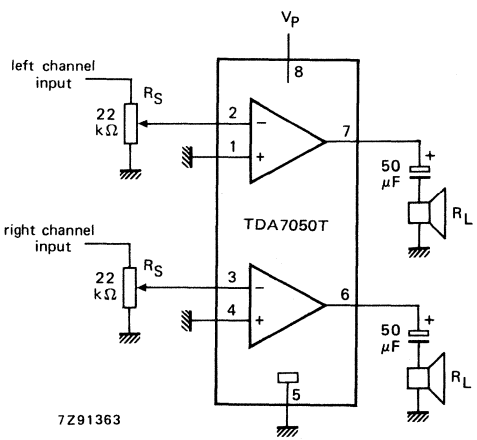


Fig. 5 Application diagram (stereo); also used as test circuit.

1 W BTL MONO AUDIO AMPLIFIER

GENERAL DESCRIPTION

The TDA7052 is a mono output amplifier in a 8-lead dual-in-line (DIL) plastic package. The device is designed for battery-fed portable audio applications.

Features:

- No external components
- No switch-on or switch-off clicks
- Good overall stability
- Low power consumption
- No external heatsink required
- Short-circuit proof

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%; 8 Ω	P_o	–	1,2	–	W
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%

PACKAGE OUTLINE

8-lead DIL; plastic (SOT97).

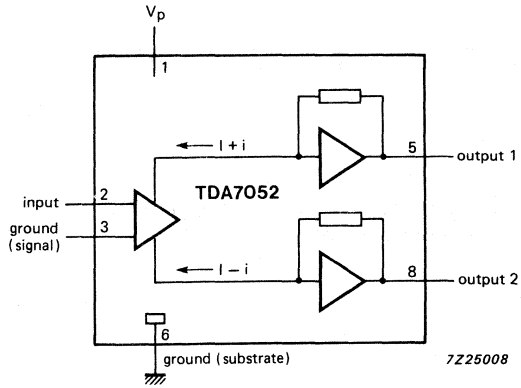


Fig. 1 Block diagram.

PINNING

1	V_P	supply voltage	5	OUT1	output 1
2	IN	input	6	GND2	ground (substrate)
3	GND1	ground (signal)	7	n.c.	not connected
4	n.c.	not connected	8	OUT2	output 2

FUNCTIONAL DESCRIPTION

The TDA7052 is a mono output amplifier designed for battery-fed portable audio applications, such as tape recorders and radios.
The gain is fixed internally at 40 dB. A large number of tape recorders and radios are still designed for mono sound, plus a space-saving trend by reduction of the number of battery cells. This means a decrease in supply voltage which results in an reduction of output power. To compensate for this reduction, the TDA7052 uses the Bridge-Tied-Load principle (BTL) which can deliver an output power of 1,2 W (THD = 10%) into an 8 Ω load with a power supply of 6 V. The load can be short-circuited at each signal excursion.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	V_P	–	18	V
Non-repetitive peak output current	I_{OSM}	–	1,5	A
Total power dissipation	P_{tot}	see Fig. 2		
Crystal temperature	T_c	–	150	°C
Storage temperature range	T_{stg}	–65	+ 150	°C

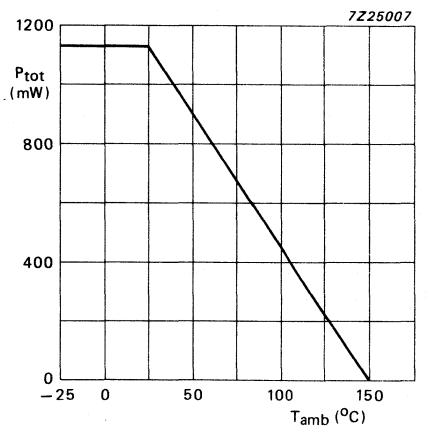


Fig. 2 Power derating curve.

POWER DISSIPATION

Assume V_P = 6 V; R_L = 8 Ω; T_{amb} = 50 °C maximum.

The maximum sinewave dissipation is 0,9 W.

$$R_{th\,j\text{-}a} = \frac{150 - 50}{0{,}9} \approx 110 \text{ K/W}.$$

Where $R_{th\,j\text{-}a}$ of the package is 110 K/W, so no external heatsink is required.

CHARACTERISTICS

V_P = 6 V; R_L = 8 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage range		V_P	3	6	15	V
Total quiescent current	$R_L = \infty$	I_{tot}	–	4	8	mA
Voltage gain		G_v	39	40	41	dB
Output power	THD = 10%	P_o	*	1,2	–	W
Noise output voltage (RMS value)						
	note 1	$V_{no(rms)}$	–	150	300	μV
	note 2	$V_{no(rms)}$	–	60	–	μV
Frequency response		f_r	–	20 Hz to 20 kHz	–	Hz
Supply voltage ripple rejection	note 3	SVRR	40	50	–	dB
DC output offset voltage pin 5 to 8	R_S = 5 kΩ	ΔV_{5-8}	–	–	100	mV
Total harmonic distortion	P_o = 0,1 W	THD	–	0,2	1,0	%
Input impedance		$\|Z_I\|$	–	100	–	kΩ
Input bias current		I_{bias}	–	100	300	nA

Notes to the characteristics

1. The unweighted RMS noise output voltage is measured at a bandwidth of 60 Hz to 15 kHz with a source impedance (R_S) of 5 kΩ.
2. The RMS noise output voltage is measured at a bandwidth of 5 kHz with a source impedance of 0 Ω and a frequency of 500 kHz. With a practical load (R = 8 Ω; L = 200 μH) the noise output current is only 100 nA.
3. Ripple rejection is measured at the output with a source impedance of 0 Ω and a frequency between 100 Hz and 10 kHz. The ripple voltage = 200 mV (RMS value) is applied to the positive supply rail.

* Value to be fixed.

APPLICATION INFORMATION

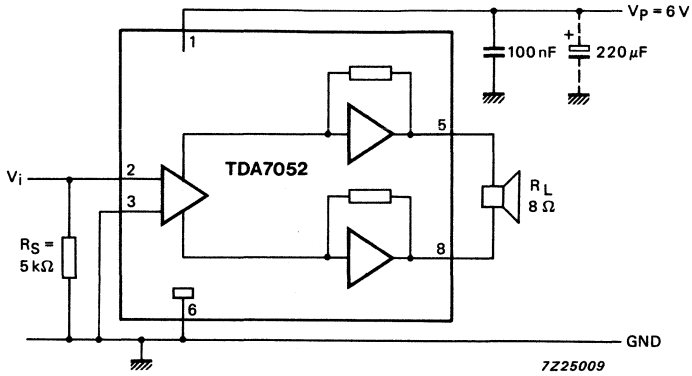


Fig. 3 Application diagram.

DEVELOPMENT DATA

LOW POWER FREQUENCY SYNTHESIZER (LOPSY)

GENERAL DESCRIPTION

The TDD1742T is a low power, high-performance frequency synthesizer in local oxidation CMOS (LOCMOS) technology. The device is designed for use in channelized VHF/UHF applications especially portable and mobile radios.

The circuit incorporates many of the features of the HEF4750V (frequency synthesizer) and HEF4751 (universal divider), including a high-gain phase comparator together with an on-chip sample-and-hold capacitor and phase modulator.

A multiplexed or bus-structured programming sequence allows interface to a microcontroller or external memory (ROM/PROM); power is applied to the memory only when it is required for programming via additional on-chip circuitry.

Operation is possible with a minimum supply voltage of 7 V and a maximum input frequency of 8,5 MHz.

Encapsulation in a 28-lead mini-pack enables the construction of small, low power consumption synthesizers with low noise performance and high side-band attenuation.

Features

- On-chip sample-and-hold capacitor
- Low power consumption
- High-gain phase comparator with low levels of noise and spurious outputs
- Auxiliary digital phase comparator for fast locking
- On-chip phase modulator
- Simple interfacing to external memory
- Microcontroller compatible
- Power-on reset circuitry

QUICK REFERENCE DATA

Supply voltage ranges		
pin 14	$V_{DD1} = V_{14\text{-}6}$	7 to 10 V
pin 8	$V_{DD2} = V_{8\text{-}6}$	4,5 to 5 V
pin 1	$V_{DD3} = V_{1\text{-}6}$	7 to 10 V
Supply current		
(at T_{amb} = 25 °C; $V_{DD1} = V_{DD3}$ = 7,4 V; V_{DD2} = 5 V)		
pin 14 (phase modulator OFF)	$I_{DD1} = I_{14}$	max. 1,5 mA
pin 8	$I_{DD2} = I_8$	max. 100 μA

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

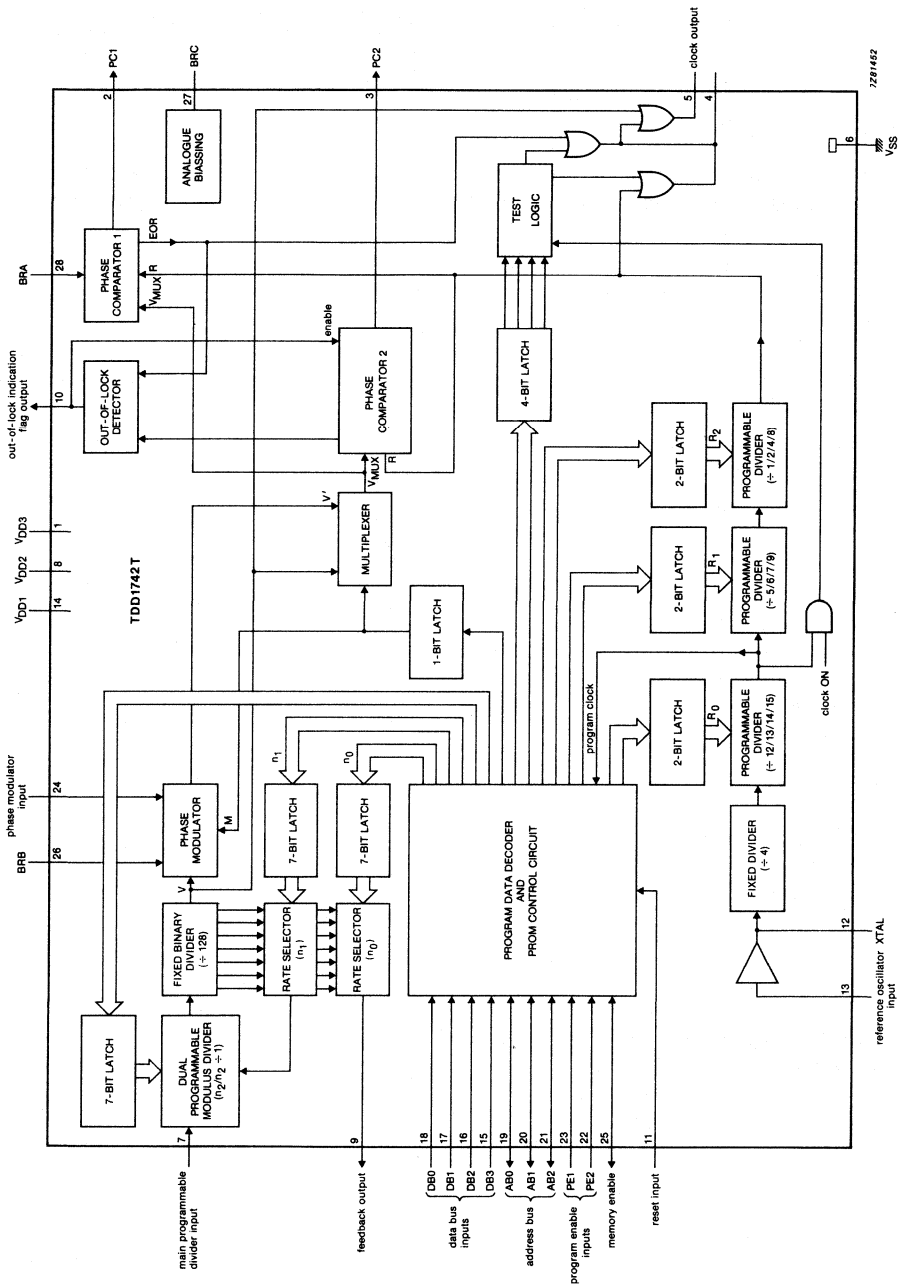


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

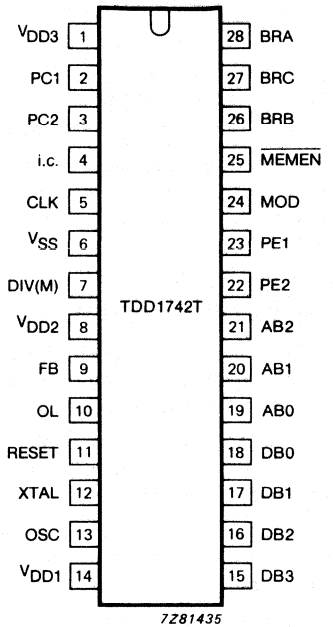


Fig. 2 Pinning diagram.

Pin functions

pin no.	mnemonic	description
1	V_{DD3}	**Power Supply 3:** analogue supply voltage (7 to 10 V).
2	PC1	**Phase Comparator 1:** high-gain analogue phase comparator output which is used when the system is in-lock to give low levels of noise and spurious outputs.
3	PC2	**Phase Comparator 2:** low-gain digital phase comparator 3-state output which enables the achievement of fast lock times when the system is initially out-of-lock. Phase comparator 2 is inhibited when the phase is within the locking range of phase comparator 1.
4	i.c.	**internally connected** (must be left floating).
5	CLK	**Clock:** clock output.
6	V_{SS}	**Ground:** circuit earth potential.
7	DIV(M)	**Divider:** input to the main programmable divider (8,5 MHz max.), usually from prescaler.
8	V_{DD2}	**Power Supply 2:** supply voltage for TTL-compatible stages (+ 5 V ± 10%).
9	FB	**Feedback:** feedback output to control the modulus of the external prescaler.
10	OL	**Out-of-lock:** out-of-lock indication flag output. This output is HIGH when phase comparator 2 is in operation (when the system is out-of-lock).
11	RESET	**Power-on-Reset:** Following power up an initial pulse is applied to this input pin to set the internal counters.

Pin functions (continued)

pin no.	mnemonic	description
12	XTAL	**Crystal:** output to external crystal to form the oscillator circuit in combination with the OSC input. Alternatively this pin may be used as a buffer output.
13	OSC	**Oscillator:** input to reference oscillator which together with the XTAL output and an external crystal is used to generate the reference frequency. Alternatively to OSC input may be used as a buffer amplifier for an external reference oscillator.
14	V_{DD1}	**Power Supply 1:** digital supply voltage (7 to 10 V).
15-18	DB3-DB0	**Data Bus:** Data Bus inputs (TTL compatible).
19-21	AB0-AB2	**Address Bus:** TTL compatible bidirectional address bus. Provides address output to an external memory or input from microcontroller. The outputs are 3-state with internal pull-downs.
22	PE2	**Program Enable 2:** TTL compatible inputs to initiate the programming cycle or strobe the internal data latches.
23	PE1	**Program Enable 1:**
24	MOD	**Modulator:** high impedance linear phase modulator input, which applies a voltage controlled delay to the programmable divider output to the phase comparator.
25	$\overline{\text{MEMEN}}$	**Memory Enable:** mode control and memory enable bidirectional pin. If pin 25 is LOW at general reset the TDD1742T is set to the microcontroller mode; if pin 25 is HIGH at general reset the TDD1742T is set to the memory mode and the ROM/PROM is enabled.
26	BRB	**Bias Resistor B:** current mirror which acts as gain control for the phase modulator.
27	BRC	**Bias Resistor C:** current mirror pin which provides analogue biassing.
28	BRA	**Bias Resistor A:** current mirror pin which acts as gain control for phase comparator 1.

FUNCTIONAL DESCRIPTION

Reference oscillator chain

The reference oscillator chain comprises a crystal oscillator and dividers to give the required frequency to drive the phase comparators.
The oscillator stage is a single inverter connected between pin 12 (XTAL) and pin 13 (OSC). Satisfactory operation is achieved with crystals up to 9 MHz. Alternatively, the OSC input may be used as a buffer amplifier for an external reference oscillator.
The reference divider chain comprises a fixed divide by 4-stage followed by three cascaded programmable dividers of ratios ÷ 12/13/14/15, ÷ 5/6/7/9 and ÷ 1/2/4/8. The output of the last stage is applied as one input (R) to the two phase comparators. Thus a number of division ratios between 240 and 4320 are possible which provides all the required VHF and UHF channel spacings with reference crystals in a 1 to 9 MHz range.

Main programmable divider

The main programmable divider is a rate feedback binary divider. As shown in figure 1 it comprises a fixed 7-bit binary divider (÷ 128) and two rate selectors (n_1 and n_0). One rate selector controls a 7-bit fully programmable dual modulus divider (÷ $n_2/n_2 + 1$) and the other controls the external dual modulus prescaler (÷ A/A + 1).

The overall division rate (N) is given by:

$N = (128\ n_2 + n_1)\ A + n_0$

Where:

$0 \leqslant n_0 \leqslant 127$
$0 \leqslant n_1 \leqslant 127$
$1 \leqslant n_2 \leqslant 127.$

The output from the programmable divider is fed to the phase comparators via the phase modulator and the multiplexer. The phase modulator is bypassed if not selected.

DEVELOPMENT DATA

Phase comparison

The TDD1742T contains 2 phase comparators which act in close co-operation. Phase comparator 1 is the main comparator. It is designed to have a high-gain analogue output, 4500 volts/cycle at 10 kHz (typ.). This enables a low noise performance to be achieved. However, the output of phase comparator 1 will saturate at high or low levels for very small phase excursions.
Phase comparator 2 is an auxiliary comparator with a wide range, which enables faster lock times to be achieved than otherwise would be possible. This digital phase comparator has a linear $\pm 2\pi$ radians phase range, which corresponds to a gain of $\frac{V_{DD}}{2}$ volts/cycle.

To avoid degrading the noise performance of the system by the relatively low gain of phase comparator 2, once a small phase error has been achieved an internal switch disconnects phase comparator 2, leaving only phase comparator 1 connected. Thus the low noise properties of phase comparator 1 are obtained once phase-lock has been achieved.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 1 (see Fig. 3)

Phase comparator 1 is comprised of a linear ramp generator and a sample and hold circuit.

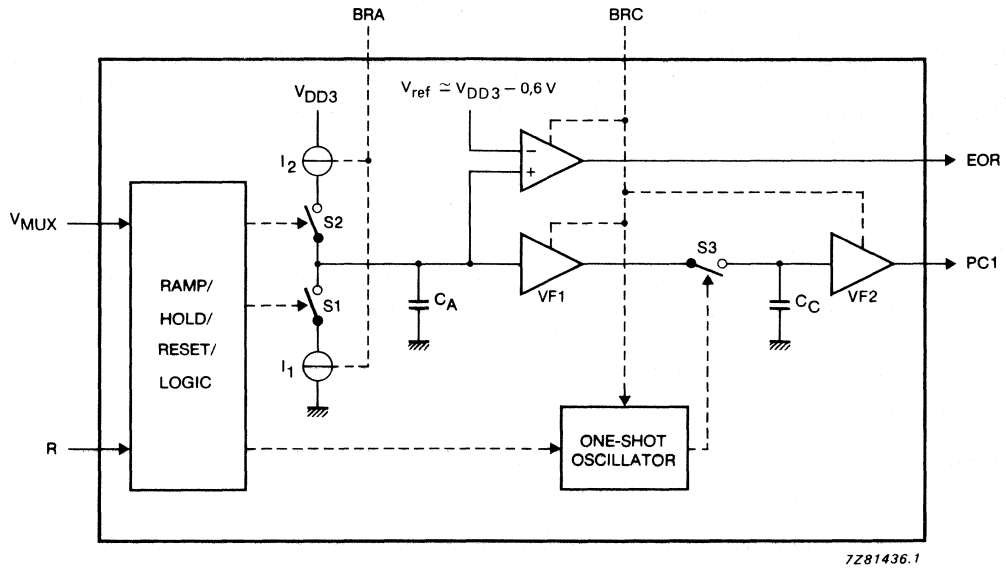


Fig. 3 Simplified block diagram of phase comparator 1.

A negative-going transition at the V_{MUX} input causes the hold capacitor C_A to be discharged via switch S1 and constant current source I_1.
A positive-going transition at the V_{MUX} input causes the hold capacitor C_A to be charged via switch S2 and constant current source I_2, which produces a linear ramp.
A negative-going transition at the R input terminates the linear ramp.
Capacitor C_A holds the voltage that the ramp has attained, and is buffered by the voltage follower VF1. After the output of VF1 is stable (2 μs), the sample switch S3 is closed for approximately 1 μs by the one-shot oscillator. This enables the capacitor C_C to charge to the voltage level of VF1 and in turn buffered by voltage follower VF2 made available at output PC1.
The construction and small duty cycle of the sample switch S3 provides a low hold step, resulting in a minimum side-band level.
If the linear ramp terminates before a negative-going transition at the R input is present, an end of ramp (EOR) signal is produced, generating in turn an out-of-lock (OL) signal. OL enables phase comparator 2 via the out-of-lock detector.

These actions are illustrated in the waveforms of Fig. 4 and Fig. 5.

The gain of phase comparator 1 as measured at PC1 is given by:

$$\text{PC gain} \simeq \frac{446\ I_{BRA}}{F_R}$$

Where:

I_{BRA} is in μA
F_R is the phase comparator reference frequency in kHz

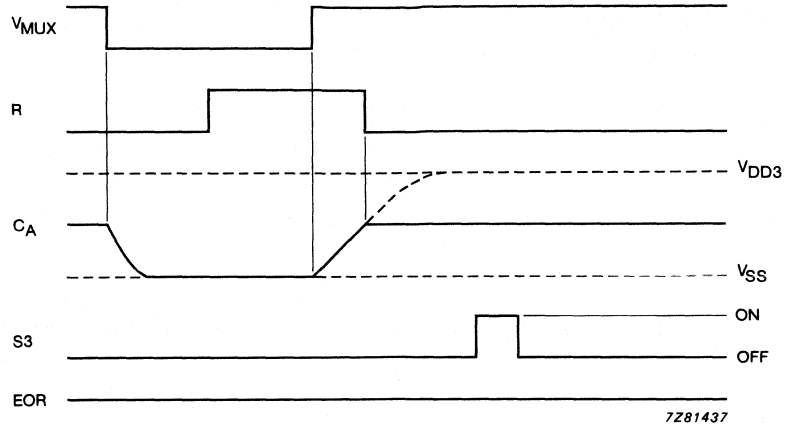


Fig. 4 Waveforms of phase comparator 1; in-lock condition.

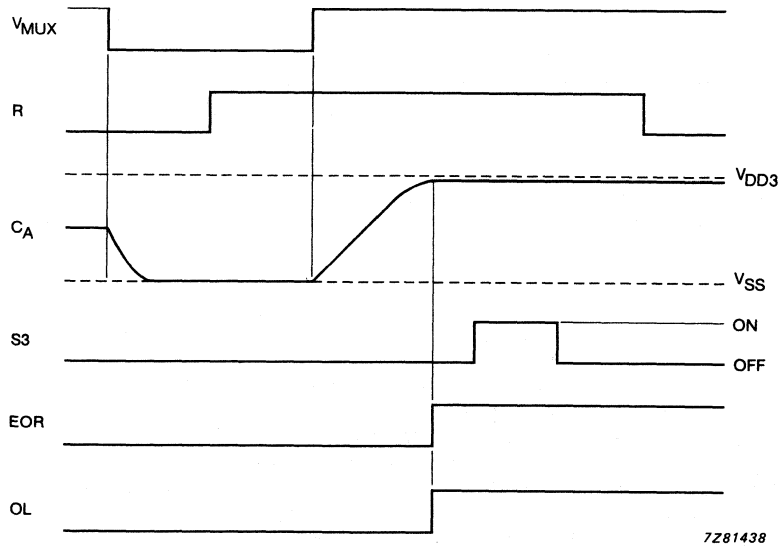


Fig. 5 Waveforms of phase comparator 1; out-of-lock condition.

When V_{MUX} leads R the output signal at pin 2 (PC1) is proportional to the phase difference (in-lock condition) or HIGH (out-of-lock condition).
When R leads V_{MUX} the output signal at pin 2 (PC1) remains LOW.

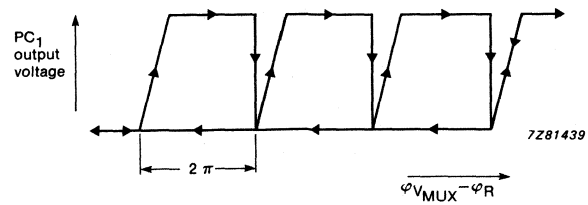


Fig. 6 Phase characteristic of output PC1.

FUNCTIONAL DESCRIPTION (continued)

Phase comparator 2 (see Fig. 7)

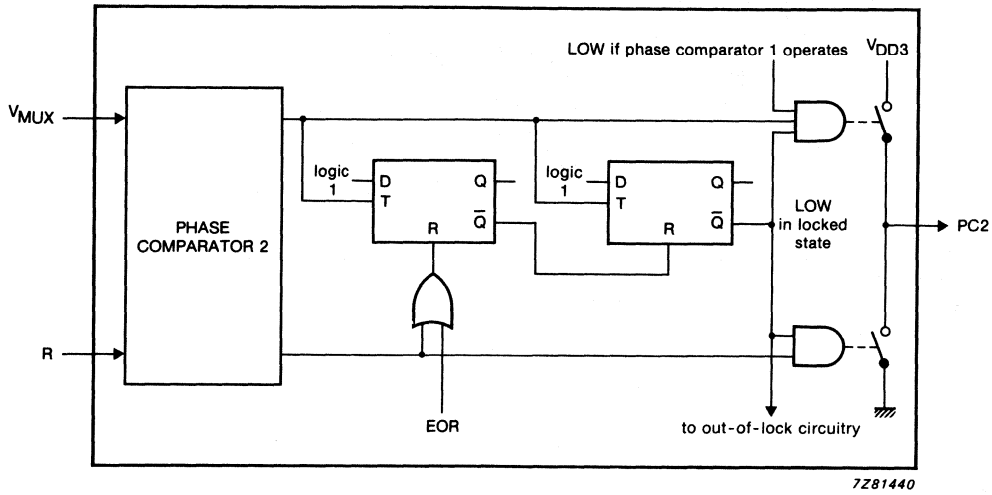


Fig. 7 Simplified block diagram of phase comparator 2.

The digital phase comparator (PC2) has three stable states:

- Reset
- V_{MUX} leads R
- R leads V_{MUX}

Table 1 Phase comparator 2: stable states and corresponding output levels

state	V_{MUX} leads R	R leads V_{MUX}
reset	0	0
V_{MUX} leads R	1	0
R leads V_{MUX}	0	1

Transition from one state to another takes place on command of either an active V_{MUX}-edge or an active R-edge as shown in Fig. 8.

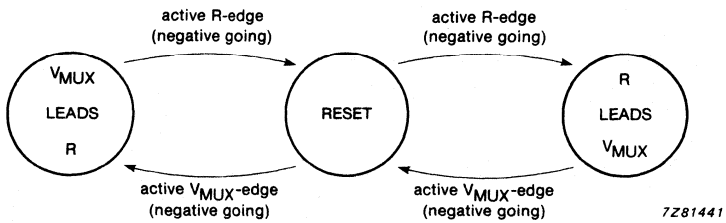


Fig. 8 Transition of state; phase comparator 2.

The output of phase comparator 2 produces positive or negative going pulses with variable width, dependent on the phase relationship of R and V_{MUX}.
The average output voltage is a linear function of the phase difference. Output at pin 3 (PC2) remains in the high impedance OFF-state in the region in which phase comparator 1 operates

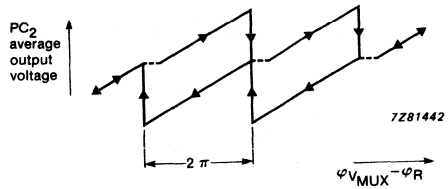


Fig. 9 Phase characteristic of output PC2.

To reach the reset state of phase comparator 2 it is necessary to apply:

- $2V_{MUX}$ + R*
  or
- 2R + V_{MUX}

Thus to achieve the R leads V_{MUX} state 2R must be applied; to achieve the V_{MUX1} leads R state $2V_{MUX}$ must be applied.

DEVELOPMENT DATA

Out-of-lock function

There are several situations when the system goes from the locked to the out-of-lock state (OL output goes HIGH):

- V_{MUX} leads R, however out of the range of phase comparator 1
- R leads V_{MUX}
- R-pulse is missing
- V_{MUX}-pulse is missing

In the first three situations the locked state can be reset by applying two successive cycles within the range of phase comparator 1.
In the fourth situation the locked state can be reset by applying a V_{MUX} pulse followed by two successive cycles within the range of phase comparator 1.

Phase modulator (see Fig. 10)

The linear phase modulator applies a voltage controlled delay to the signal from the programmable divider to the phase comparator input. The gain of the phase modulator is adjustable via an external bias resistor (BRB) which is connected between pin 26 and ground.
The time delay introduced into the V path to the phase modulator is:

$$\frac{909}{I_{BRB}} \text{ ns/volt of input applied to pin 24 (MOD)}$$

When a positive-going transition appears at the V-input, the D type flip-flop produces a HIGH V' level and causes capacitor C_B to produce a positive-going ramp via switch S1 and constant current source I_1 starting at the V_{SS} potential. When the ramp has reached a value equal to the modulation input voltage (at MOD), the comparator resets the D type flip-flop, which terminates the V pulse. C_B now discharges to V_{SS} via switch S1 and constant current source I_2 and the circuit returns to the start position. Because the trailing edge of the V' pulse is the active edge for the phase comparators, a linear phase modulation is achieved. The associated waveforms are shown in Fig. 11. The phase modulator can be switched OFF, via the programming logic, to avoid superfluous dissipation. To achieve, this the M signal must be programmed to logic 0. The V pulse will then be connected via switch S2 to V_{MUX}.

* This means apply two successive active V_{MUX} edges followed by one active R edge.

FUNCTIONAL DESCRIPTION (continued)

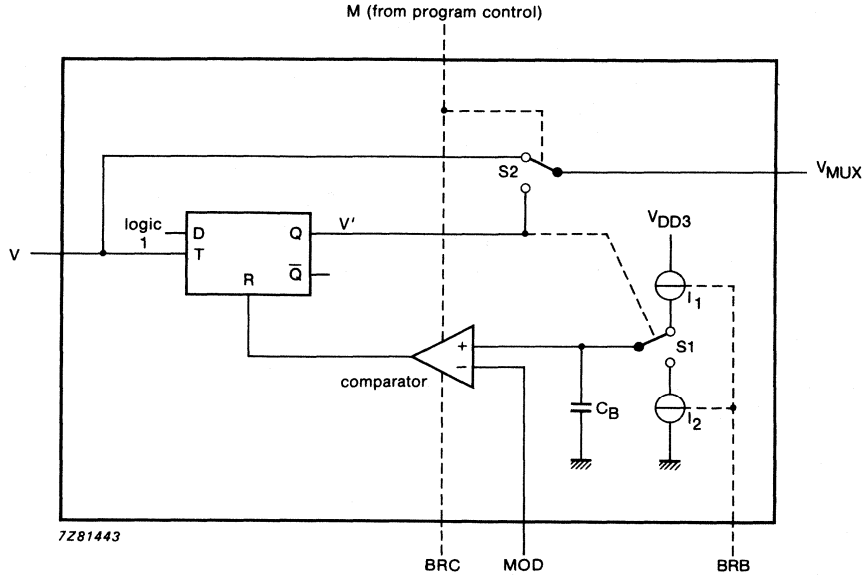


Fig. 10 Simplified block diagram of the phase modulator.

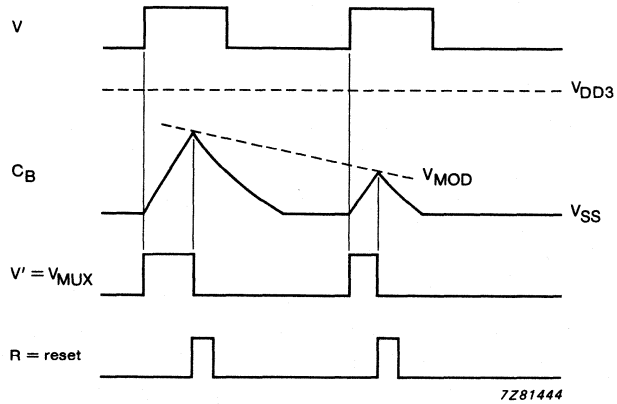


Fig. 11 Phase modulator waveforms; M = 1.

Program control

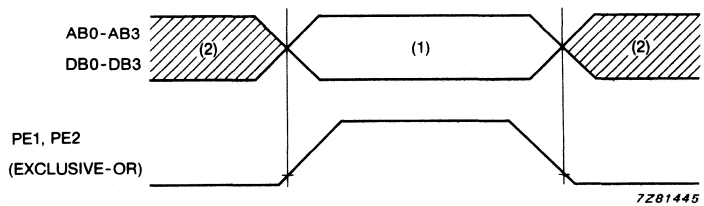
A multiplexed or bus structured sequence allows the TDD1742T to be interfaced to a microcontroller or a PROM.
The device is fully programmable in terms of:

- 6 bits to define the reference divider ratio
- 21 bits to define the main divider ratio
- 1 bit to switch the modulator
- 4 bits to determine the test status

Thus the TDD1742T is programmed with a total of 32 bits which are organized as eight 4-bit words. The address bus is 3 bits wide and the data bus is 4 bits wide. Both buses are TTL compatible. The data words are described in detail in Tables 3 to 7.

Microcontroller mode

If pin 25 ($\overline{\text{MEMEN}}$) is LOW at general reset, the device is set to the micro-controller mode. In this mode a 7-bit word, comprised of 3 address bits (AB0 to AB2) and 4 data bits (DB0 to DB3), may be strobed into the TDD1742T when the program enable pins PE1 and PE2 are set to opposite state (EXCLUSIVE -OR condition; see Fig. 12 and Table 2). One frame of 8 words is necessary to completely program the TDD1742T. Incoming data is not clocked into the internal counter latches until after the receipt of data corresponding to address 111. Upon subsequent reprogramming it is not necessary to change all eight words but a reprogramming sequence must always finish with the data corresponding to address 111.



(1) Address and data valid.
(2) Address and data not valid.

Fig. 12 Waveforms for program enable function; microcontroller mode.

Table 2 Truth table for program enable function; microcontroller mode

PE1	PE2	load
0	0	NO
1	0	YES
0	1	YES
1	1	NO

Program control (continued)

Memory mode (PROM)

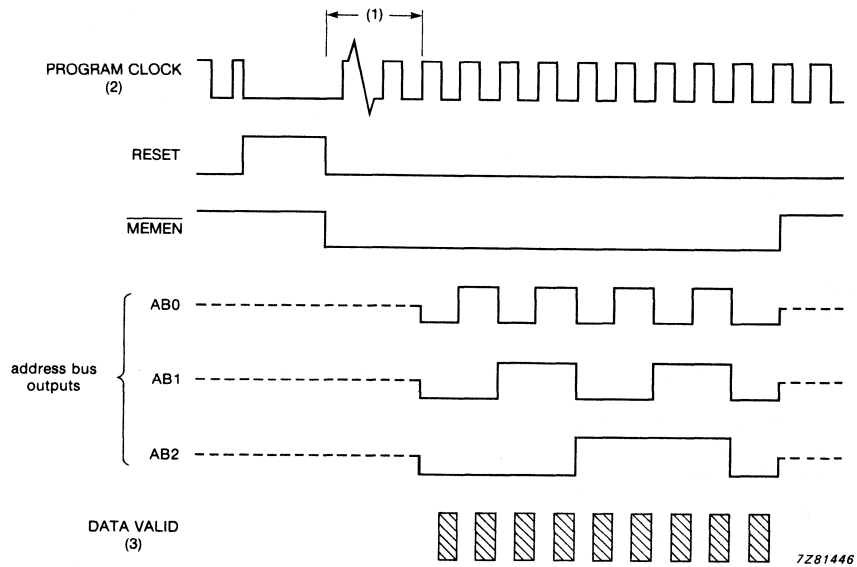
If pin 25 ($\overline{\text{MEMEN}}$) is HIGH at general reset, TDD1742T is set to the memory mode and a programming cycle is initiated. Subsequent reprogramming is performed by applying a pulse to program enable PE1 (pin 23) or PE2 (pin 22). If PE1 is LOW, programming will occur on the LOW-to-HIGH transition of PE2. If PE1 is HIGH, programming will occur on the HIGH-to-LOW transition of PE2. PE1 and PE2 are interchangeable. Reprogramming will also occur by applying a pulse to RESET (pin 11).

At the start of a programming sequence pin 25 goes LOW and may be used to apply power to the memory via an external driver. After a settling time the address bus outputs 000 followed by the remaining seven addresses. During the second half of each address period data, from the memory is latched into the TDD1742T so that the access time of the PROM is not critical.

Note

The program clock is derived from the reference divider chain and its frequency equals $f_{OSC}/4R_0$.

After the full 32 bits have been read the address returns to address 000 before going 3-state. This step transfers data from the internal data latches to the appropriate divider latches. Pin 25 now returns to a high impedance state and power is removed from the memory. Fig. 13 shows the timing for a reset initiated programming sequence; the timing is similar for program enable initiated sequence.



(1) Delay time for PROM settling.
(2) The program clock is derived from the reference divider chain.
(3) Data is valid during the shaded period.

Fig. 13 Timing diagram for TDD1742T PROM control.

Data memory maps

Table 3 Bit programming of the eight 4-bit words

address			data			
AB2	AB1	AB0	DB3	DB2	DB1	DB0
0	0	0	see Table 4			
0	0	1	$n_0 3$	$n_0 2$	$n_0 1$	$n_0 0$
0	1	0	$R_0 0$	$n_0 6$	$n_0 5$	$n_0 4$
0	1	1	$n_1 3$	$n_1 2$	$n_1 1$	$n_1 0$
1	0	0	$R_0 1$	$n_1 6$	$n_1 5$	$n_1 4$
1	0	1	$n_2 3$	$n_2 2$	$n_2 1$	$n_2 0$
1	1	0	M	$n_2 6$	$n_2 5$	$n_2 4$
1	1	1	$R_2 1$	$R_2 0$	$R_1 1$	$R_1 0$

In Table 3

n_0, n_1 and n_2 comprises the main programmable divider.

$n_0 0$ is the LSB of n_0, $n_0 6$ the MSB and so forth.

If M is 1 the modular is ON.

Table 4 Memory map for address 000

DB3	DB2	DB1	DB0	program clock to output CLK	mode
0	0	X	X	yes	idle
0	1	0	0	no	idle
all other combinations				not defined	not defined

Where

X = don't care.

For optimum performance (minimum crosstalk) 0100 should be programmed into address 000.

Memory maps (continued)

Table 5 Reference divider control; part 1

R_01	R_00	division ratio
0	0	12
0	1	13
1	0	14
1	1	15

In Table 5:

R_00 and R_01 control the ÷ 12/13/14/15 portion of the reference divider.

Table 6 Reference divider control; part 2

R_11	R_10	division ratio
0	0	9
0	1	5
1	0	6
1	1	7

In Table 6:

R_10 and R_11 control the ÷ 5/6/7/9 portion of the reference divider.

Table 7 Reference divider control; part 3

R_21	R_20	division ratio
0	0	1
0	1	2
1	0	4
1	1	8

In Table 7:

R_20 and R_21 control the ÷ 1/2/4/8 portion of the reference divider.

Current biassing

Current biassing is provided by 3 external bias resistors A, B and C.

Bias Resistor A: is connected between pin 28 (BRA) and ground. The value of the resistor must be such that I_{BRA} = 20 μA, which acts as gain control for analogue phase comparator 1.
Bias Resistor B: is connected between pin 26 (BRB) and ground. The value of the resistor must be such that I_{BRB} = 3 to 25 μA, which acts as gain control for the phase modulator.
Bias Resistor C: is connected between pin 27 (BRC) and ground. The value of the resistor must be such that I_{BRC} = 5 to 30 μA, which provides biassing for the remainder of the analogue circuitry.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges			
pin 14	V_{DD1}		−0,5 to + 15 V
pin 8	V_{DD2}		−0,5 to + 15 V
pin 1	V_{DD3}		−0,5 to + 15 V
Voltage on any input	V_I		−0,5 to V_{DD1} + 0,5 V
Relative supply voltage	V_{DD2}-V_{DD1}	max.	0,5 V
Relative supply voltage	V_{DD3}-V_{DD1}	max.	0,5 V
D.C. current into any input or output	± I	max.	10 mA
Power dissipation per package for T_{amb} = 0 to + 85 °C	P_{tot}	max.	400 mW
Power dissipation per output for T_{amb} = 0 to + 85 °C	P_O	max.	100 mW
Storage temperature range	T_{stg}		−65 to 150 °C
Operating ambient temperature range	T_{amb}		−40 to 85 °C

DEVELOPMENT DATA

D.C. CHARACTERISTICS

$V_{DD1} = V_{DD3} = 7{,}4$ V; $V_{DD2} = 5$ V; $V_{SS} = 0$ V; $T_{amb} = 25$ °C unless otherwise specified; for definitions see note 1.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage					
pin 14	V_{DD1}	7	–	10	V
pin 8	V_{DD2}	4,5	–	5	V
pin 1	V_{DD3}	7	–	10	V
Supply current					
pin 14 (phase modulator OFF)	I_{DD1}	–	–	1,5	mA
pin 8	I_{DD2}	–	–	100	μA
pin 1 (phase modulator OFF)	I_{DD3}	–	–	1,5	mA
Input leakage current (notes 2 and 3)					
logic inputs, MOD	$\pm I_{LI}$	–	–	300	nA
Output leakage current (notes 2 and 3)					
at ½ V_{DD}					
PC2 high impedance OFF state	$\pm I_{LO}$	–	–	50	nA
$\overline{\text{MEMEN}}$ high impedance state	$\pm I_{LO}$	–	–	1,6	μA
I/O current					
AB0 to AB2 high impedance state	$I_{I/O}$	5	–	30	μA
Logic input voltage LOW					
CMOS inputs; CMOS I/Os	V_{IL}	–	–	$0{,}3V_{DD1}$	V
TTL inputs; TTL I/Os	V_{IL}	–	–	0,8	V
Logic input voltage HIGH					
CMOS inputs; CMOS I/Os	V_{IH}	$0{,}7V_{DD1}$	–	–	V
TTL inputs; TTL I/Os	V_{IH}	2	–	–	V
Logic output voltage LOW (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OL}	–	–	50	mV
Logic output voltage HIGH (note 2)					
at $\lvert I_O \rvert < 1$ μA	V_{OH}	V_{DD1}-50	–	–	mV

parameter	symbol	min.	typ.	max.	unit
Logic output voltage LOW (note 2)					
$\overline{\text{MEMEN}}$ at I_{OL} = 4 mA	V_{OL}	–	–	1	V
PC2 at I_{OL} = 1,5 mA	V_{OL}	–	–	0,5	V
CLK; OL at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
XTAL at I_{OL} = 3 mA	V_{OL}	–	–	0,5	V
FB at I_{OL} = 1 mA	V_{OL}	–	–	0,5	V
AB0; AB1; AB2 at I_{OL} = 0,2 mA	V_{OL}	–	–	0,4	V
Logic output voltage HIGH (notes 2 and 3)					
PC2 at $-I_{OH}$ = 1,5 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
CLK; OL at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD1}-0,5$	–	–	V
XTAL at $-I_{OH}$ = 3 mA	V_{OH}	$V_{DD1}-1$	–	–	V
FB at $-I_{OH}$ = 1 mA	V_{OH}	$V_{DD2}-1$	–	–	V
AB0; AB1 at I_{OH} = 0,2 mA	V_{OH}	2,4	–	–	V
AB2 at I_{OH} = 0,8 mA	V_{OH}	2,4	–	–	V
Output PC1					
sink current (notes 2, 3 and Fig. 15)	I_O	1	–	–	mA
source current (notes 2, 3 and Fig. 16)	$-I_O$	1	–	–	mA
Internal resistance of phase comparator 1 (notes 2 and 3) locked state |output swing| $<$ 200 mV specified output range: $0,5\ V_{DD}-0,5$ V to $0,5\ V_{DD}+0,5$ V	R_i	–	2,0	–	Ω

DEVELOPMENT DATA

A.C. CHARACTERISTICS

A dynamic specification is given for the circuit, built-up with external components as shown in Fig. 14, under the following conditions; for definitions see note 1; V_{DD} = 7,4 ± 0,4 V; T_{amb} = 25 °C; input transition times ⩽ 40 ns; $C_A = C_B = C_C$ = 10 nF; R_A chosen so that I_{RA} = 20 μA ± 1 μA; R_B chosen so that I_{RB} = 3 to 25 μA; R_C chosen so that I_{RC} = 5 to 30 μA; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Main programmable divider (DIV(M); pin 7)					
input frequency all divider ratios (square wave input)	$f_{DIV(M)}$	8,5	–	–	MHz
Reference divider					
input frequency all divider ratios (square wave input)	$f_{DIV(R)}$	9	–	–	MHz
Oscillator frequency (OSC; pin 13)	f_{OSC}	9	12	–	MHz
Input capacitance					
DIV(M); OSC	C_I	–	–	3	pF
DB0 to DB3; PE1; PE2; AB0 to AB2	C_I	–	–	5	pF
Propagation delay (see Fig. 17)					
Feedback output to external prescaler					
DIV(M) → FB at C_L = 10 pF					
HIGH to LOW*	t_{PHL}	–	35	70	ns
LOW to HIGH*	t_{PLH}	–	35	70	ns
Average power supply current (notes 3 and 4)					
in-lock state	I_{DD1}	–	2	–	mA
	I_{DD2}	–	0,15	–	mA
	I_{DD3}	–	0,45	–	mA

* Measured from 30% point of negative-going edge at DIV(M) to 50% point of either output edge of FB.

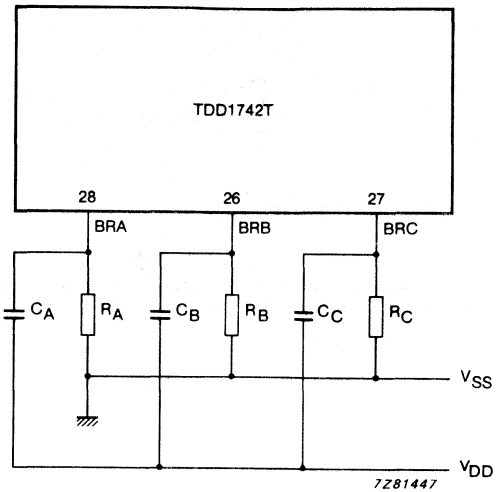


Fig. 14 Test circuit for measuring a.c. characteristics.

DEVELOPMENT DATA

Notes to the characteristics

1. Definitions:
   R_A = external biassing resistor between pins BRA and V_{SS}.
   R_B = external biassing resistor between pins BRB and V_{SS}.
   R_C = external biassing resistor between pins BRC and V_{SS}.
   C_A = decoupling capacitor between pins BRA and V_{DD}.
   C_B = decoupling capacitor between pins BRB and V_{DD}.
   C_C = decoupling capacitor between pins BRC and V_{DD}.
   CMOS logic inputs: RESET, OSC.
   CMOS logic outputs: PC2, CLK, OL, XTAL.
   CMOS logic I/O: $\overline{\text{MEMEN}}$.
   TTL logic inputs: DB0 to DB3, PE2, PE1.
   TTL logic output: FB.
   TTL logic I/O: AB0 to AB2.
   Analogue inputs: DIV(M), MOD.
   Analogue output: PC1.
   Analogue biassing pins: BRA, BRB, BRC.
2. All logic inputs at V_{SS} or V_{DD}.
3. R_A connected; its value chosen such that $I_{BRA} = 20\ \mu A$.
   R_B connected; its value chosen such that $I_{BRB} = 20\ \mu A$.
   R_C connected; its value chosen such that $I_{BRC} = 20\ \mu A$.
4. Average power supply current measured at:
   f_{OSC} = 5 MHz, external clock, divider ratio 420;
   $f_{DIV(M)}$ = 2 MHz, divider ratio 168.

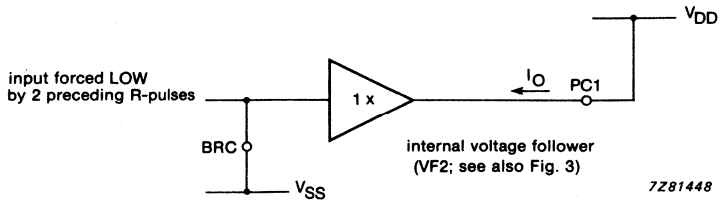


Fig. 15 Equivalent circuit for output PC1 sink current.

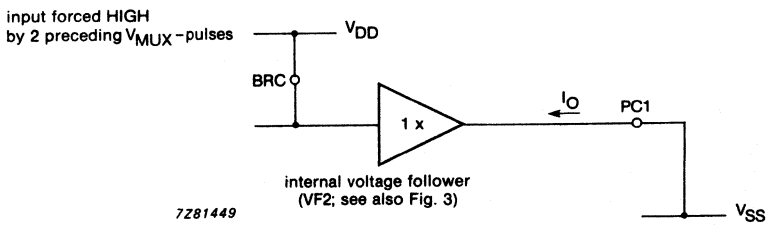


Fig. 16 Equivalent circuit for output PC1 source current.

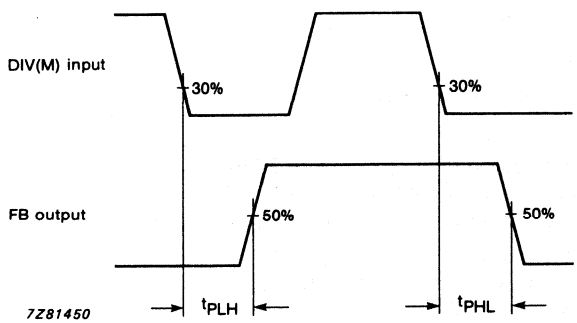


Fig. 17 Waveforms showing propagation delay; DIV (M) → FB.

APPLICATION INFORMATION

Fig. 18 shows a typical application circuit using the TDD1742T in the memory mode with the following design parameters:

Frequency range	150 to 155 MHz
VCO sensitivity	1 MHz/V
Reference frequency	12,5 kHz
Prescaler	÷ 80/81
Reference crystal frequency	5,25 MHz
Reference divider chain	÷ 15; ÷ 7; ÷ 1
Total division ratio	12000 to 12400
Loop bandwidth	300 Hz

DEVELOPMENT DATA

APPLICATION INFORMATION (continued)

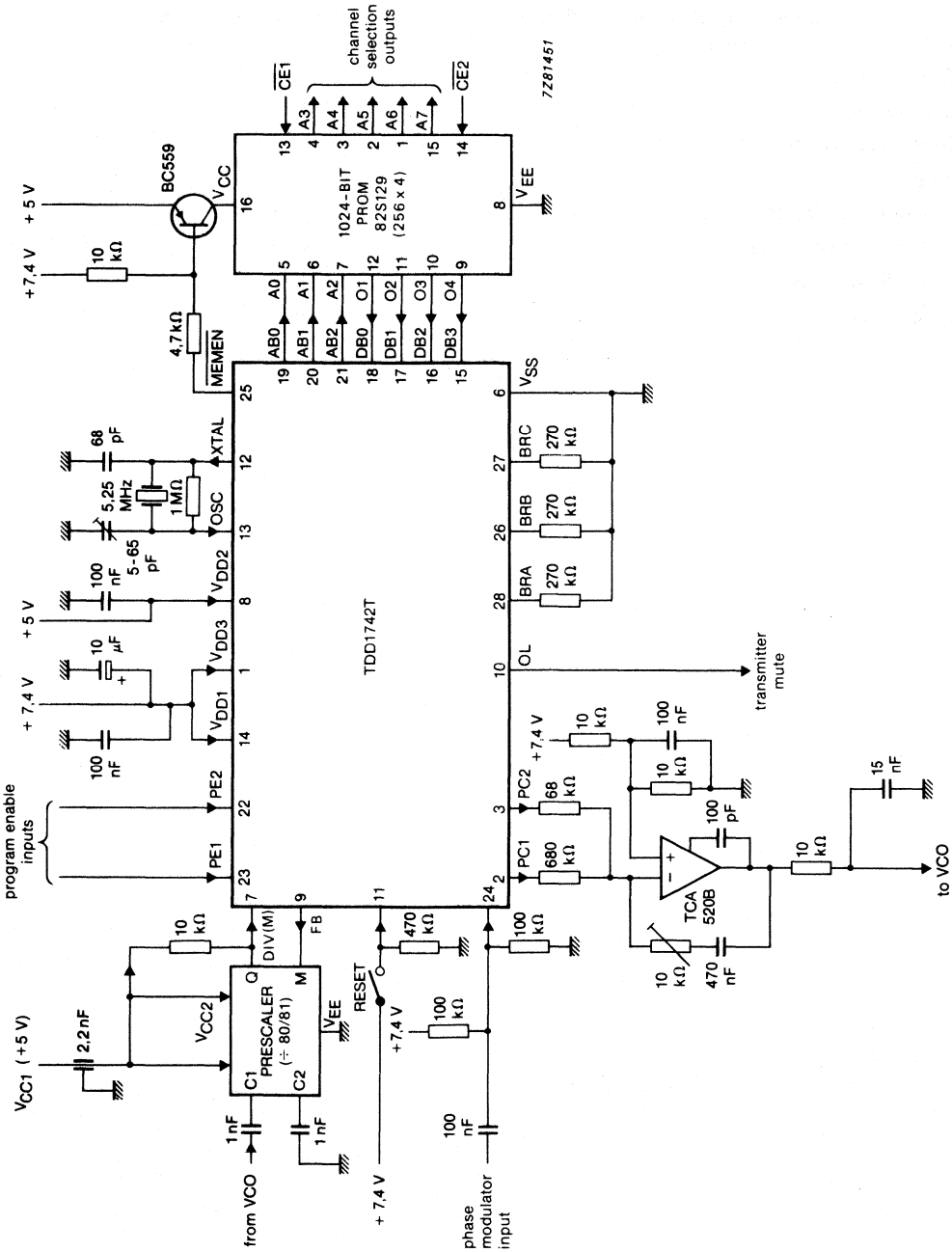


Fig. 18 Typical application circuit using the TDD1742T in memory mode.

LOW POWER DIGITAL PAGING RECEIVER

GENERAL DESCRIPTION

The UAA2033T is a very low power radio receiver circuit for use in VHF paging receivers (30 to 174 MHz) of wide-area digital paging systems employing direct FM non-return-to-zero (NRZ) frequency-shift keying (FSK) modulation.

Used in conjunction with the PCA5000T decoder for POCSAG paging systems, it offers an extremely advanced radio paging concept.

The receiver design is based on the offset receiver principle which gives improved performance, lower power consumption and requires less external components than the two-branch type of receiver architecture found in presently available ICs. The receiver provides fully filtered and squared data to drive the decoder device and can be turned off completely by external inputs.

Features

- Wide operating supply voltage range
- Low current consumption
- Fully compatible with world-wide POCSAG paging systems
- Receiver power externally addressable
- High sensitivity
- Low battery voltage detector
- Uses low cost crystal
- Automatically tracks offsets in the input frequency

QUICK REFERENCE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{14-15}$	2,0	2,7	3,5	V
Supply current		I_{14}	2,2	2,7	3,3	mA
Sensitivity	10^{-2} bit error rate	EMF/2	–	–	0,3	μV
Operating ambient temperature range		T_{amb}	−10	–	+70	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

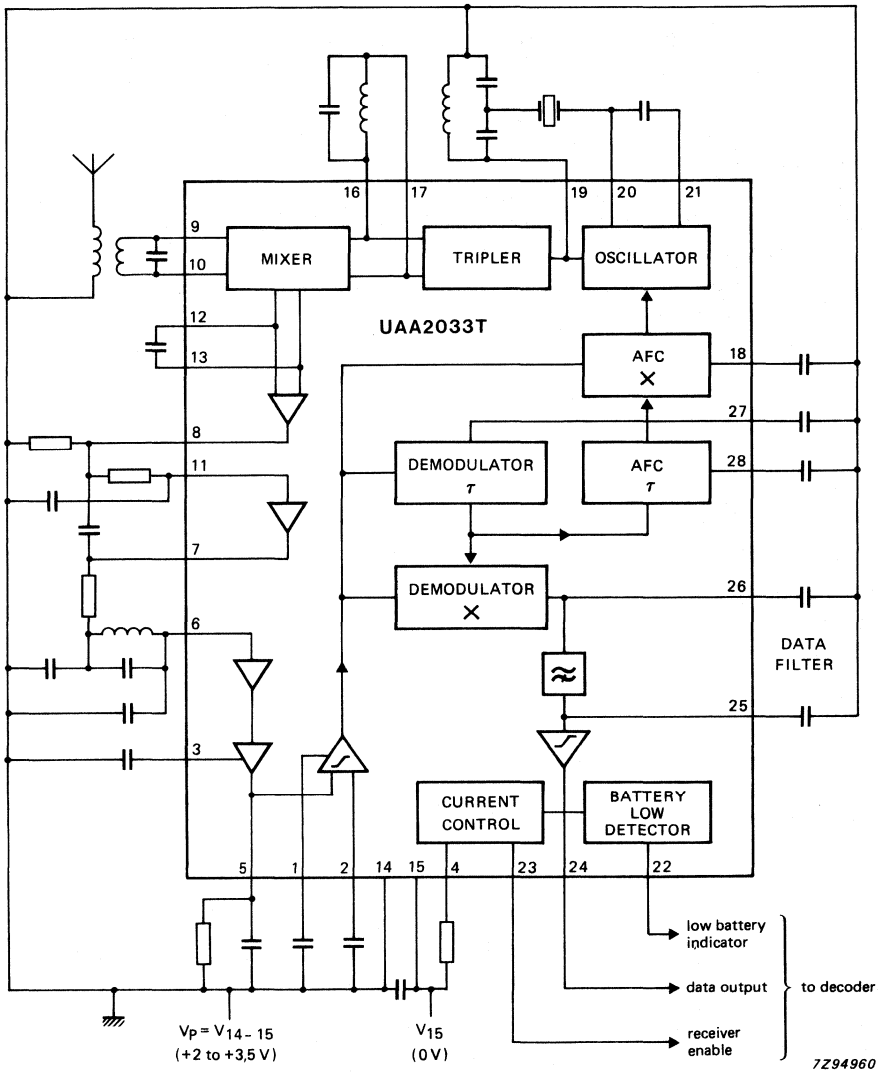


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

pin	description
1	low frequency filter '3' (limiter decoupling '2')
2	low frequency filter '2' (limiter decoupling '1')
3	low frequency filter '1'
4	current control (internal reference)
5	IF filter
6	IF filter
7	IF filter
8	IF filter
9	mixer input '2'
10	mixer input '1'
11	IF filter
12	mixer output 'B'
13	mixer output 'A'
14	supply voltage (positive)
15	supply voltage (negative)
16	tripler coil '2'
17	tripler coil '1'
18	AFC '2'
19	oscillator output
20	oscillator input
21	oscillator AFC range
22	low battery voltage indicator
23	receiver enable
24	data output
25	data filter '2'
26	data filter '1'
27	demodulator centre frequency
28	AFC '1'

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage	$V_P = V_{14-15}$	−0,3	8,0	V
Operating ambient temperature range	T_{amb}	−10	+70	°C
Storage temperature range	T_{stg}	−55	+125	°C

DC CHARACTERISTICS

V_P = 2,0 to 3,5 V; T_{amb} = −10 to +70 °C; typical values measured at T_{amb} = 25 °C, V_P = 2,7 V; test circuit as Fig. 3 with L4 short circuited, no RF input and crystal XL1 removed

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage		$V_P = V_{14-15}$	2,0	2,7	3,5	V
Supply current	pin 23 = HIGH	I_{14}	2,2	2,7	3,3	mA
	pin 23 = LOW	I_{14}	–	–	1,0	μA
Receiver enable (pin 23)						
Input voltage HIGH		V_{23-15}	V_P–0,6	–	–	V
Input voltage LOW	I_{14} = 1 μA	V_{23-15}	–	–	0,4	V
Input current HIGH		I_{23}	–	+1	–	μA
Input current LOW		I_{23}	–	−1	–	μA
Data output (pin 24)						
Output voltage HIGH		V_{24-15}	V_P–0,7	–	–	V
Output voltage LOW	I_{24} = ±10 μA	V_{24-15}	–	–	0,5	V
Low battery voltage indicator (pin 22)						
Detection voltage	note 1	V_{DET}	2,035	2,135	2,235	V
Output voltage HIGH	I_{22} = ±5 μA	V_{22-15}	V_P–0,5	–	–	V
Output voltage LOW	I_{22} = ±5 μA	V_{22-15}	–	–	0,5	V

AC CHARACTERISTICS

V_P = 2,0 to 3,5 V; T_{amb} = −10 to +70 °C; typical values measured at T_{amb} = 25 °C, V_P = 2,7 V; test circuit as Fig. 3 with f = 173,950 MHz; channel spacing = 25 kHz; deviation = ±4,5 kHz; bit rate = 512 b/s (256 Hz square wave); AFC frequency limits 173,948 and 173,952 MHz; see Tuning Procedure

parameter	conditions	symbol	min.	typ.	max.	unit
RF sensitivity and AFC performance						
Sensitivity for 10^{-2} bit error rate (note 2)	T_{amb} = 25 °C	EMF/2	–	–	0,30	μV
	T_{amb} = −10 to +70 °C	EMF/2	–	–	0,43	μV
Bit error rate	EMF/2 = 1 μV	BER	–	10^{-3}	–	
Data output (pin 24)						
Duty factor	EMF/2 = 100 μV; f = 174 MHz	δ	35	–	55	%
Transition time	EMF/2 = 100 μV; f = 174 MHz; R_L = 1 MΩ; C_L = 100 pF	t_T	–	–	50	μs

Notes to the characteristics

1. V_{22-15} goes HIGH if V_P is less than V_{DET}.
2. Sensitivity measurement.

   A simple digital method of performing an approximate bit error rate (BER) measurement with a counter is shown in Fig. 2. At high signal levels (10 μV) the counter should read the exact frequency of the data input to the signal generator. As the signal level is reduced, errors occur at the receiver output and effectively increase the output frequency read by the counter (error duration is nearly always less than a bit length).

   For a bit error rate of 1 in a 100 on a 512 b/s system, the counted frequency will increase from 256 Hz at high signal levels to 261 Hz when the input signal level is reduced to the 1 in a 100 BER point.

Tuning procedure for AC tests

1. After performing the DC tests, set up the device in the AC test circuit as per Fig. 3.
2. Connect pin 18 to a voltage source of $V_{18-14} = -0{,}59$ V. Measure the oscillator frequency with a counter connected to the link winding of L3.
   Tune C21 (crystal frequency trimmer) to set the crystal oscillator to a frequency of:

$$\frac{\text{received frequency} + 2\text{ kHz}}{3} \pm 100\text{ Hz}.$$

   For a received frequency of 173,950 MHz the oscillator frequency is 57,984 MHz.
3. Remove test voltage source and turn on the signal generator (f = 173,950 MHz, deviation = ± 4,5 kHz, 256 Hz square-wave modulation, RF input level = 3 mV).

   Monitor the audio amplitude at pin 5 using an oscilloscope with an AC sensitivity of at least 2 mV per division.

Note that in the following tests the RF signal generator level should be reduced as the receiver is tuned to ensure that the peak-to-peak audio output voltage at pin 5 lies between 20 mV and 100 mV.

4. Tune C22 (tripler) to obtain peak audio output voltage at pin 5. The tuning will be found to have a discontinuity on one side of the peak response, i.e. the level will drop much faster on one side of the peak than on the other. Therefore when setting C22 ensure that it is not set too close to the discontinuity.
5. Tune C3 (mixer input) to obtain a peak audio output on pin 5.
6. Disconnect the frequency counter from the oscillator output. Measure the voltage on pin 18 and check that it is within the range −0,57 to −0,61 V. If it is outside this range then adjust C21 (oscillator trimmer) until it comes within the limits.
7. Check with an oscilloscope that clean data is appearing on DATA OUTPUT (pin 24) and proceed with the AC tests.

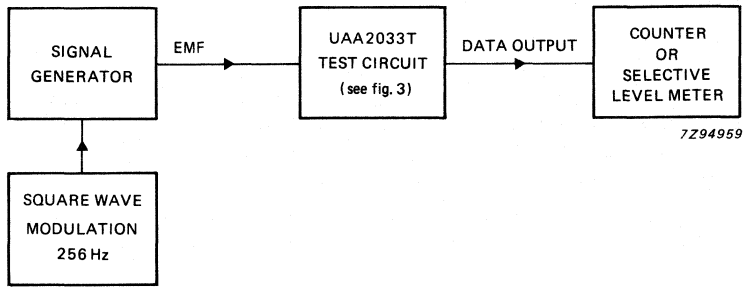


Fig. 2 Bit error rate measurement: signal generator frequency (f) = 173,95 MHz; input impedance of counter or selective level meter greater than 100 kΩ.

DEVELOPMENT DATA

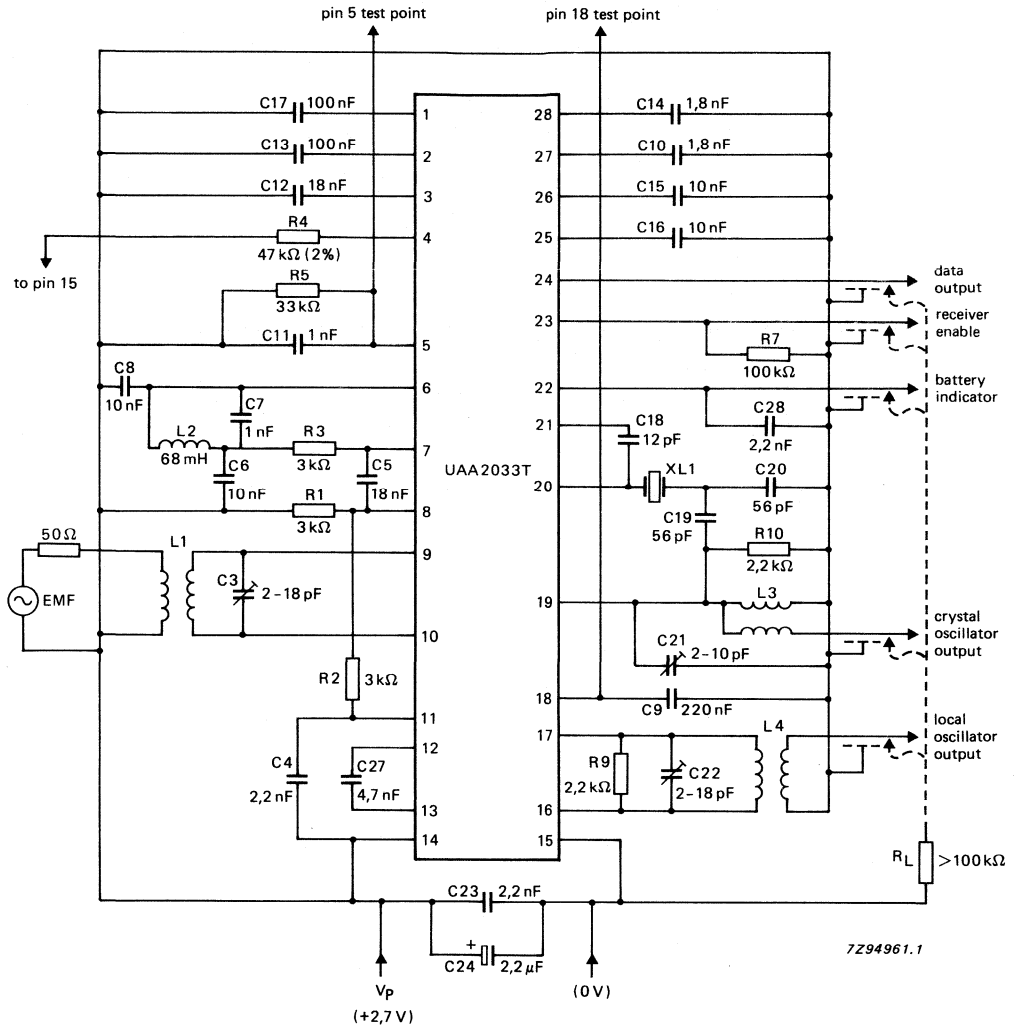


Fig. 3 Test circuit.

Coil data

L1, L3 and L4 wound with 0,315 mm enamelled wire on Toko ϕ 4,5 mm diameter former without pot or core. Screening cans also used.

L1 – 4 turns, one turn/groove. Link winding, 2 turns over the centre of the other winding.
L3 – 6 turns, 2 turns/groove. Link winding, 1 turn at bottom of former.
L4 – 3 turns, 1 turn/groove. Link winding, 1 turn at bottom of former.
L2 – 68 mH inductor. At 10 kHz minimum Q = 10.

Crystal (XL1) frequency 57985,90 kHz

DATA PROCESSOR FOR CELLULAR RADIO (DPROC)

GENERAL DESCRIPTION

The UMA1000T is a low power CMOS LSI device incorporating the data transceiving, data processing, and SAT functions (including on-chip filtering) for an AMPS or TACS hand-held portable cellular radio telephone.

Features

- Single chip solution to all the data handling and supervisory functions
- Configurable to both AMPS and TACS
- I^2C serial bus control
- All analogue interface and filtering functions fully implemented on chip
- Error handling in hardware reduces software requirements
- Low current consumption
- Small physical size
- Minimum external peripheral components required

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage (pin 28)	V_{DD}	4,5	5,0	5,5	V
Supply current (pin 28) normal operation	I_{DD}	–	2	–	mA
Operating ambient temperature range	T_{amb}	–40	–	+ 70	°C

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

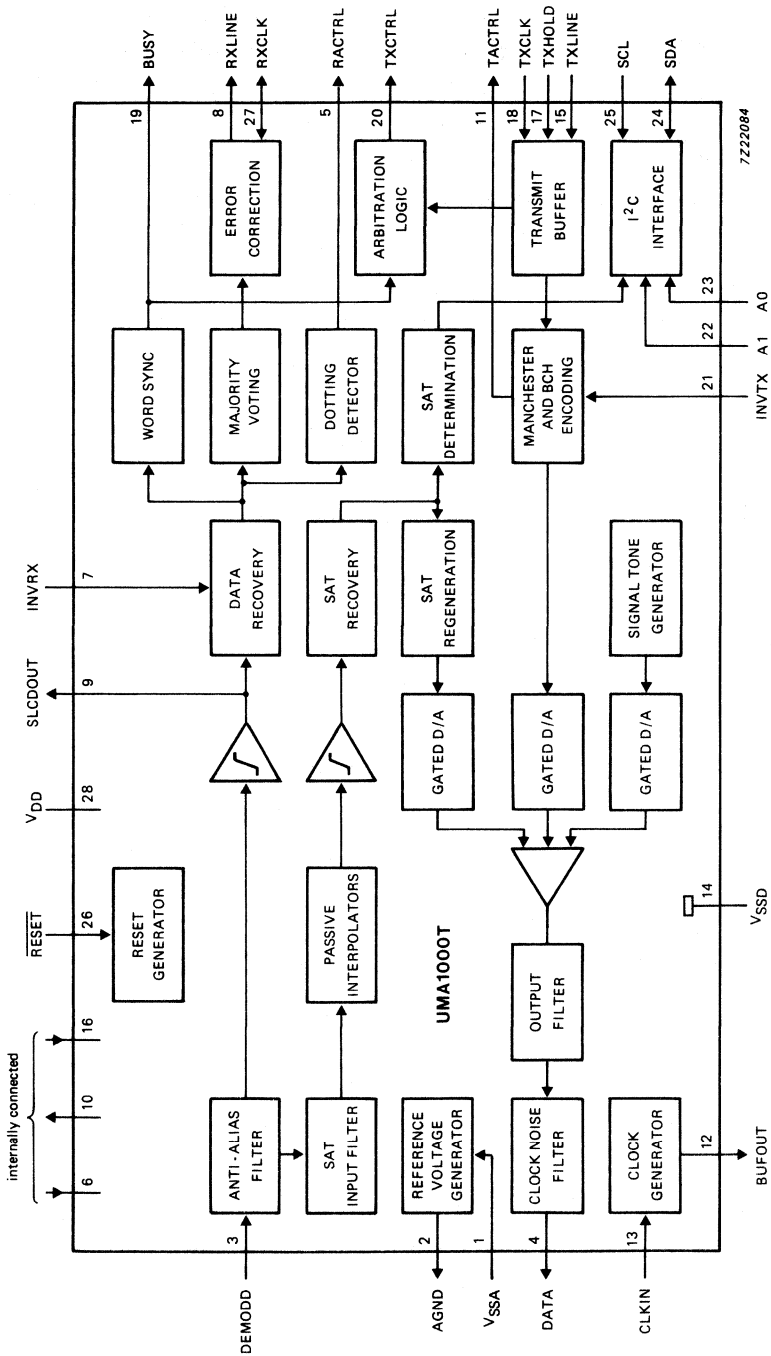


Fig. 1 Block diagram.

DEVELOPMENT DATA

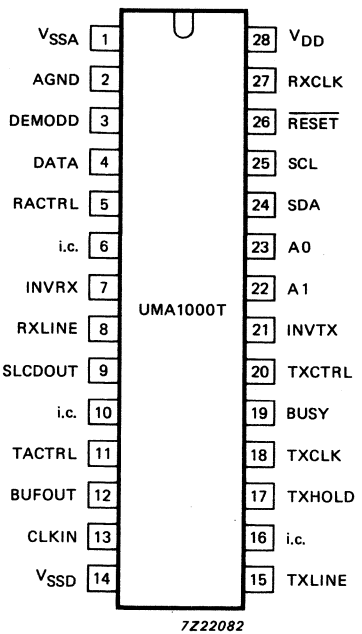


Fig. 2 Pinning diagram.

PINNING

1	V_{SSA}	analogue negative supply (0 V)
2	AGND	2,5 V analogue reference ground
3	DEMODD	received data signal input
4	DATA	transmitted data signal output
5	RACTRL	received audio control output
6	i.c.	internally connected; must be connected to V_{SSD}
7	INVRX	inverts sense of received data stream
8	RXLINE	received data signal output
9	SLCDOUT	sliced data
10	i.c.	internally connected; must be left open -circuit
11	TACTRL	transmitter audio control output
12	BUFOUT	buffered output of internal clock oscillator
13	CLKIN	1,2 MHz external master clock input
14	V_{SSD}	digital ground
15	TXLINE	transmitted data signal
16	i.c.	internally connected, must be connected to V_{SSD}
17	TXHOLD	holds off transmission of data
18	TXCLK	transmitted data clock input
19	BUSY	reverse control channel status putput
20	TXCTRL	transmitter control output
21	INVTX	inverts sense of transmitted data stream
22	A1	address input 1 (I²C bus)
23	A0	address input 0 (I²C bus)
24	SDA	serial data input/output (I²C bus)
25	SCL	serial clock input (I²C bus)
26	$\overline{\text{RESET}}$	master reset input
27	RXCLK	received data clock input
28	V_{DD}	positive supply voltage (+ 5 V)

CHARACTERISTICS

V_{DD} = 5 V ± 10%; T_{amb} = −40 to +70 °C; unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage			V_{DD}	4,5	5,0	5,5 V
Supply current	normal operation	I_{DD}	–	2,0	–	mA
Digital inputs	note 1					
Input voltage LOW		V_{IL}	0	–	0,3 V_{DD}	V
Input voltage HIGH		V_{IH}	0,7 V_{DD}	–	V_{DD} + 0,3	V
Input capacitance		C_I	–	–	6	pF
Digital outputs	note 1					
Output voltage LOW	I_{sink} = 1 mA	V_{OL}	–	–	0,8	V
Output voltage HIGH	I_{source} = 1 mA	V_{OH}	V_{DD}−0,8	–	–	V
Open-drain outputs	note 2					
Output voltage LOW	I_{sink} = 2 mA	V_{OL}	–	–	0,8	V

Notes to the characteristics

1. All digital inputs and outputs of DPROC are compatible with standard CMOS devices and the following general characteristics apply.
2. Open-drain outputs have no internal pull-up resistors.

FUNCTIONAL DESCRIPTION

General

The UMA1000T (DPROC) is a single chip CMOS device which handles the data and supervisory functions of an AMPS or TACS subscriber set.
These functions are:

- Data reception and transmission
- Control and voice channel exchanges
- Error detection, correction, decoding and encoding
- Supervisory Audio Tone decoding and transponding
- Signalling Tone generation

In an AMPS or TACS cellular telephone system, mobile stations communicate with a base over full duplex RF channels. A call is initially set up using one out of a number of dedicated control channels. This establishes a duplex voice connection using a pair of voice channels. Any further transmission of control data occurs on these voice channels by briefly blanking the audio and simultaneously transmitting the data. The data burst is brief and barely noticable by the user. A data rate of 10 kbit/s is used in the AMPS system and 8 kbits/s in TACS. The signalling formats for both Forward Channels (base to mobile) and Reverse Channels (mobile to base) are shown in Fig. 3.

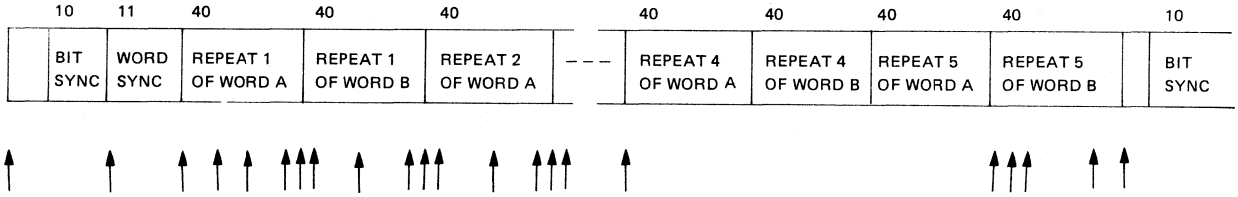
A function known as Supervisory Audio Tone (SAT), a set of 3 audio tones (5970, 6000 and 6030 Hz), is used to indicate the presence of the mobile on the designated voice channel. This signal, which is analagous to the On-Hook signal on land lines, is sent out to the mobile by the base station on the Forward Voice Channel. The signal must be accurately recovered and transponded back to the base station to complete the 'loop'. At the base station this signal is used to ascertain the overall quality of the communication link.

Another voice channel associated signal is Signalling Tone (ST). This tone (8 kHz TACS, 10 kHz AMPS) is generated by the mobile and is sent in conjunction with SAT on the Reverse Voice Channel to serve as an acknowledgement signal to a number of system orders.

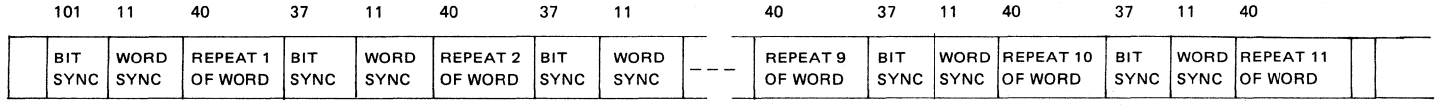
The key requirements of a hand held portable cellular set are:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

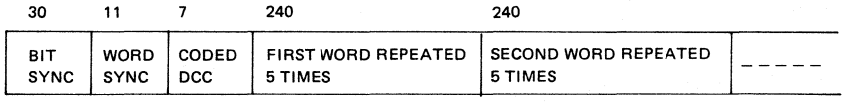
The DPROC is a member of our Cellular Radio chipset, based on the I^2C bus, which meets these requirements. A cellular radio system schematic using the chip set is shown in Fig. 4.



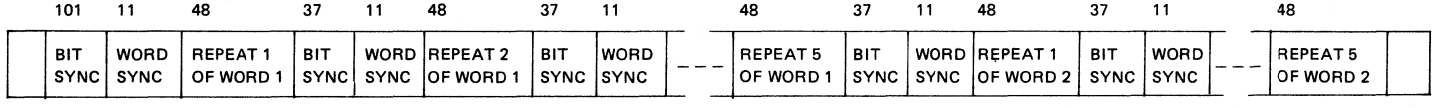
(a) forward control channel



(b) forward voice channel



(c) reverse control channel



(d) reverse voice channel

Fig. 3 Signalling formats.

DEVELOPMENT DATA

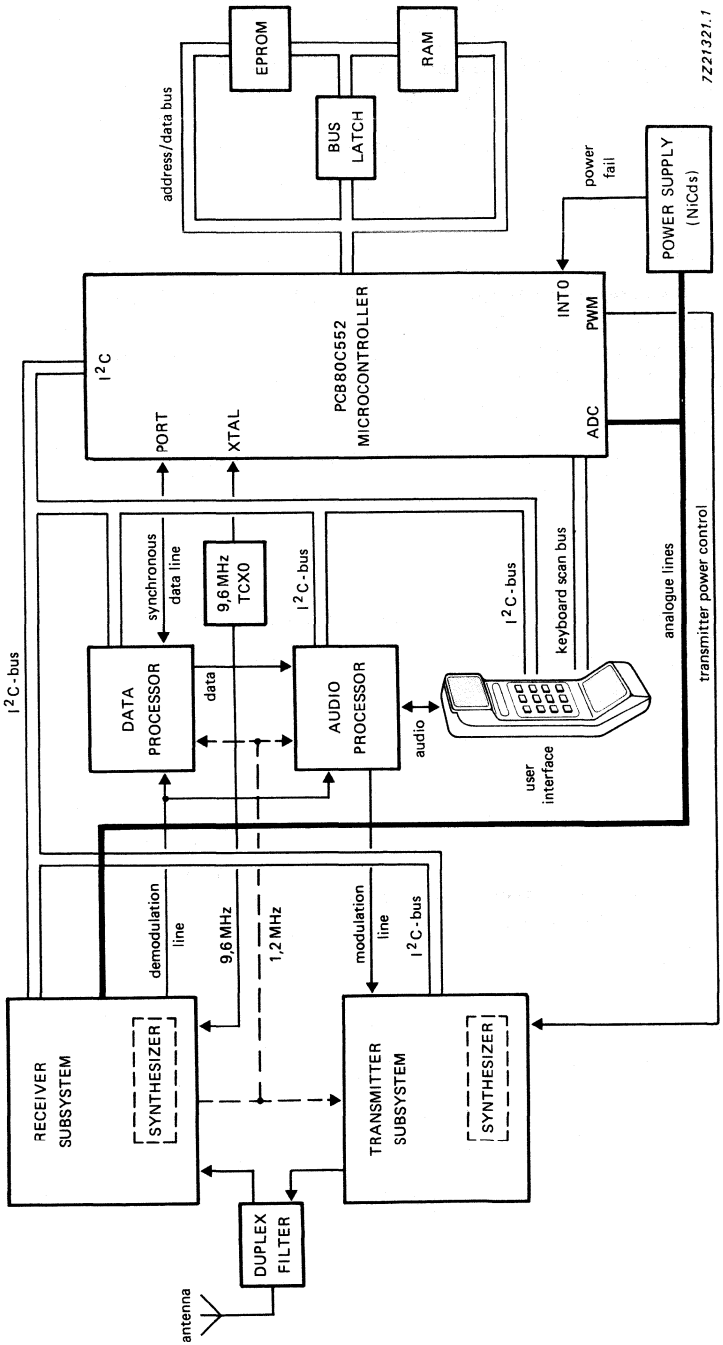


Fig. 4 Cellular radio system schematic.

EXTERNAL PIN DESCRIPTION

Supply (V_{DD}; V_{SSA}; V_{SSD}; AGND)

V_{DD} : Positive supply voltage for digital and analogue circuitry (± 5 V +10%)
V_{SSA} : Negative supply voltage for analogue circuitry (0 V)
V_{SSD} : Digital ground (0 V)
AGND: Internally generated reference ground used by internal analogue circuitry. Voltage level $(V_{DD} - V_{SSA})/2 \pm 2\%$.

Both V_{SSA} and V_{SSD} must be connected to common ground.

System clock (CLKIN; BUFOUT)

CLKIN is a digital input for the externally generated 1,2 MHz master clock. This signal should be accurate to 100 ppm and have a worst case of 60 : 40 mark-space ratio. BUFOUT is the buffered output of the clock oscillator and provides the option of generating the clock signal on chip by connecting a 1,2 MHz crystal between BUFOUT and CLKIN.

I^2C serial data link (SDA; SCL)

SDA is the bi-directional data line; SCL the clock input from an I^2C master. These constitute a typical I^2C link and conform to standard characteristics as defined in the I^2C bus specification.

- data rate: up to 100 kbit/s

Slave Address Select (A0; A1)

Selection of the device slave address is achieved by connecting A0 and A1 to either V_{SSD} or V_{DD}.

The slave address is defined in accordance with the I^2C specifications as shown in Fig. 5.

1	1	0	1	1	A1	A0	R/$\overline{W}$

Fig. 5 Device slave address.

Master reset ($\overline{RESET}$)

$\overline{RESET}$ is an asynchronous active LOW master reset input, with a minimum active pulse width of 2 μs used to reset certain logic within DPROC to a predefined state as illustrated in Tables 1 and 2. The device should be reset using this pin after power up.

Power-up state

DPROC will not respond reliably to any inputs (including $\overline{\text{RESET}}$) until 100 μs after the power supply has settled within the specified tolerance. The analogue sections of the device will have stabilized within 5 ms. No power-on-reset is provided, therefore before the device can enter normal operation $\overline{\text{RESET}}$ must be pulsed LOW. Following a device master reset the digital output pins and I^2C registers will have predefined states as illustrated in Tables 1 and 2.

Table 1 Predefined state of the digital output pins

output	state
RXLINE	HIGH
TXCTRL	HIGH
TACTRL	HIGH
RACTRL	HIGH
BUSY	HIGH

Table 2 Predefined state of the I^2C registers

register	bit							
	7	6	5	4	3	2	1	0
status	LOW	LOW	LOW	LOW	LOW	LOW	HIGH	HIGH
control	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
SATD	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
TST	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW

DEVELOPMENT DATA

Data Transfer Link (RXLINE; TXLINE; TXHOLD; TXCLK and RXCLK)

RXLINE, TXLINE, TXCLK and RXCLK provide a dedicated serial data link for the transfer of system data messages between DPROC and the system controller at variable rates of up to 200 kbits/s. TXHOLD allows the system controller to preload the DPROC transmit register with one word without the data being transmitted. DPROC then starts transmitting the instant TXHOLD is driven LOW.

- RXCLK : clock input from system controller
- RXLINE : data output from DPROC to system controller
- TXCLK : clock input from system controller
- TXLINE : open drain data bi-directional line to the system controller
- TXHOLD : (HIGH) holds off transmission of data
- data rate : up to 200 kbit/s

Note

A minimum mean data transfer rate for the received data of 2,1 kbits/s (AMPS) and 1,7 kbits/s (TACS) is required to ensure against loss of message words.

The format for received and transmitted data words is shown in Fig. 13 (a) and Fig. 13 (b) respectively. The receive and transmit data timing is illustrated in Fig. 14 (a) and Fig. 14 (b) respectively.

EXTERNAL PIN DESCRIPTION (continued)

Transmitter Control (TXCTRL)

TXCTRL is an open-drain output used to disable the transmitter during a Reverse Control Channel access failure.

- output level HIGH : RF enable
- output level LOW : RF disable

Transmitter Audio Enable (TACTRL)

TACTRL is an open-drain digital output signal used to blank the audio path and enable the data path to the modulator during data bursts on the Reverse Voice Channel.

- output level HIGH : audio enabled
- output level LOW : audio muted

Receiver Audio Enable (RACTRL)

RACTRL is an open-drain digital output used to blank the audio path to the earpiece when a sequence of dotting is detected.

RACTRL and TACTRL functions can be combined using one line.

- output level HIGH : audio enabled
- output level LOW : audio muted

Reverse Control Channel Status (BUSY)

BUSY is a digital output giving the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits and has the following logic levels:

- output level HIGH : channel busy
- output level LOW : channel idle

On a voice channel BUSY indicates channel idle.

Invert Receive Data (INVRX)

Enables an additional inverter in the receive data path. This allows RF demodulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the demodulated data stream into DPROC depends on the receiver local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Invert Transmit Data (INVTX)

Enables an additional inverter in the transmit data path. This allows RF modulators with high or low local oscillators to be used. The TACS and AMPS specifications define a NRZ encoded logic 1 as a LOW-to-HIGH transition in the centre of a data bit period. The polarity of the modulated data stream depends on the transmitter local oscillator.

- input HIGH : data inverted
- input LOW : data normal

Transmitted Data Output (DATA)

Data is an analogue output which provides Manchester encoded and filtered data signal SAT and signalling tone. This signal should normally be AC coupled into the Audio/Data summer.

- DC level : analogue ground (AGND)
- signal level : 2 V (p-p) *
- signal tolerance : 2% + supply voltage variation (ΔV_{DD})
- minimum load impedance : 10 kΩ
- maximum load capacitance : 2 nF
- maximum output impedance : 50 Ω

Received Data Input (DEMODD)

Demodd inputs analogue data and SAT signals from the RF demodulator. This pin should normally be AC coupled.

- DC level : analogue ground (AGND)
- nominal data level : 250 mV (p-p)
- minimum data level: : 130 mV (p-p)
- input impedance : $>$ 1 MΩ

Sliced Data Output (SLCDOUT)

Unbuffered output from data slicer. Normally used only for test purposes.
Should be left open-circuit for normal operation.

DEVELOPMENT DATA

* Signal level with filtered data signal.

CHARACTERISTICS OF THE I²C BUS

The I²C bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals.

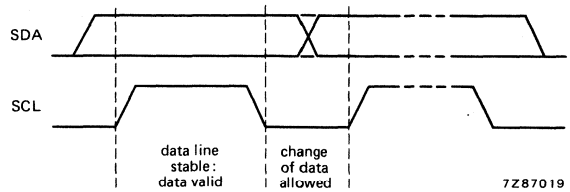


Fig. 6 Bit transfer.

Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the start condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the stop condition (P).

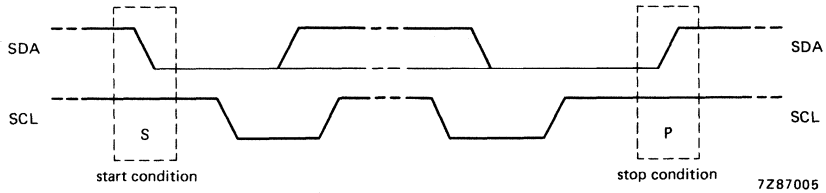


Fig. 7 Definition of start and stop conditions.

System configuration

A device generating a message is a "transmitter", a device receiving a message is the "receiver". The device that controls the message is the "master" and the devices which are controlled by the master are the "slaves".

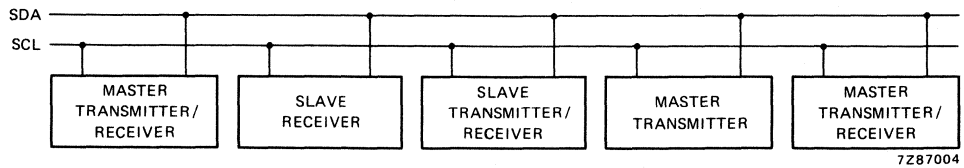


Fig. 8 System configuration.

CHARACTERISTICS OF THE I²C bus (continued)

Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse, set up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by *not* generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

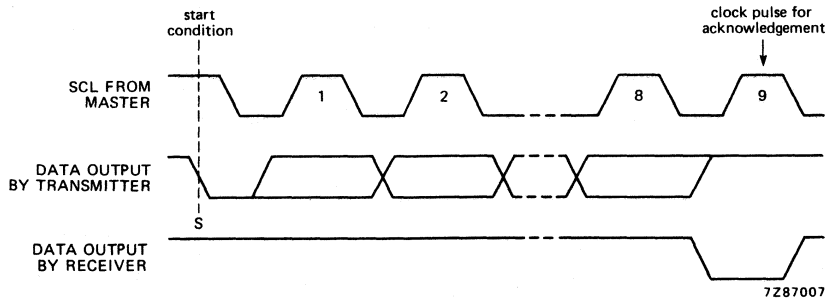


Fig. 9 Acknowledgement on the I²C bus.

Timing specifications

Masters generate a bus clock with a maximum frequency of 100 kHz. Detailed timing is shown in Fig. 10.

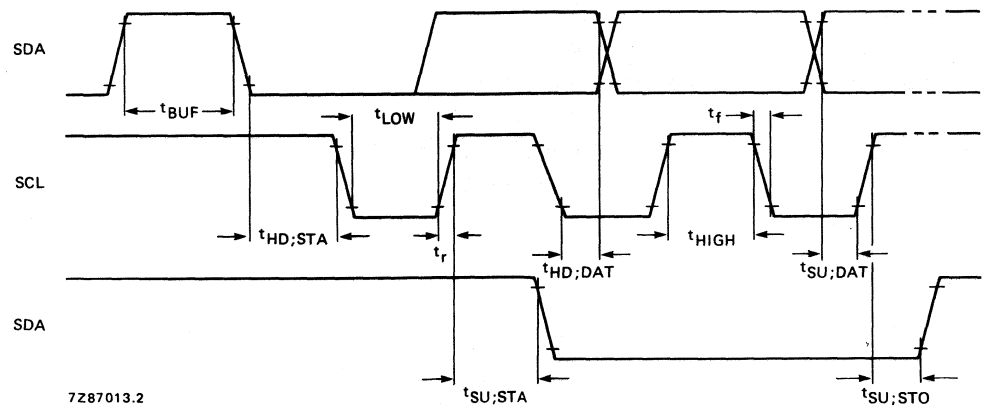


Fig. 10 Timing.

CHARACTERISTICS OF THE I²C BUS (continued)

Where:

t_{BUF}	$t \geqslant t_{LOWmin}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;STA}$	$t \geqslant t_{HIGHmin}$	Start condition hold time
t_{LOWmin}	4,7 μs	Clock LOW period
$t_{HIGHmin}$	4 μs	Clock HIGH period
$t_{SU;STA}$	$t \geqslant t_{LOWmin}$	Start condition set-up time, only valid for repeated start code
$t_{HD;DAT}$	$t \geqslant 0$ μs	Data hold time
$t_{SU;DAT}$	$t \geqslant 250$ ns	Data set-up time
t_r	$t \leqslant 1$ μs	Rise time of both the SDA and SCL line
t_f	$t \leqslant 300$ ns	Fall time of both the SDA and SCL line
$t_{SU;STO}$	$t \geqslant t_{LOWmin}$	Stop condition set-up time

Note

All the values refer to V_{IH} and V_{IL} levels with a voltage swing of V_{DD} to V_{SS}.

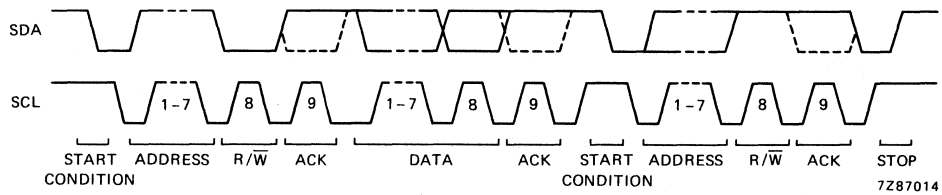


Fig. 11 Complete data transfer.

Where:

Clock t_{LOWmin}	4,7 μs
$t_{HIGHmin}$	4 μs
The dashed line is the acknowledgement of the receiver	
Max. number of bytes	Unrestricted
Premature termination of transfer	Allowed by generation of STOP condition
Acknowledge clock bit	Must be provided by the master

Note

The general characteristics and detailed specification of the I²C bus are available on request.

I²C REGISTERS

General

The I²C register block resides internally within the I²C interface block and contains various items of status and control information which are transferred to and from DPROC via the I²C bus. The block is organized into four 8-bit registers:

- Status Register — contains read only items
- Control Register
- SAT Programmable Phase Shift Register — contain write only items

Note

In normal operation the SAT delay register requires programming only after a device reset.

Table 3 Register map

register	bit							
	7	6	5	4	3	2	1	0
status	–	–	WSYNC	BUSY	TXABRT	TXIP	MSCC1	MSCC0
control	–	SERV	STS	TXRST	ABREN	FVC	STEN	SATEN
SATD	<---------- SAT delay data ---------->							

S	DPROC ADR	R	A	STATUS	A	P

(a) read from DPROC status register

S	DPROC ADR	W	A	CONTROL	A	P

(b) write to DPROC control register

S	DPROC ADR	W	A	CONTROL	A	SAT DELAY	A	P

(c) write to all DPROC registers

Where:

S : START condition
W : read/write bit (logic 0 = write)
R : read/write bit (logic 1 = read)
A : acknowledge bit
P : STOP condition
DPROC ADR : slave address of DPROC

Fig. 12 I²C data format.

I^2C REGISTERS (continued)

Status Register

This is a read only register containing DPROC status information.

Measured SAT Colour Code (MSCC1; MSCC0)

MSCC1 and MSCC0 provide information about the current measured SAT colour code in accordance with Table 4.

Table 4 Measured SAT Colour Code

MSCC1	MSCC0	SAT frequency (Hz)
0	0	5970
0	1	6000
1	0	6030
1	1	no valid SAT

Transmission In Progress (TXIP)

TXIP indicates whether DPROC is currently accessing the Reverse Control or Voice Channels.

- logic 1 : data transmission in progress
- logic 0 : transmission not in progress

Transmission Abort Status (TXABRT)

TXABRT indicates that a Reverse Control Channel Access Attempt has been aborted by DPROC without successful message transmission.

- logic 1 : transmission attempt aborted
- logic 0 : no access collision detected

Reverse Control Channel Status (BUSY)

BUSY gives the status of the Reverse Control Channel. This is determined by a majority decision on the result of the last 3 consecutive Busy-Idle bits.

- logic 1 : channel busy
- logic 0 : channel idle

On a voice channel the BUSY bit defaults to the cleared state.

Note

This signal is also routed to the BUSY output pin.

Word Synchronization Indicator (WSYNC)

WSYNC indicates whether DPROC has acquired frame synchronization according to the Forward Control Channel format.

- logic 1 : frame synchronization acquired
- logic 0 : no frame synchronization

Control Register

This is a write only register containing DPROC control information.

SAT Path Enable (SATEN)

SATEN enables the SAT transponded signal to be output on external pin DATA.

- logic 1 : SAT tone enabled
- logic 0 : SAT tone inhibited

Signalling Tone (ST) Path Enable (STEN)

STEN enables the Signalling Tone to be output on external pin Data.

- logic 1 : ST enabled
- logic 0 : ST inhibited

Channel Format Select (FVC)

FVC selects the required channel format.

- logic 1 : Voice channel format
- logic 0 : Control channel format

Transmission Abort Permission (ABREN)

ABREN indicates whether DPROC has permission to abort data transmission and disable RF on the Reverse Control Channel following the detection of a channel access attempt collision.

- logic 1 : RF disable allowed
- logic 0 : RF disable inhibited

Message Transmission Abort (TXRST)

TXRST terminates a message being transmitted on the reverse channel. It is a monostable signal which when activated causes a reset of the message transmission circuitry and causes TXABRT and TXIP I^2C signals to be reset.

- logic 1 : reset active
- logic 0 : reset inactive

System Type Select (STS)

STS selects required system format.

- logic 1 : AMPS
- logic 0 : TACS

Serving System Select (SERV)

SERV selects which of the serving system data streams (A or B) is accepted.

- logic 1 : system A selected
- logic 0 : system B selected

SAT Programmable Delay Register (SATD)

SATD programs the value of phase shift which is applied to the SAT tones in the SAT Regeneration Block. This value will be determined and programmed into the System Controller during manufacture. The recovered SAT is delayed in time by approximately 0,8 μs x value in the register which corresponds to approximately 1,8 degrees x value in the register. The total phase shift is limited to 360 degrees.

DIGITAL CIRCUIT BLOCKS

General

The majority of the digital circuitry within the DPROC device is identical for both AMPS and TACS. The device has little additional redundancy to implement both systems. The functions of these blocks are described in the following sections and relate to those shown in Fig. 1.

Data Recovery

The Data Recovery Block receives wideband Manchester encoded data in sampled and sliced form from the Strobed Comparator Block, on which it performs the following functions:

- clock recovery
- Manchester decoding
- data regeneration

The Clock Recovery Block extracts an 8 or 10 kHz (TACS or AMPS) phase locked clock signal from the Manchester encoded data stream. This is implemented using a digital-phase-locked-loop (PLL) which has an adjustable "bandwidth" to provide both fast acquisition and low jitter.

Manchester decoding is performed by exclusive ORing the recovered Manchester encoded data with the recovered clock.

The NRZ data regeneration is performed by a digital integrate and dump circuit. This consists of an up/down counter that counts 1,2 MHz cycles during the data period. The sense of the count is determined by the result of the Manchester Decoder output. The number of counts is sampled at the end of a data period. If this number exceeds a threshold the data is latched as a 1 otherwise it is latched as a 0.

SAT Processing

The Supervisory Audio Tone processing consists of the following functions:

- SAT recovery
- SAT determination
- SAT regeneration

SAT recovery

The SAT Recovery Block receives a filtered and sliced SAT signal which must be recovered before being routed to the Determination and Regeneration Blocks.
The recovery is performed using a digital phase-locked-loop.

SAT determination

The SAT Determination Block indicates which, if any, of the valid SAT tones is detected from the recovered SAT. The AMPS and TACS specifications require that a determination is made at least every 250 ms. Determination involves counting the number of cycles of the regenerated SAT in this time period. This count is then compared to a set of four known counts which define the boundaries between the SAT frequencies and the SAT not valid events. The result is then coded into the I^2C status registers MSCC0 and MSCC1 as shown in Table 5.

Table 5 Status registers MSCC0, MSCC1; decoded SAT frequencies

register		SAT frequency band (Hz ± 4 Hz)	decoded SAT (Hz)
MSCC0	MSCC1		
1	1	< 5956	not valid
0	0	5956 to 5986	5970
0	1	5986 to 6014	6000
1	0	6014 to 6046	6030
1	1	> 6046	not valid

SAT regeneration

The SAT Regeneration Block generates a digital SAT stream from the recovered SAT stream for transponding back to the base station. The AMPS and TACS specifications require the SAT to be transponded with a maximum phase shift of 20 degrees between the point the modulated RF signal enters the mobile from the base station, and the point the modulated RF leaves the mobile. A variable phase compensation circuit is provided in DPROC to shift the recovered SAT through 0 to 360 degrees before being passed to the output summing network. The degree of phase shift is determined during manufacture of the set and the required additional phase shift is stored in non-volatile RAM and programmed via I^2C at each power-on cycle. The phase correction is performed by a counter delay method using signals which are phase locked to the recovered SAT.

DEVELOPMENT DATA

Dotting Detector

The Dotting Detector Block determines whether a data inversion (dotting) pattern has been received on the Forward Voice Channel. The detection of 32 bits of data inversion indicates that the Clock Recovery Block has acquired bit synchronization and that the narrow bandwidth mode on the clock recovery phase-locked-loop is selected. This signal is also used to indicate that a data burst is expected and activates the audio mute RACTRL for the duration of the burst.

Word Synchronization Detector

The Word Synchronization Block performs the following functions:

- Frame synchronization
- Reverse Control Channel status (B/I determination)
- Valid Serving System determination

These functions are associated solely with the Forward Control Channel and have no meaning on the Forward Voice Channel.

Information in a data stream is identified by its position with respect to a unique synchronization word. This synchronization word is an 11 bit-Barker code which has a low probability of simulation in an error environment, and can be easily detected. Data received is only considered valid at times when DPROC has achieved frame synchronization. In this condition the block leaves its search mode and enters its lock mode. This is indicated by bit WSYNC being set HIGH. In order to achieve this two consecutive synchronization words separated by 463 bits must be detected. Once in lock mode, the synchronization word detector is examined every 463 bits and only loses frame synchronization after 5 consecutive unsuccessful attempts at detecting the synchronization word have been made. At this point bit WSYNC is cleared and the device is returned to its search mode. On the Forward Voice Channel detection of the synchronization word indicates that the following 40 bits are valid data. Information detailing the status of the Reverse Control Channel is given by the Busy/Idle bits. These occur at intervals of 11 bits within the frame, the first occurring immediately following the synchronization word. The status of the channel is determined by a majority decision on the last three consecutive Busy/Idle bits.

DIGITAL CIRCUIT BLOCKS (continued)

Majority Voting Block

The Majority Voting Block performs the following functions:

- identifying position and validity of frames in the received data stream
- extracting 5 repeats of each word from a valid frame
- performing a bit-wise majority decision on the five repeats of the data word

The validity of the frames is determined by setting a counter in operation which times out and resets the circuitry after 920 or 463 bit periods from detecting valid word synchronization. The time out period selected depends on whether DPROC is monitoring the Forward Voice or Control Channel respectively.

Up to five repeats of the message word are searches for and extracted by DPROC. On the forward Voice Channel DPROC will extract the first five words that occur for which a correct synchronization word is found. These words can occur in any position in the frame. A serial majority vote is performed as the fifth word is being extracted.

Error Correction Block

The Error Correction Block performs the following functions:

- extraction of a valid message from the Majority-Voted Word
- computation of the S1 and S3 syndromes
- correction of up to one error in the word
- communication of received data to the System Controller via the Received Data Serial Link.

Interpretation of parity of a received word is obtained from knowledge of the syndromes of the word. The syndromes are calculated using feedback shift registers with two characteristic equations:

$$1 + X + X^6 \text{ and } 1 + X + X^2 + X^4 + X^6$$

Once the syndromes of a received word are known, it is possible to determine if a correctable error is present. DPROC only corrects up to one error although the code used has a Hamming distance of five. The occurence of two or more errors is signalled by setting the BCH error flag, which is communicated to the System Controller via the Received Data Serial Link.

Received Data Serial Link

The Received Data Serial Link transfers data and control information from DPROC to the System Controller over RXLINE under control of a clock signal RXCLK generated by the System Controller.

Data Format

Each Received Data word consists of 4 bytes. The word format is shown in Fig. 13 (a). The sense and function of the fields is shown in Table 6.

Table 6 Received Data word

bit	title	sense	function
31	start	LOW	identifies start of word
30	BCH error	active HIGH	indicates that an uncorrected BCH error is associated with the word
29 to 2	received data	binary data	received data word
1	RXLINE error	LOW	if detected as HIGH indicates that a transmission error has occured on the serial link
0	stop	HIGH	identifies end of the word

Link Protocol

The Received Data protocol is described by the timing diagram Fig. 14 (a) and has the following parameters:

- maximum receive window (RWIN)
  Control Channel (TACS) = 47 ms
  Control Channel (AMPS) = 37 ms
- minimum clock period ($t_{CLK(min)}$ = 2 μs

Transmit Data Serial Interface

The Transmit Data Serial Link performs reception of data from the System Controller to DPROC over a dedicated line TXLINE. The transfer of data is synchronous with a clock signal TXCLK, generated by the System Controller.

Data Format

Each Transmit Data word consists of 5 bytes. The word format is shown in Fig. 13 (b). The sense and function of the fields is shown in Table 7.

Table 7 Transmit Data word

bit	title	sense	function
39	start	LOW	identifies start of word
38, 37	DCC	binary data	digital colour code
36 to 1	transmit data	binary data	transmit data word
0	stop	HIGH	identifies end of the word

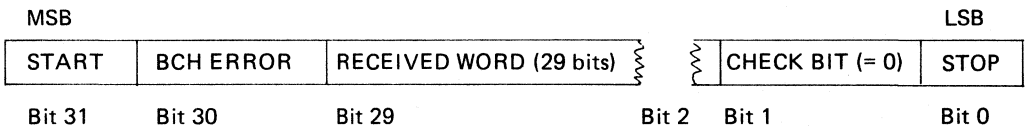
DIGITAL CIRCUIT BLOCKS (continued)

Transmit Data Serial Interface (continued)

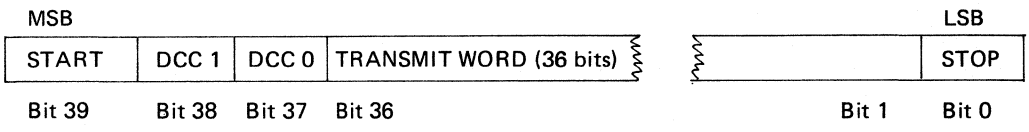
Link Protocol

Messages can be up to 5 words in length on the Reverse Control Channel and up to 2 words in length on the Reverse Voice Channel. These must be transmitted on the data stream without interruption. To avoid the need for large buffer areas, a flexible protocol is used to allow DPROC to control the transfer of data words. The System Controller can abort the transmission of a message at any point by activating the I^2C signal TXRST. This signal causes the interface to return to its power-up state and resets TXIP and TXABRT (see Table 3). On completion of these tasks TXRST will return to its inactive state. The Transmit Data Protocol is described by the timing diagram shown in Fig. 14 (b) and has the following parameters:

- maximum transmit window (TWIN)
  - Voice channel (TACS) = 60 ms
  - Voice channel (AMPS) = 48 ms
  - Control channel (TACS) = 29 ms
  - Control channel (AMPS) = 23 ms
- minimum clock period ($t_{CLK(min)}$) = = 2 μs
- minimum clock hold-off time (t_{WAIT}) = 10 μs

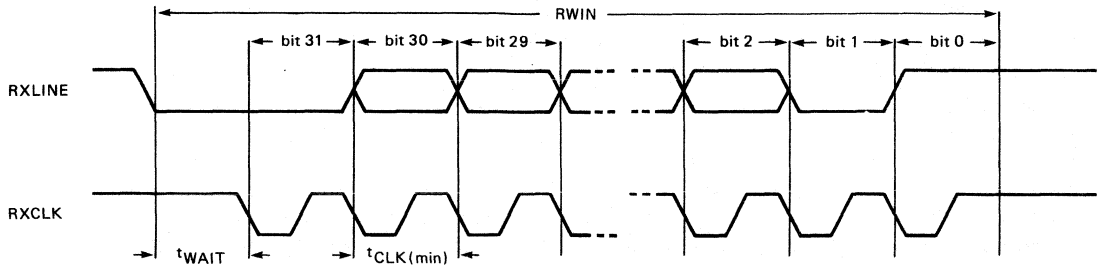


(a) received data word

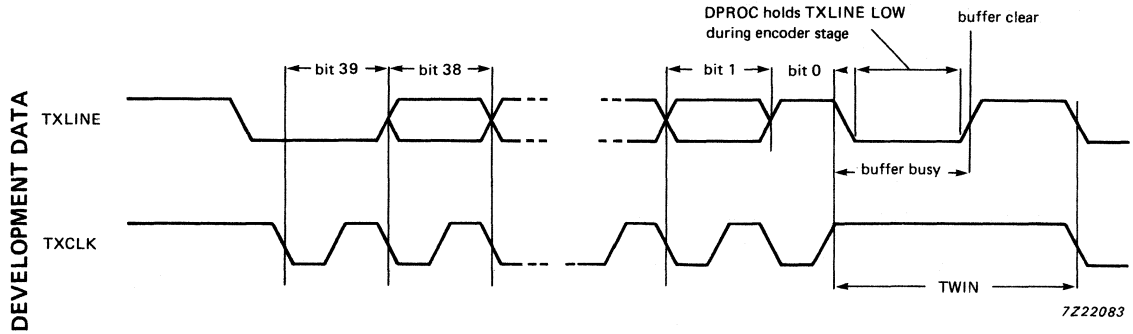


(b) transmit data word

Fig. 13 Data word formats.



(a) DPROC to microcontroller link; receive data timing



DEVELOPMENT DATA

(b) Microcontroller to DPROC link; transmit data timing

Fig. 14 Data timing diagrams.

DIGITAL CIRCUIT BLOCKS (continued)

BCH and Manchester Encoding Block

The functions performed by this circuit block include:

- reception of data from the System Controller
- parity generation
- message construction
- Manchester encoding

Each 36-bit Information Word sent on the Reverse Voice and Control Channels is coded into a 48 bit code word. The code word consists of the 36-bit word followed by 12 parity bits. These parity bits are formed by clocking the information word into a 12-bit feedback shift register with characteristic equation:

$$1 + X^3 + X^4 + X^5 + X^8 + X^{10} + X^{12}$$

The BCH Encoder Block constructs the Reverse Voice and Control Channel data streams from the information it receives from the System Controller.
The streams are formed out of the four possible field types:

- Dotting (data inversions)
- 11-bit Synchronization Word
- Digital Colour Code
- 48-bit code word

The 2 bits of DCC received from the System Controller are coded into a 7-bit word as shown in Table 8.

Table 8 Digital Colour Code; 7-bit word

DCC1	DCC0	Coded DCC						
0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1
1	0	1	1	0	0	0	1	1
1	1	1	1	1	1	1	0	0
		DCC1		DCC0			DCC1.EXOR.DCC0	

The data sense for Manchester Encoding has a NRZ logic 1 encoded as a 0-to-1 transition and a NRZ logic 0 encoded as a 1-to-0 transition.

Reverse Control Channel Access Arbitration

The AMPS and TACS specifications require a method of arbitration on the Reverse Control Channel to prevent two mobiles from transmitting on the same channel at the same time. This function is performed by DPROC monitoring the Busy/Idle stream sent on the Forward Control Channel.

The AMPS and TACS specifications state that once the mobile has commenced transmitting on the Reverse Control Channel it must monitor the Busy/Idle stream. If this stream becomes active outside a predetermined 'window', measured from the start of the transmission of the message, the mobile must terminate its transmission and disable the transmitter immediately.

In the Cellular Radio chip-set there are two levels of control of the RF transmitter; the first is absolute control by the System Controller, the second is conditional by other devices in the set. In DPROC the conditional control of the transmitter is performed via the output TXCTRL. This line is effectively wired ORed together, using open-drain outputs, with other devices which may wish to control the transmitter. When these devices do not wish to disable the transmitter their output is in a HIGH impedance state.

An exception to this procedure occurs when the Serving System instructs the mobile not to monitor the Busy/Idle bits. In this event the arbitration logic can be disabled by clearing I^2C register bit ABREN.

The flow of events during a Control Channel Access attempt is as follows:

Initial State

- transmitter power off via I^2C
- DPROC transmit circuitry in power-up state
- TXCTRL line HIGH

Access Attempt Procedure

1. System Controller decides to send message (note 1).
2. System Controller drives TXCTRL low directly.
3. System Controller switches transmitter power on and waits for power-up for the transmitter module (RF transmitter is still disabled by TXCTRL).
4. System Controller sets ABREN via I^2C (if required) allowing DPROC to control the transmitter.
5. System Controller determines status of Reverse Control Channel by monitoring the Busy/Idle bit. If busy, waits a random time then tries again.
6. System Controller releases TXCTRL allowing it to be pulled HIGH enabling the transmitter output.
7. System Controller transfers message to DPROC via serial link (note 1).
8. DPROC sets I^2C signal TXIP and starts sending message while monitoring Busy/Idle status.
9. If channel becomes busy before 56 bits and ABREN is set then perform Abort Procedure.
10. If channel remains idle after 104 bits and ABREN is set then perform Abort Procedure.
11. On completion of entire message DPROC clears TXIP and 25 ms later the System Controller disables transmitter via I^2C.
12. System Controller finally sends TXRST to prepare DPROC for next transmission.

Note to the Access Attempt Procedure

At stage 1 the system controller may choose to preload DPROC with the first word of the message and hold it from transmission until stage 7 using the TXHOLD line. This gives a lower time overhead between detecting an IDLE channel and commencing the transmission. To use this feature TXHOLD must be driven HIGH before the last bit of data has been transferred into DPROC.

DIGITAL CIRCUIT BLOCKS (continued)

Abort Procedure

1. DPROC immediately disables transmitter output by driving TXCTRL low.
2. DPROC sets TXABRT.
3. System Controller detects failure by monitoring TXCTRL and TXABRT.
4. System Controller disables transmitter via RF power amplifier.
5. System Controller sends TXRST to prepare DPROC for next transmission.

Signal Tone Generation (ST)

The 8 or 10 kHz (TACS or AMPS) tone generated from the Manchester Encoding Block is used as the Signalling Tone stream.

ANALOGUE CIRCUIT BLOCKS

General

The analogue signal processing functions on DPROC are implemented using switched-capacitor techniques. The main filtering functions are operated at 300 kHz, and these circuits are 'interfaced' to the continuous time and sampled digital domains by distributed RC active filters, passive interpolators and comparators.

The distributed RC sections, the Anti-Alias Filter and the Clock Noise Filter, are non-critical and are designed to tolerate process spreads. The critical filtering in the SAT Filter and the Output Filter, is performed by 300 kHz switched-capacitor circuitry. The Passive Interpolators increase the sampling rate from 300 kHz to 1,2 MHz. The sampled analogue signals from the Passive Interpolators are converted to sampled 2-state digital signals by the Strobed Comparators. The Gated Digital-to-Analogue converters and Analogue Summer blocks perform resynchronization and sub-sampling of the digitally generated DPROC output signals, and conversion to the sampled analogue domain.

These analogue sections of the device are shown in Fig. 1.

Reference Voltage Generator

The Reference Voltage Generator generates the analogue ground reference voltage (AGND) used internally within the DPROC device. To minimize noise AGND must be externally decoupled to V_{SSA} as shown in Fig. 15.

Anti-Alias Filter

The Anti-Alias Filter is placed before the SAT sampling block to prevent any unwanted signals or high-frequency noise present on the DEMODD pin being aliased into the pass-band by the sampling action of the switched-capacitor filter. To achieve this the Anti-Alias Filter is a continuous time-distributed RC-active low-pass filter.

SAT Input Filter

The SAT Input Filter is a switched-capacitor filter which provides band-pass filtering of the SAT signals from the DEMODD pin to improve the SAT signal-to-noise ratio prior to recovery and transponding.

Passive Interpolator

The function of the Passive Interpolator is to increase the sampling rate at the output of the switched-capacitor filters. This reduces the coarseness of the zero crossing information which would otherwise cause unacceptable isochronous distortion in the recovered signal.

Strobed Comparators

The Strobed Comparators form the analogue-to-digital interface for the received data and SAT signals from the DEMODD pin. These comparators act as limiting amplifiers wich convert the filtered sampled analogue signals into 2-state sampled digital signals containing only the zero-crossing information from the analogue signal.

ANALOGUE CIRCUIT BLOCKS (continued)

Gated Digital-to-Analogue and Analogue Summer

The Gated Digital-to-Analogue converters and Analogue Summer form the interface between the digital and analogue circuitry on the transmit path of DPROC. It is at this point that the three sampled digital signals, containing SAT, ST and encoded digital data, are combined to form a composite signal. The data streams are enabled by the I^2C signals STEN, SATEN and the internal signal DATAEN respectively (DATAEN disables SAT and ST when data is being transmitted). The digital-to-analogue conversion and sub-sampling operation is performed by the Gated Digital-to-Analogue converters and Analogue Summer. The relative signal weights applied in the summer (with respect to the data path) are shown in Table 9.

Table 9 Relative signal weights

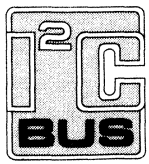
signal	relative output level AMPS and TACS
ST	1,0
SAT	0,25
DATA	1,0

Output Filter

The Output Filter is a switched-capacitor filter which performs band-limiting of the DPROC output signals in accordance with the AMPS and TACS specifications. The required below band roll-off is achieved via external AC coupling from the DATA pin.

Clock Noise Filter

The filter is a non-critical continuous time-distributed RC-active low-pass filter used to remove any switching transient residues from the output signal.



APPLICATION INFORMATION

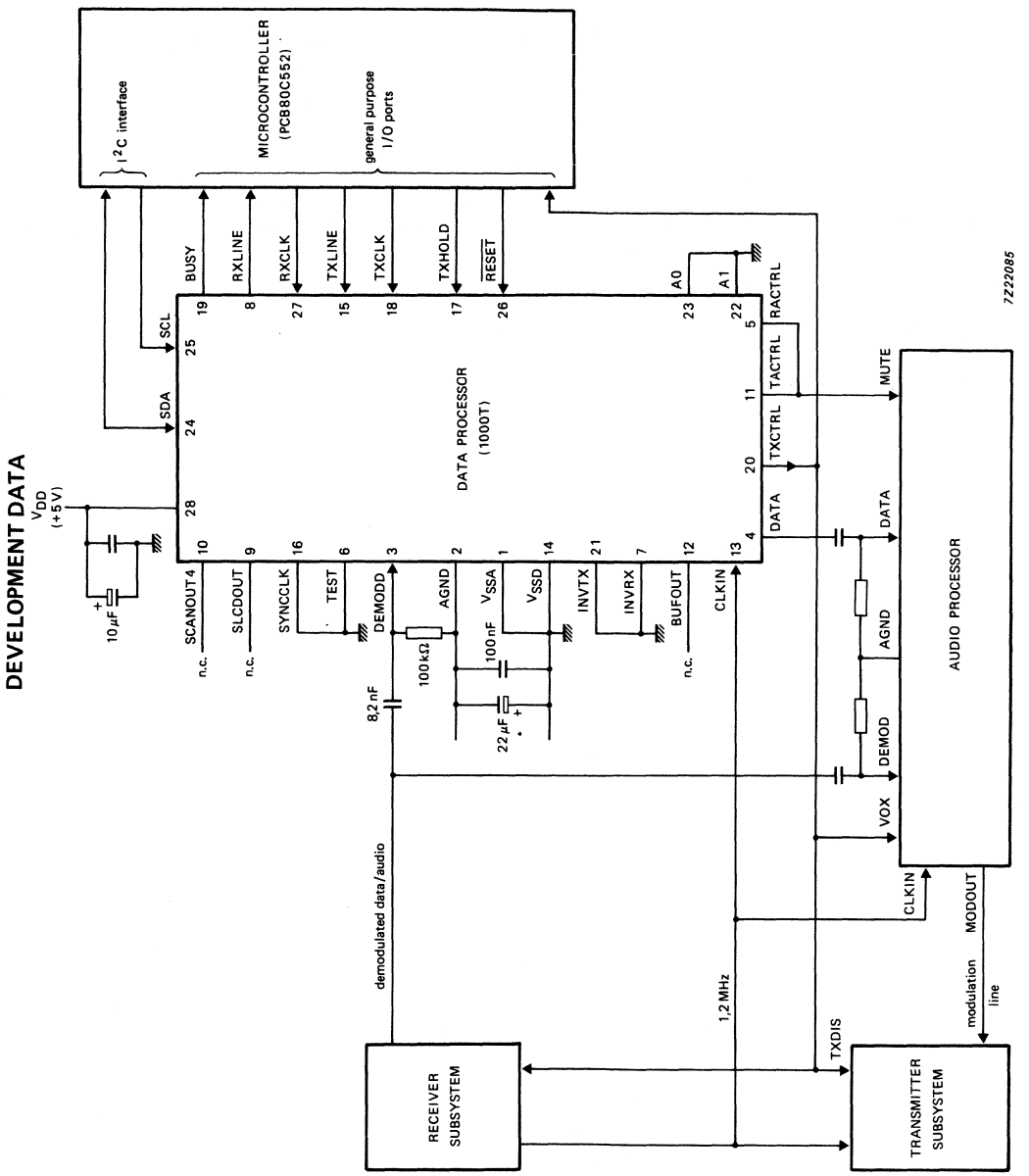


Fig. 15 DPROC application circuit.

LOW-POWER UNIVERSAL SYNTHESIZER FOR RADIO COMMUNICATION

DESCRIPTION

The UMA1010T is a low power universal synthesizer for radio communication. The IC is manufactured in bipolar technology and is designed to achieve 10 kHz to 100 kHz channel spacing in the frequency band of 400 MHz to 1 GHz.
The channel is selected via the standard I^2C-two-line serial bus.
The UMA1010T has an integrated low-power prescaler (up to 1150 MHz), a low-noise 7.5 V amplifier for the loop filter and a programmable reference divider oscillator.
Power down circuitry enables the device to be idled.

Features

- Fully programmable RF divider from 400 MHz to 1150 MHz
- I^2C-bus interface for two-line serial data transfer
- On-chip crystal oscillator from 3 MHz to 16 MHz; circuit can be used with a crystal or a tuned-circuit oscillator (TCXO)
- 4-bit crystal frequency divider that generates a reference frequency between 5 kHz and 50 kHz with a large number of crystal frequencies
- Digital comparator that provides a wide pull-in range
- High gain sample-and-hold phase comparator to achieve a low noise and a high reference rejection
- On-chip out-of-lock indication
- Two extra VCO control outputs
- Latched synthesizer alarm signal output
- Status register including out-of-lock and power failure indication
- On-chip power-on-reset presetting the registers
- Low-noise high-voltage operational amplifier allowing a large tuning range at the VCO
- Programmable phase comparator gain
- Asymmetric RF input
- Power down possibilities via the I^2C-bus or the $\overline{HPD}$ pin
- Crystal frequency divide-by-eight output

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage ranges					
digital + 5 V	V_P	4.5	5.0	5.5	V
analogue + 7.5 V	V_{P1}	4.5	7.5	8.0	V
analogue + 5 V	V_{P2}	4.5	5.0	5.5	V
Operating currents					
V_P (digital) = 5 V	I_P	–	12	–	mA
V_{P1} (analogue) = 7.5 V	I_{P1}	–	1	–	mA
V_{P2} (analogue) = 5 V	I_{P2}	–	1	–	mA
Total current in power down mode	$I_P + I_{P1} + I_{P2}$	–	3.5	–	mA
RF input frequency range	f_{RFI}	400	–	1150	MHz
Crystal frequency range	f_{XTAL}	3	–	16	MHz

PACKAGE OUTLINE

28-lead mini-pack; plastic (SO28; SOT136A).

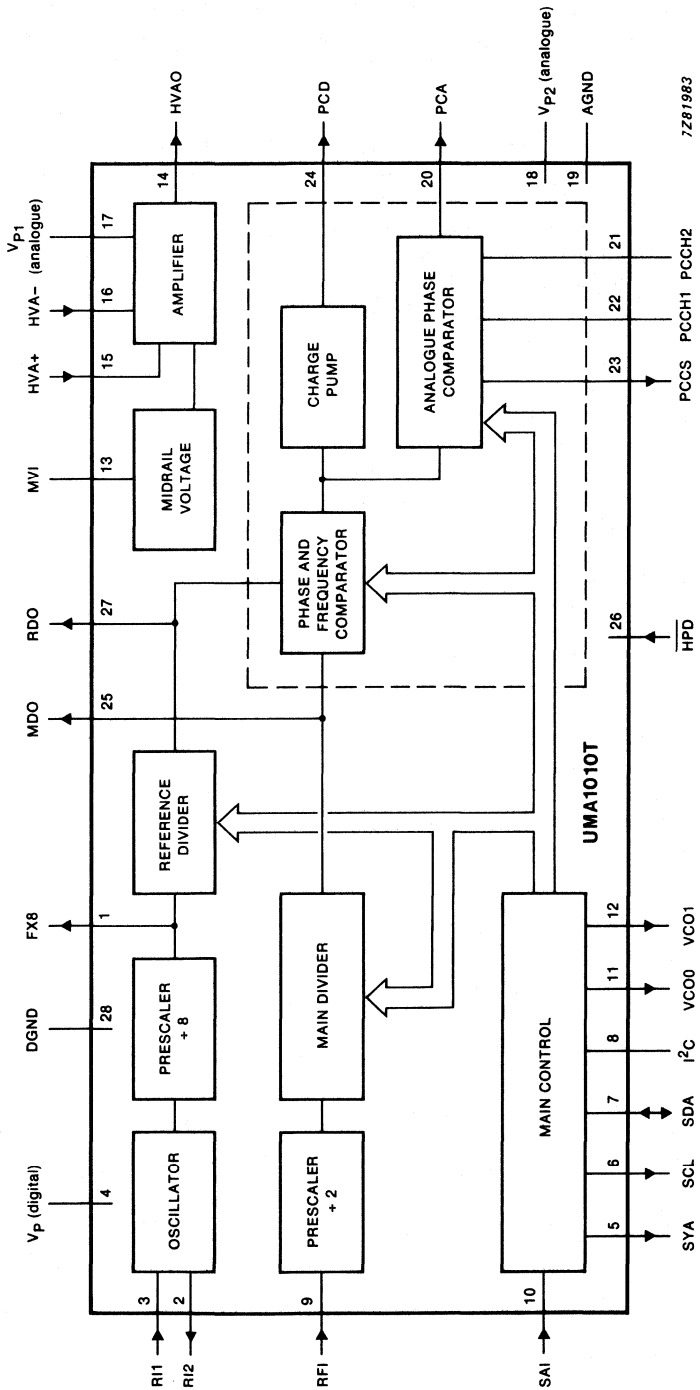


Fig. 1 Block diagram.

DEVELOPMENT DATA

PINNING

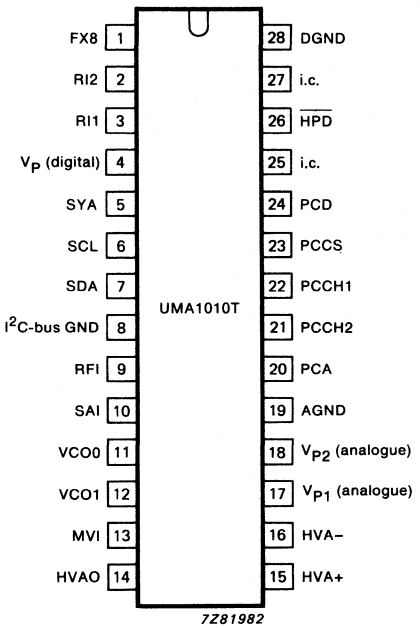


Fig. 2 Pinning diagram.

1	FX8	Output reference prescaler
2	RI2	Reference input 2
3	RI1	Reference input 1
4	V_P	Digital + 5 V supply
5	SYA	Synthesizer alarm
6	SCL	Serial clock line ⎫ I²C-bus
7	SDA	Serial data line; input/output ⎭ I²C-bus
8	I²C-bus GND	Ground for I²C-bus
9	RFI	RF input
10	SA1	Slave address select input
11	VCO0	Oscillator buffer switch output 0
12	VCO1	Oscillator buffer switch output 1
13	MV1	Mid-rail voltage (not buffered)
14	HVAO	Output high-voltage amplifier
15	HVA+	Non-inverting input high-voltage amplifier
16	HVA−	Inverting input high voltage amplifier
17	V_{P1}	Analogue +7.5 V supply
18	V_{P2}	Analogue + 5 V supply
19	AGND	Analogue ground
20	PCA	Analogue phase comparator output
21	PCCH2	Phase comparator external hold capacitor node 2
22	PCCH1	Phase comparator external hold capacitor node 1
23	PCCS	Phase comparator external sampling capacitor node
24	PCD	Digital phase comparator output
25	i.c.	Internally connected
26	$\overline{HPD}$	Inverting hardware power-down input
27	i.c.	Internally connected
28	DGND	Digital ground

FUNCTIONAL DESCRIPTION

Power supply

V_P (digital) is the + 5 V supply which feeds the dividers, the control and the digital part of the comparator. V_{P1} (analogue) is the + 7.5 V supply for the amplifier output stage. The + 5 V analogue supply is V_{P2} (analogue) which should be very clean to prevent spurious signal on the VCO control voltage.

Main divider

The main divider is a fully programmable divider. The division ratio range is from 2048 to 262142 in steps of two. It is sufficient for 10 kHz channel spacing with an input of 1050 MHz. Due to the fixed divide-by-two prescaler, half of the ratio is programmed via the I^2C-bus in the Registers C, D and E (see Table 1).

Table 1 1/2 ratio in binary form

MSB															LSB
0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
C ◄					D			►	◄				E			►

The new programmed ratio is only updated after programming Register E.

Oscillator

To provide the reference frequency, two modes of operation exist:

- Use an external resonator connected between RI1 and RI2
- Use an external reference source as a TCXO on RI1

Reference divider

Table 2 Division ratios as a function of the program

	A0	0	1	0	1
	A1	0	0	1	1
A3	A2				
0	0	128	160	192	240
0	1	256	320	384	480
1	0	512	640	768	960
1	1	1024	1280	1536	1920

One eighth of the crystal frequency is available on pin 1 (FX8). It can be used as a reference frequency input for other circuits.

Phase comparator

The phase comparator includes two comparators:

- Digital 3-state comparator with charge pump output (PCD) which provides a wide pull-in range
- High-gain sample-and-hold analogue phase comparator output (PCA) gives the possibility of high performance.

The analogue phase comparator gives an "out-of-lock" indication when the loop phase error is outside its linear range or if one of its inputs is missing. In the event of one of these, PCA is 3-state and PCD pushes or pulls 300 μA for the duration of the phase error.

$$\text{PCD gain} = \frac{300\ \mu A}{2 \times \pi}\ \text{(A/rad)}$$

Under "in-lock" condition PCD goes to 3-state and PCA becomes active. If the bit PCD select is set PCD remains active, this is used in systems which need minimum complexity. The sampling capacitor (CC) is connected between PCCS and GND. CC fixes the gain of the phase comparator.

$$\text{PCA gain} = \frac{300}{2 \times \pi \times CC \times f_{ref}}\ \text{(V/rad)}$$

where CC is the sampling capacitor (nF)
and f_{ref} is the reference frequency (kHz).

The hold capacitor is connected between PCCH1 and PCCH2. The sample-and-hold is designed to suppress the reference frequency at the output of the phase comparator.

DEVELOPMENT DATA

Main control

Two formats for the I^2C-bus protocol have been implemented on the UMA1010T:

- Burst mode, this includes subaddressing and selectable auto-increment for writing information to the synthesizer
- Single byte without subaddressing for reading the status register of the synthesizer

The status register contains information related to the synthesizer alarm (SYA) as shown in Table 3.

Table 3 Status register

MSB							LSB
0	0	0	00L	0	L00L	LPD	DI

Where: 00L = momentarily out of lock
L00L = latched out of lock
LPD = latched power dip
DI = disable interrupt

The alarm is generated by an "out-of-lock" or a power dip and is reset when the register is read. If one of these conditions occurs SYA is forced LOW.

I²C-BUS DEFINITION BIT ALLOCATION

The I²C-bus data format to write on the synthesizer has the following form:

START – address – subaddress – data 1 – data 2 – . . . – data n – STOP where:

address 1 1 0 0 0 0 SA1 R/$\overline{W}$

SA1 is logic level on pin SA1
R/$\overline{W}$ is read/not write

subaddress 0 0 0 DI AVI SB2 SB1 SB0

DI is disable interrupt, DI = 1 disables the alarm on SYA.
AVI is auto value increment, AVI = 1 allows increment of the register pointer.
SB3 – SB0 is register pointer, it indicates the register number where data 1 will be written. The pointer value is 0 for Register A up to 4 for Register E.

data n (n up to 5)

register	pointer	bit allocation								preset values		
		7	6	5	4	3	2	1	0	decimal	binary	hexa-decimal
A	000	PD	X	X	PCD	RD3	RD2	RD1	RD0	14	00001110	0E
B	001	VCO1	X	X	VCO0	X	X	X	X	16	00010000	10
C	010	X	0	X	X	1	PCG2	PCG1	MD16	173	10101101	A0
D	011	MD15	MD14	MD13	MD12	MD11	MD10	MD9	MD8	56	00111000	38
E	100	MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0	128	10000000	80

Register A is: PD (Power down), PD = 0 is normal operation.
PCD (PCD select), PCD = 1 PCD is always active.
RD3 . . . RD0 (reference division ratio), see Table 2 preset 1536

Register B is: VCO1 set VCO1 pin.
VCO0 set VCO0 pin, VCO0 is forced LOW during an "out-of-lock" indication.

Register C is: PCG2, PCG1, i.e. gain of the phase comparator;
preset + 2 dB
00 –6 dB
01 –2 dB
10 + 2 dB
11 + 6 dB
MD16, MSB of the main division ratio.

Register D is: MD15 to MD8, division ratio bit 15 to 8.

Register E is: MD7 to MD0, division ratio bit 7 to 0. Preset 160000.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage ranges				
digital + 5 V	V_P	4.5	5.5	V
analogue + 8 V	V_{P1}	4.5	8.0	V
analogue + 5 V	V_{P2}	4.5	5.5	V
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Storage temperature range	T_{stg}	−40	+ 125	°C
Total power dissipation				
V_P = 5 V	P_{tot}	–	70	mW
power down	P_{tot}	–	16	mW

CHARACTERISTICS

T_{amb} = 25 °C unless otherwise specified

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
SUPPLY						
Supply voltage ranges						
digital + 5 V		V_P	4.5	5	5.5	V
analogue + 7.5 V		V_{P1}	4.5	7.5	8.0	V
analogue + 5 V		V_{P2}	4.5	5	5.5	V
Supply current ranges						
digital + 5 V		I_P	–	10	–	mA
analogue + 7.5 V		I_{P1}	–	0.7	1	mA
analogue + 5 V		I_{P2}	–	3	–	mA
MAIN DIVIDER						
Division ratio	step = 2		2048	–	262142	
RF input (RFI)						
Frequency range		f_{RFI}	400	–	1150	MHz
Input voltage level (RMS value)		$V_{i(rms)}$	50	–	150	mV
Input impedance		R_{RFI}	–	*	–	Ω

* Value to be fixed.

CHARACTERISTICS (continued)

parameter	conditions	symbol	min.	typ.	max.	unit
MAIN CONTROL						
Serial clock input (SCL)						
Serial data input (SDA)						
Clock frequency		f_{CLK}	0	–	100	kHz
Input voltage HIGH		V_{IH}	3	–	--	V
Input voltage LOW		V_{IL}	–	–	1.5	V
Input current HIGH		I_{IH}	–	3	10	μA
Input current LOW		I_{IL}	−10	−5	–	μA
Input capacitance		C_I	–	*	–	pF
SDA sink current	V_{OL} = 0.4 V	I_{OL}	–	–	3	mA
Slave address select input (SA1)	note 1					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Sink current HIGH		I_{IH}	–	–	0.1	μA
Source current LOW		$-I_{IL}$	–	–	2	μA
Oscillator buffer switch output 0 (VCO0)	note 2					
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	−400	–	–	μA
Oscillator buffer switch output 1 (VCO1)						
Output voltage LOW		V_{OL}	–	–	0.2	V
Sink current LOW		I_{OL}	−400	–	–	μA
Inverting hardware power down input ($\overline{HPD}$)	note 1					
Input voltage HIGH		V_{IH}	3	–	–	V
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current HIGH		I_{IH}	–	0.1	–	mA
Input current LOW		I_{IL}	−5	−2	–	μA
Synthesizer alarm (SYA)						
Input voltage LOW		V_{IL}	–	–	0.4	V
Input current LOW		I_{IL}	−400	–	–	μA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
OSCILLATOR						
Reference input 1 (RI1)						
Frequency range		f_{ref1}	3	–	16	MHz
Input level (RMS value)	sinewave	$V_{ref1(rms)}$	0.1	–	2	V
Input level (peak-to-peak value)	square wave	$V_{ref1(p-p)}$	0.3	–	5	V
Reference input 2 (RI2)	note 3					
Frequency range		f_{ref2}	3	–	16	MHz
Output impedance		Z_o	–	–	2	kΩ
REFERENCE DIVIDER						
Division ratio			128	–	1920	
Input frequency range		f_i	3	–	16	MHz
Output frequency range		f_o	5	–	50	kHz
Output reference prescaler (FX8)	note 4					
Voltage output LOW		V_{OL}	–	–	0.4	V
Sink current LOW		V_{OL}	–	–	1.5	mA
Reference divider test output (RDO)	note 5					
Voltage output LOW		V_{OL}	–	–	0.4	V
Sink current LOW		V_{OL}	–	–	500	μA

DEVELOPMENT DATA

CHARACTERISTICS (continued)

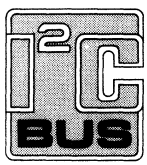
parameter	conditions	symbol	min.	typ.	max.	unit
PHASE COMPARATOR						
Frequency range		f	5	–	50	kHz
Digital phase comparator output (PCD)	note 6					
Output source current		$-I_O$	–	–300	–	μA
Output sink current		I_O	–	300	–	μA
Output leakage current		I_{LO}	–	–	10	nA
Phase comparator external sampling capacitor node (PCCS)	note 7					
Capacitance to ground		C_{PCCS}	20	–	–	pF
Phase comparator external hold capacitor nodes 1 and 2 (PCCH1; PCCH2)						
Hold capacitor		C_{HOLD}	–	1	–	nF
Analogue phase comparator output (PCA)	note 8					
Output source current		$-I_O$	–500	–	–	μA
Output sink current		I_O	–	–	700	μA
Output leakage current	V_{PCA} = 2.5 V	I_{LO}	–	–	250	nA
Gain	RF = 5 kHz; note 9	G_v	–	–	500	V/rad
	RF = 25 kHz; note 9	G_v	–	–	200	V/rad
LOOP AMPLIFIER						
Mid-rail voltage; not buffered (MV1)						
AC decoupling		C_{MV1}	–	47	–	μF

parameter	conditions	symbol	min.	typ.	max.	unit
Non-inverting high voltage amplifier input (HVA+)	note 10					
AC decoupling		C_{HVA}	–	*	–	μF
Inverting high voltage amplifier input (HVA–)						
Input impedance		Z_i	–	*	–	kΩ
Input noise (0.3 to 3 kHz)		N_{af}	–	10	–	$nV/\sqrt{Hz}$
High voltage amplifier output (HVAO)						
Open loop voltage gain		G_{ol}	30	60	–	dB
Output voltage		V_O	2	–	$V_{P1}-0.4$	V
Unity gain bandwidth		$B_{G=1}$	–	2	–	MHz
Open loop output resistance		R_O	–	70	–	kΩ
Output current		I_O	–	350	–	μA

Notes to the characteristics

1. When left open is HIGH.
2. During out-of-lock the VCO0 pin is forced LOW.
3. If a TCXO is used this pin is to remain open or be used as a reference frequency.
4. This pin is an open-collector output of the reference frequency divided by eight.
5. This pin is an open-collector output.
6. This pin is active when out-of-lock is indicated and will be 3-state when the analogue phase comparator takes over after the in-lock indication.
7. The capacitor on this pin fixes the gain of the analogue phase comparator.
8. This pin will be 3-state when out-of-lock is indicated.
9. Gain is calculated with a phase comparator gain (PVG) programmed to 6 dB.
10. This pin is connected internally, via a buffer, to MVI.

DEVELOPMENT DATA



* Value to be fixed.

APPLICATION INFORMATION

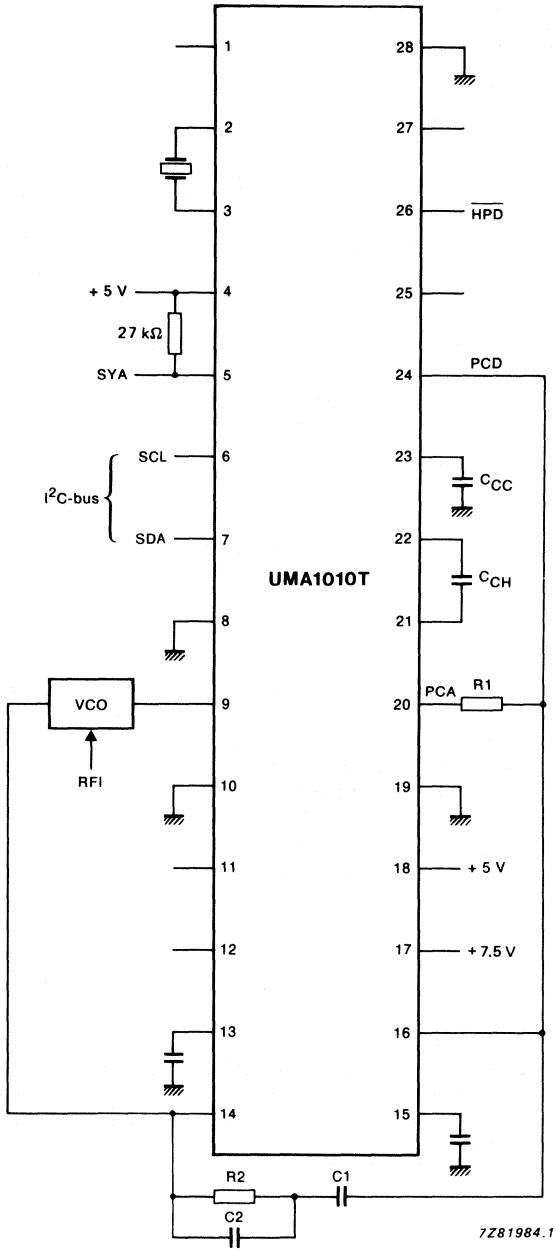


Fig. 3 Synthesizer application.

DEVELOPMENT DATA

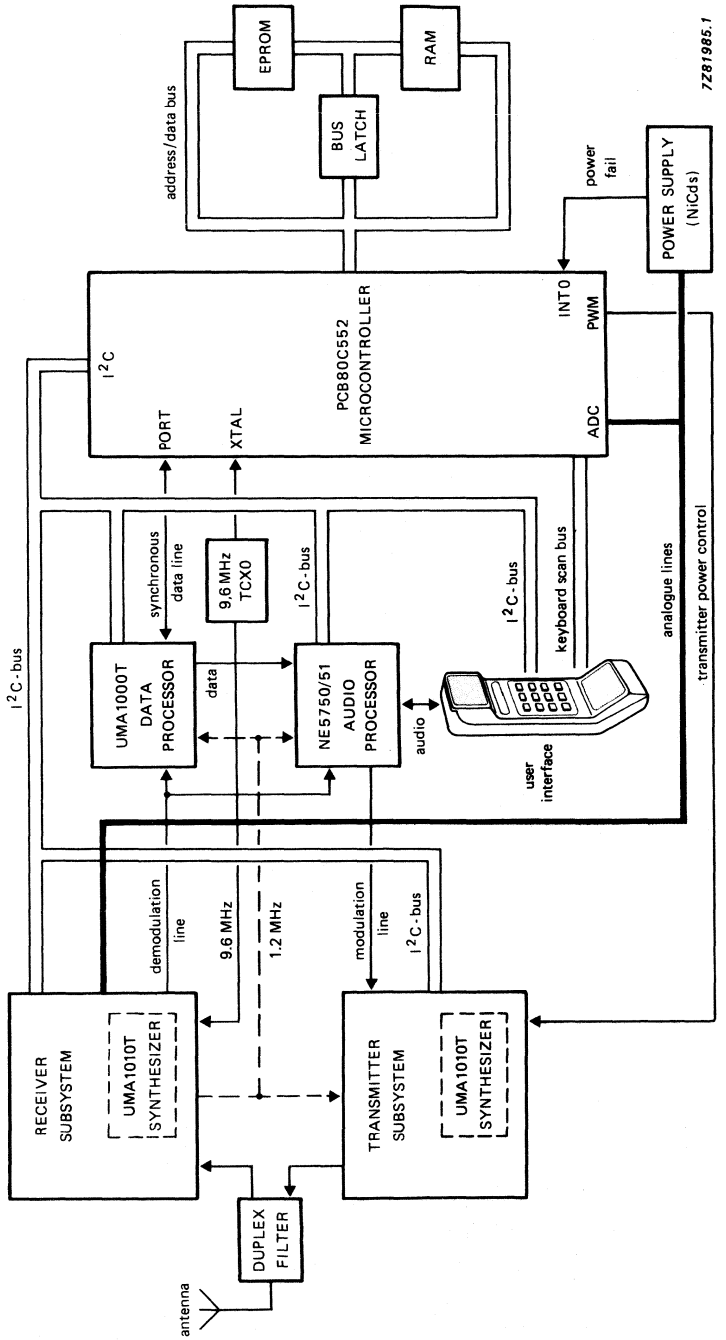


Fig. 4 Cellular radio system schematic.

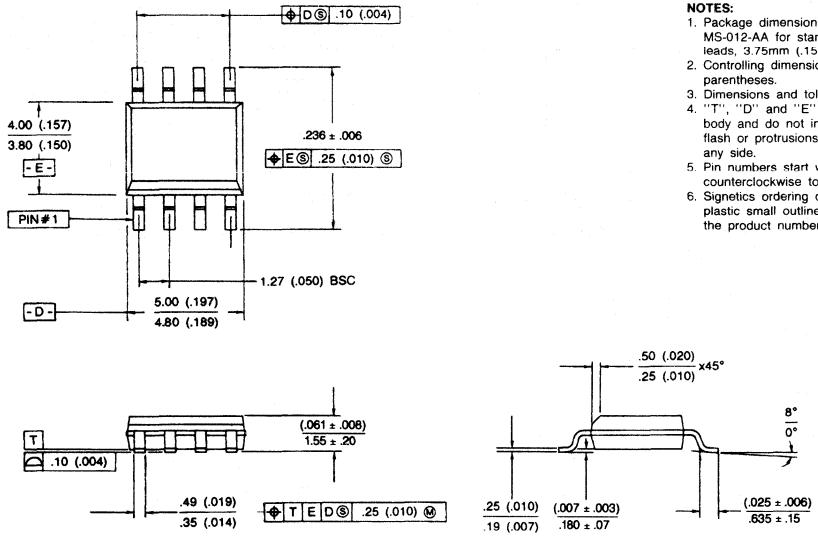
The UM1010T is a member of our Cellular Radio chipset, based on the I²C-bus, which meets the key requirements of a hand-held portable cellular set:

- small physical size
- minimum number of interconnections (serial bus)
- low power consumption
- low cost

PACKAGE INFORMATION

Package outlines
Soldering

8-PIN PLASTIC SO (D PACKAGE)

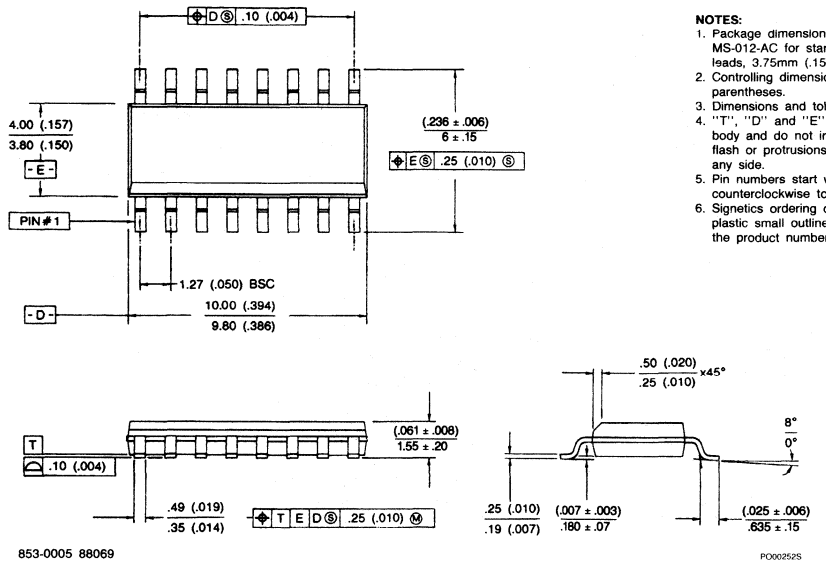


853-0174 88070

PO00273S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AA for standard small outline (SO) package, 8 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

16-PIN PLASTIC SO (D PACKAGE)

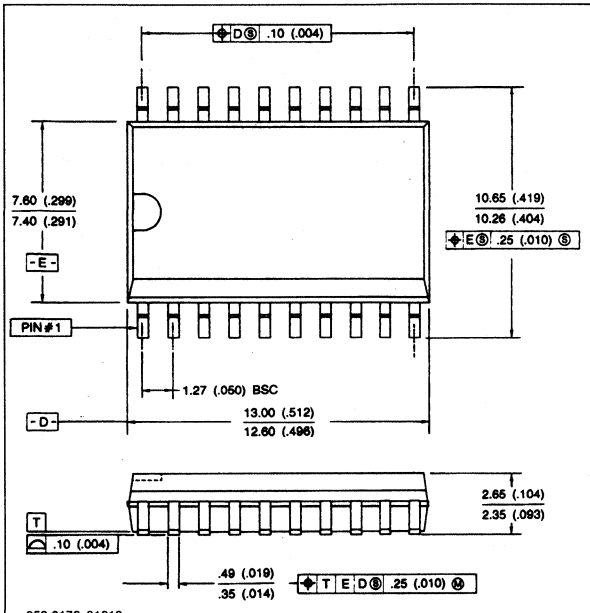


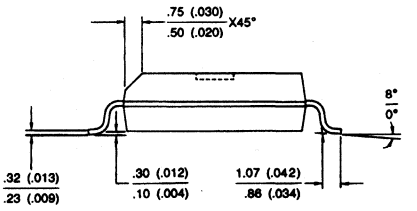
853-0005 88069

PO00252S

NOTES:
1. Package dimensions conform to JEDEC specification MS-012-AC for standard small outline (SO) package, 16 leads, 3.75mm (.150") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

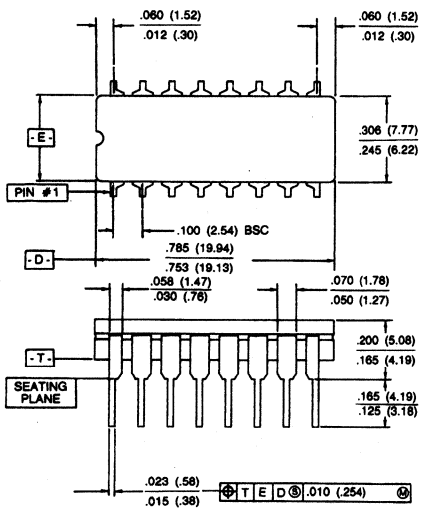
20-PIN PLASTIC SOL (D PACKAGE)

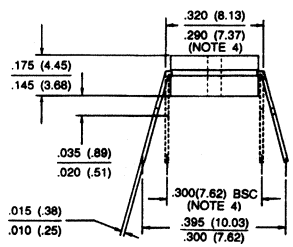




NOTES:
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

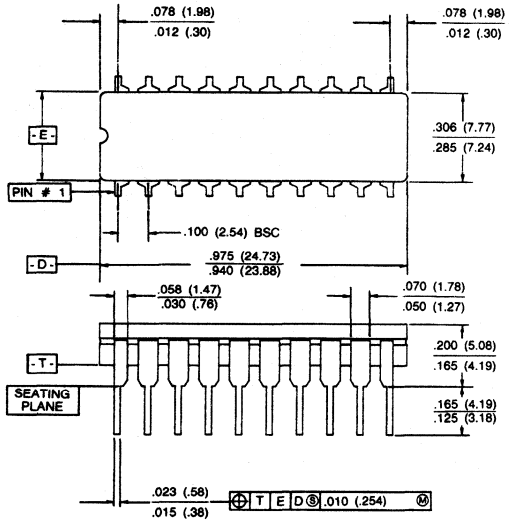
16-PIN CERDIP (F PACKAGE)

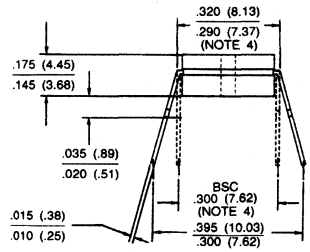




NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

20-PIN CERDIP (F PACKAGE)



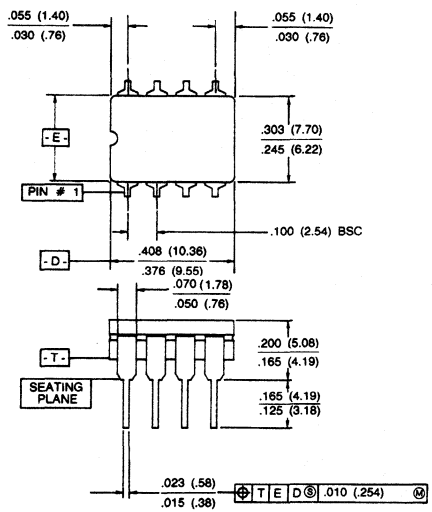


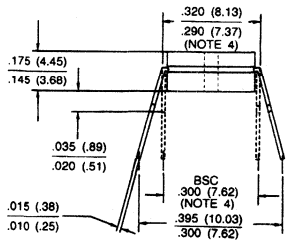
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0584 81594

PO00430S

8-PIN CERDIP (FE PACKAGE)



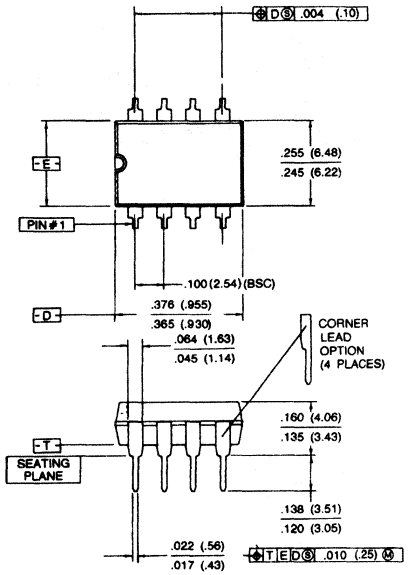


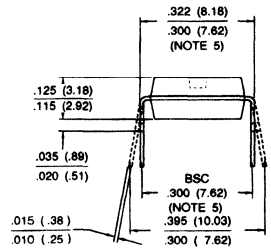
NOTES:
1. Controlling dimension: inches. Millimeters are shown in parentheses.
2. Dimensions and tolerancing per ANSI Y14.5M – 1982.
3. "T", "D", and "E" are reference datums on the body and include allowance for glass overrun and meniscus on the seal line, and lid to base mismatch.
4. These dimensions measured with the leads constrained to be perpendicular to plane T.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0580 81594

PO00480S

8-PIN PLASTIC PDIP (N PACKAGE)



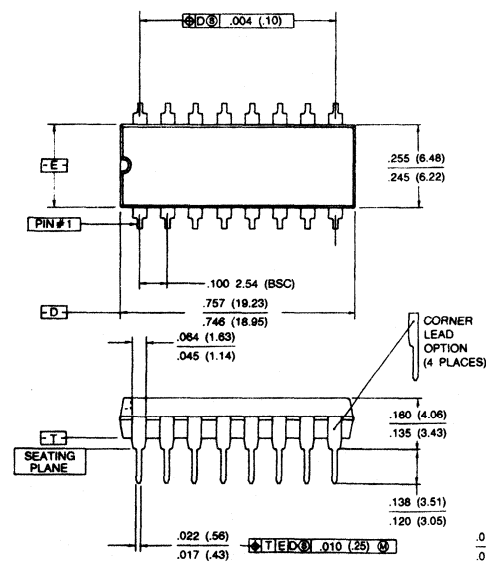


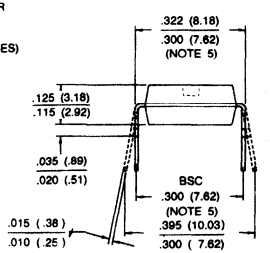
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #8 when viewed from the top.

853-0404 81230

PO00312S

16-PIN PLASTIC DIP (N PACKAGE)



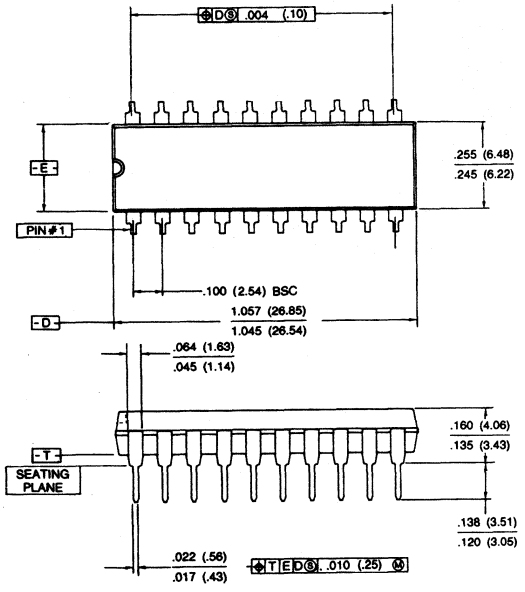


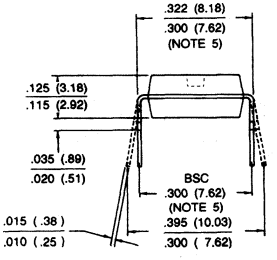
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

853-0406 81232

PO00280S

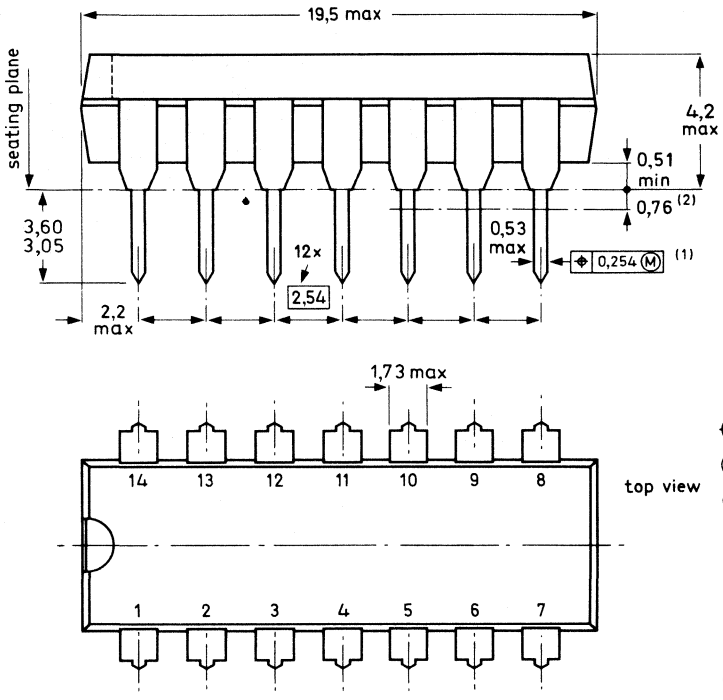
20-PIN PLASTIC DIP (N PACKAGE)





NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

14-LEAD DUAL IN-LINE; PLASTIC (SOT27)



⊕ Positional accuracy.

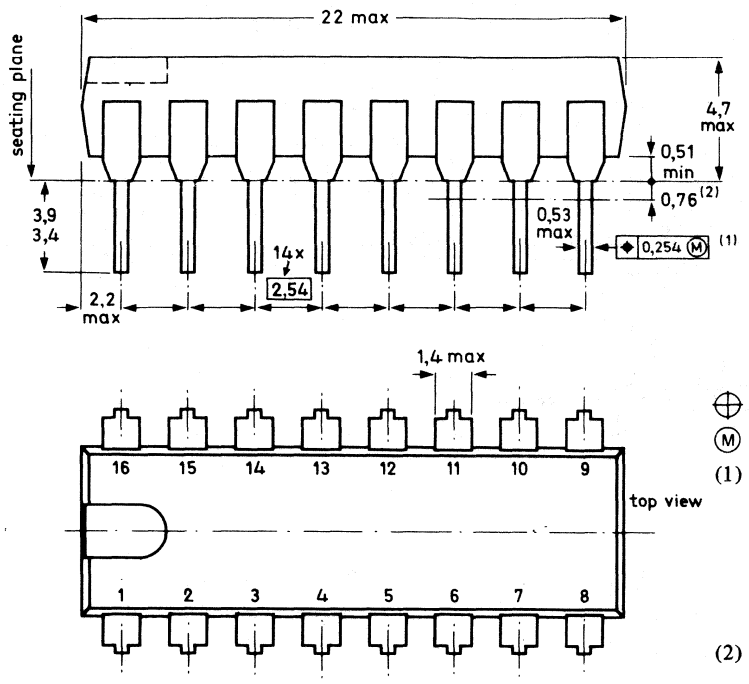
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

16-LEAD DUAL IN-LINE; PLASTIC (SOT38)



Dimensions in mm

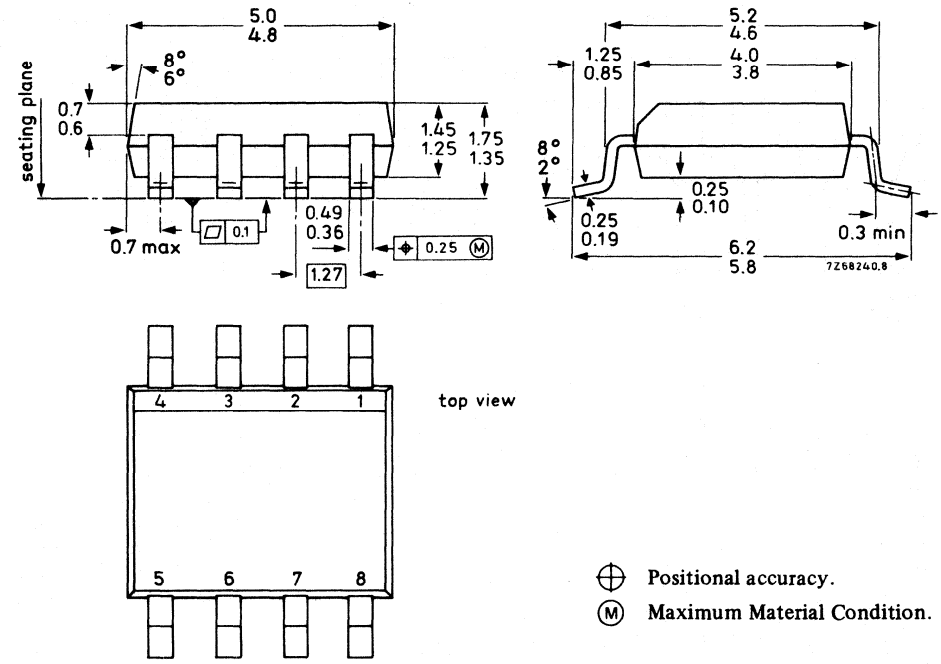
⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

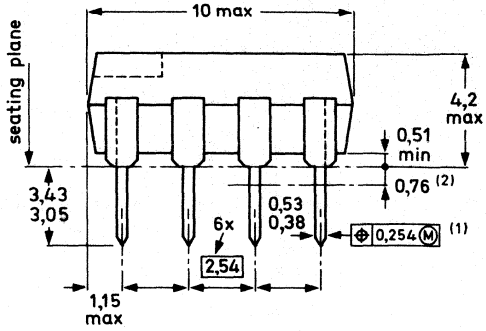
(2) Lead spacing tolerances apply from seating plane to the line indicated.

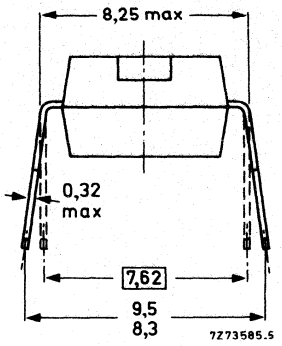
8-LEAD MINI-PACK; PLASTIC (SO8; SOT96A)

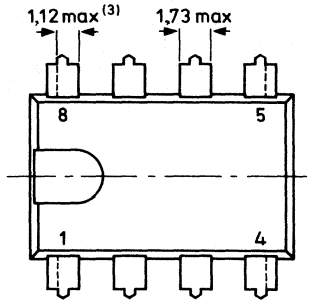


Dimensions in mm

8-LEAD DUAL IN-LINE; PLASTIC (SOT97)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

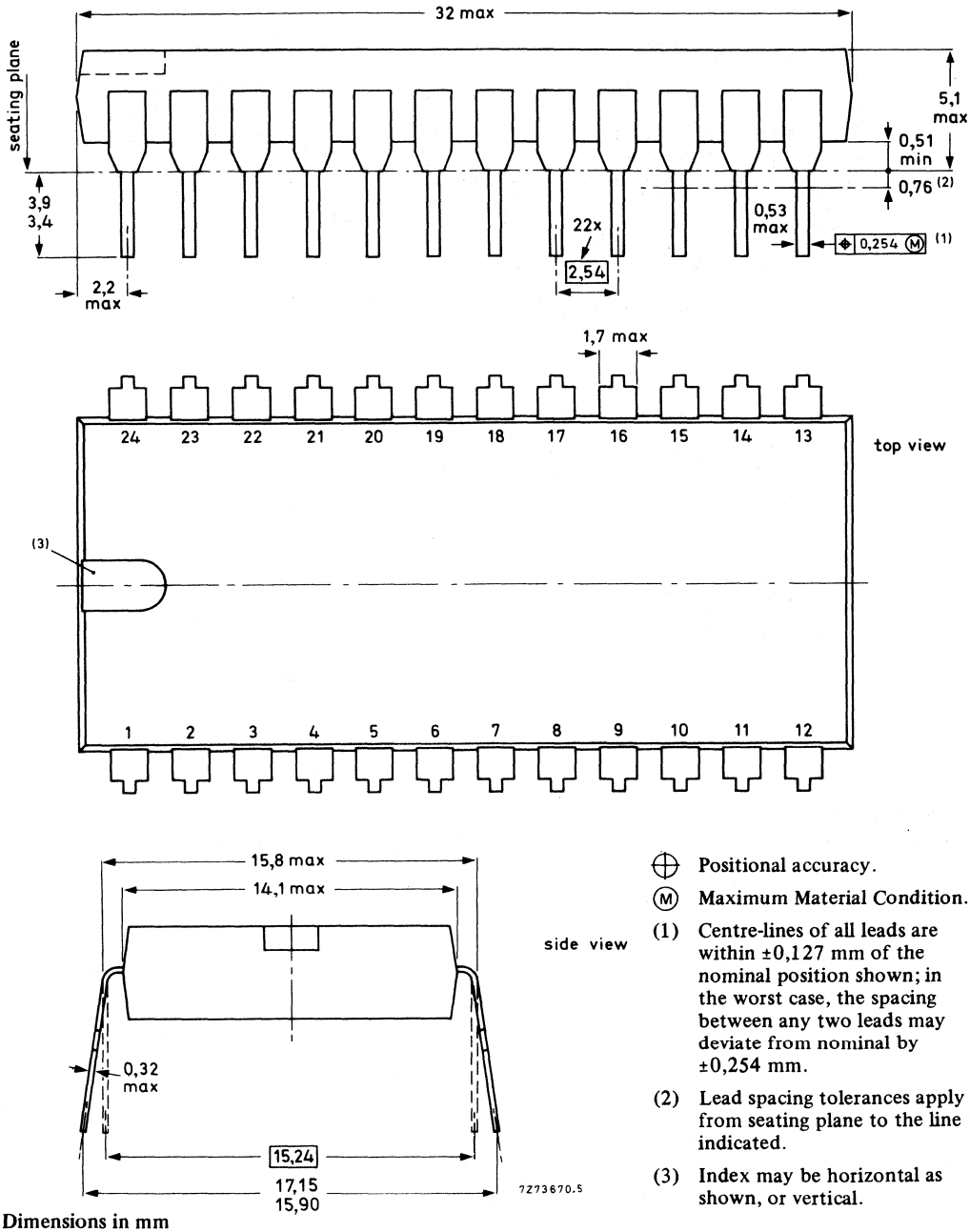
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Only for devices with asymmetrical end-leads.

Dimensions in mm

24-LEAD DUAL IN-LINE; PLASTIC (SOT101A, B, F, G, L)



Dimensions in mm

⊕ Positional accuracy.

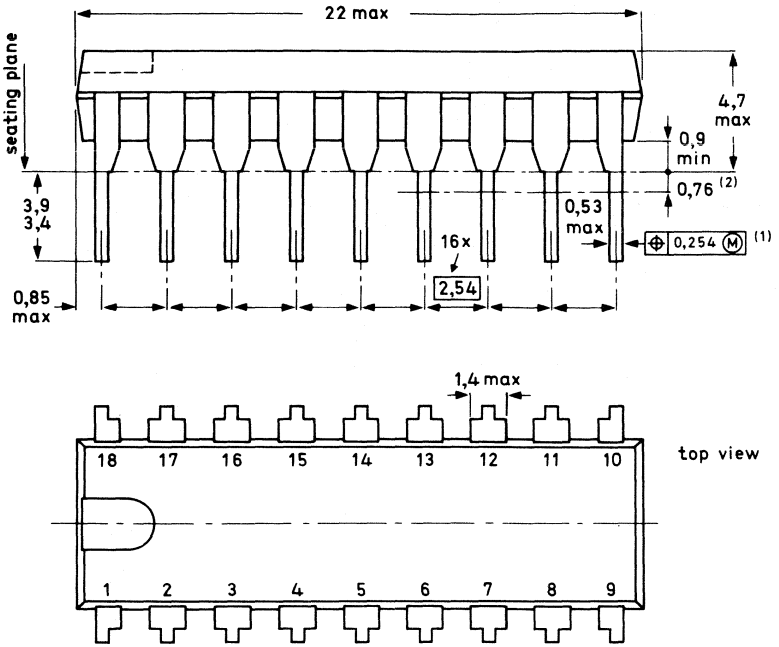
Ⓜ Maximum Material Condition.

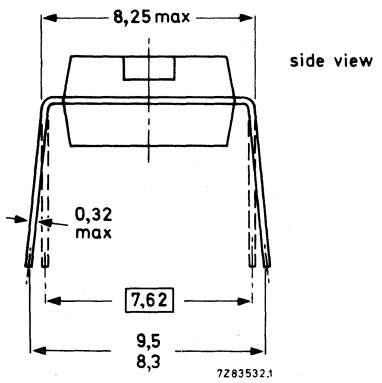
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

18-LEAD DUAL IN-LINE; PLASTIC (SOT102)





⊕ Positional accuracy.

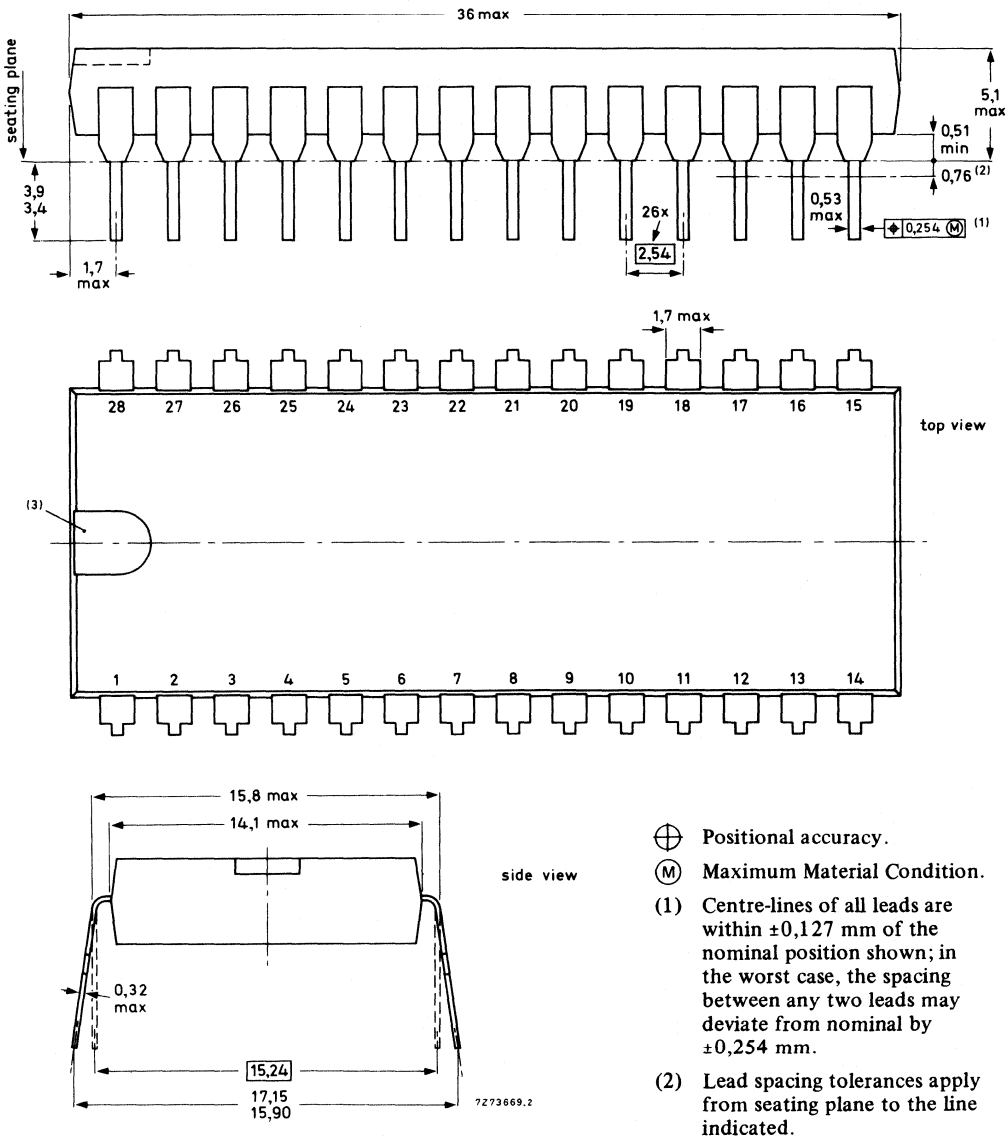
Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT117)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

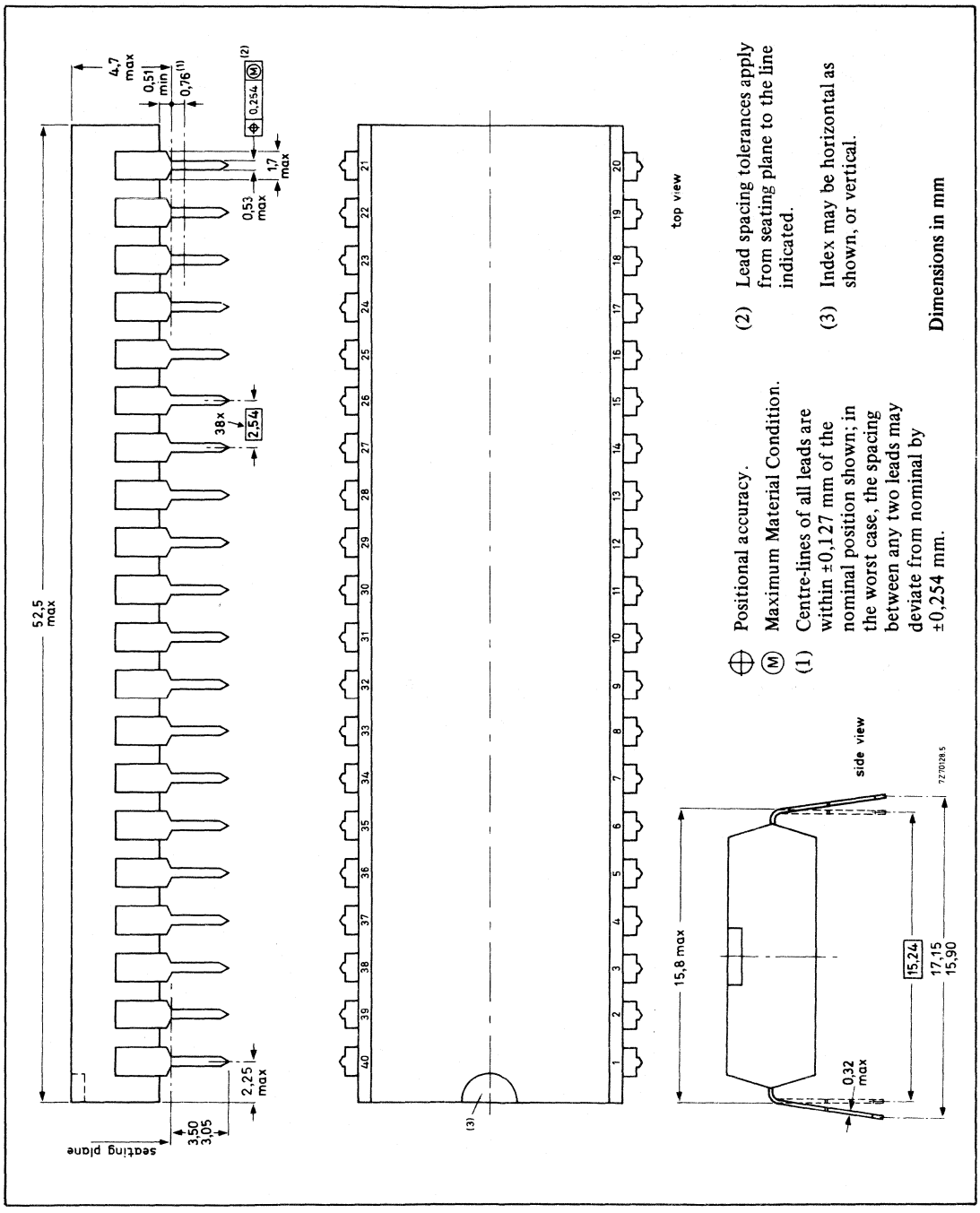
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

40-LEAD DUAL IN-LINE; PLASTIC (SOT129)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

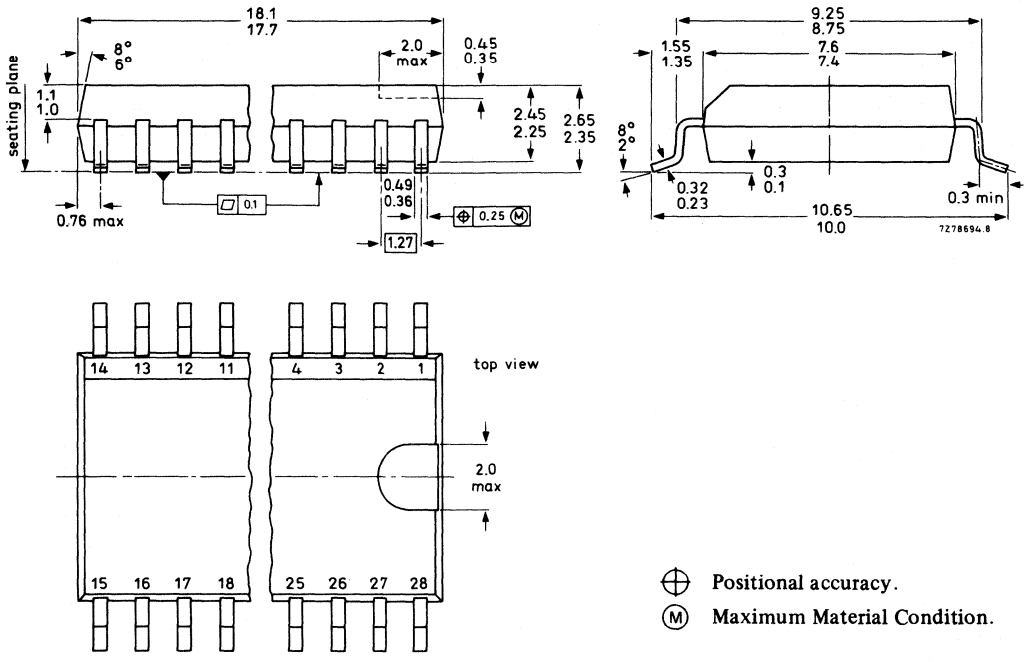
(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

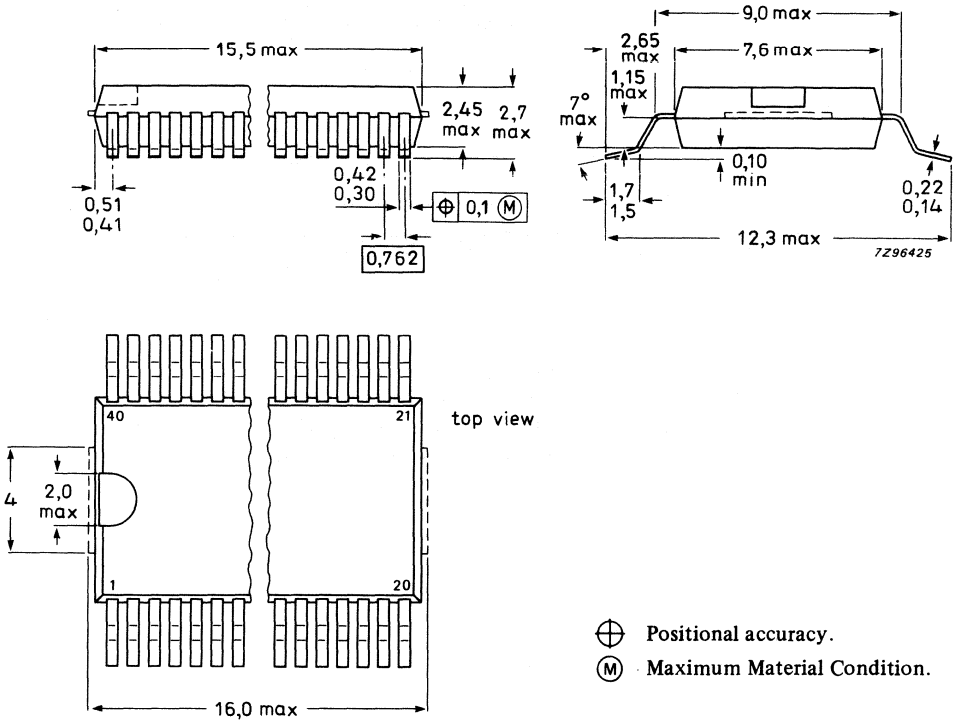
Dimensions in mm

28-LEAD MINI-PACK; PLASTIC (SO28; SOT136A)



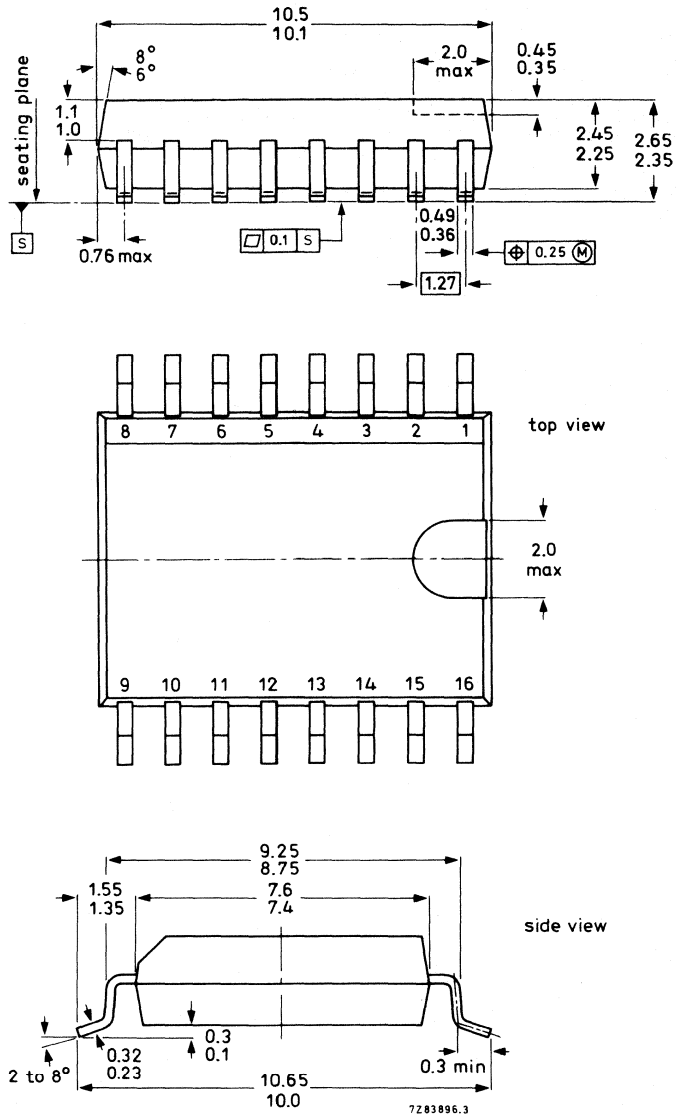
Dimensions in mm

40-LEAD MINI-PACK; PLASTIC (VSO40; SOT158A)



Dimensions in mm

16-LEAD MINI-PACK; PLASTIC (SO16L; SOT162A)

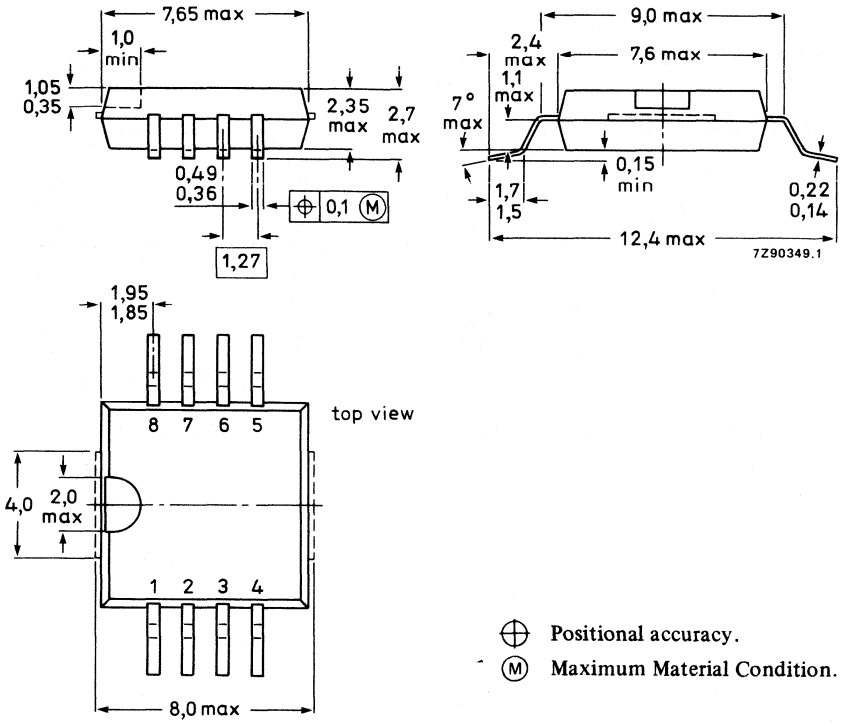


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

8-LEAD MINI-PACK; PLASTIC (SO8L; SOT176)

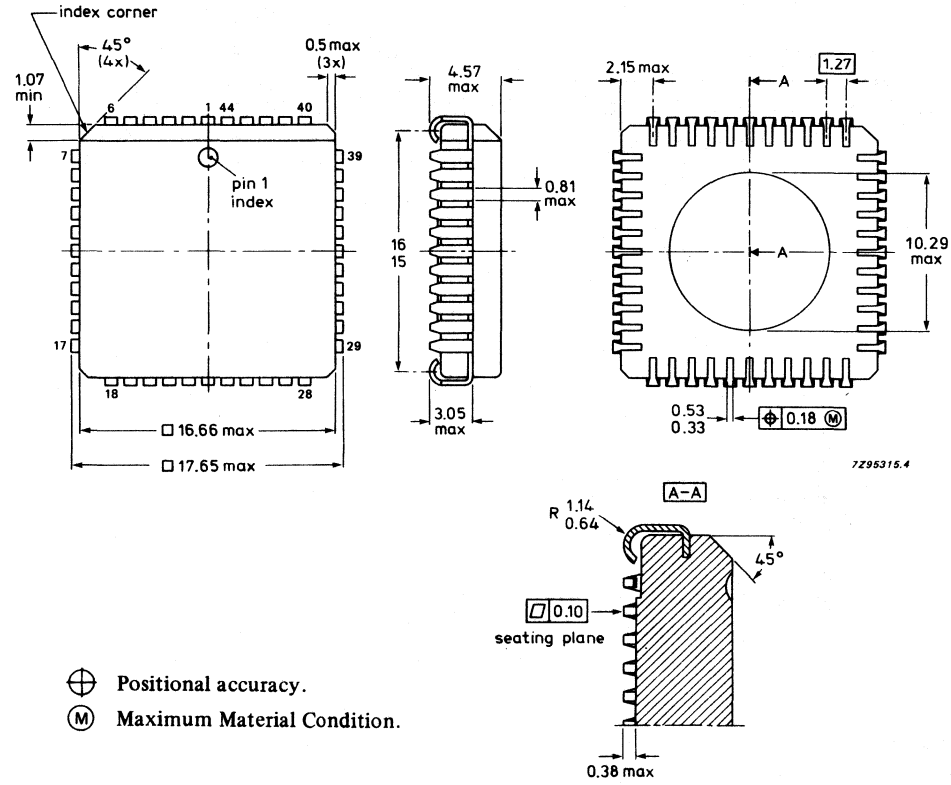


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

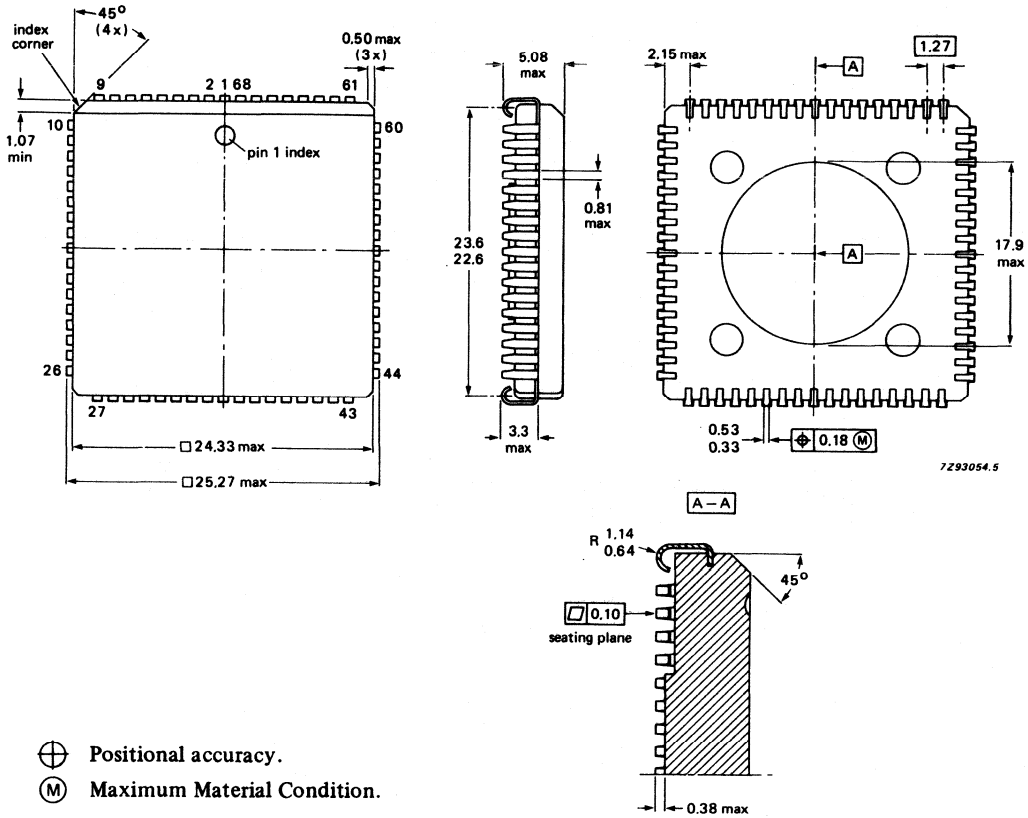
Dimensions in mm

44-LEAD PLASTIC LEADED CHIP CARRIER (PLCC) (SOT187)



Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'PEDESTAL' VERSION (SOT188)

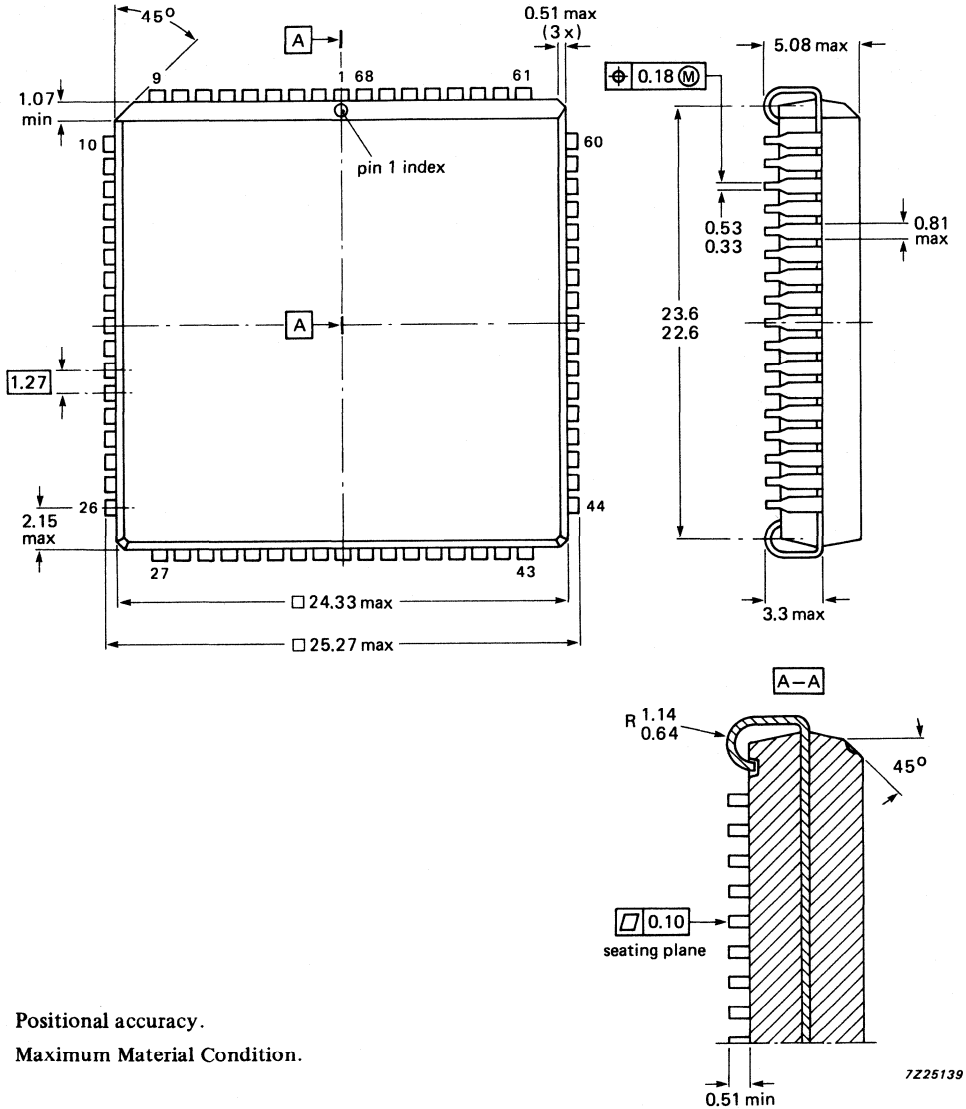


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

68-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'POCKET' VERSION (SOT188AA)

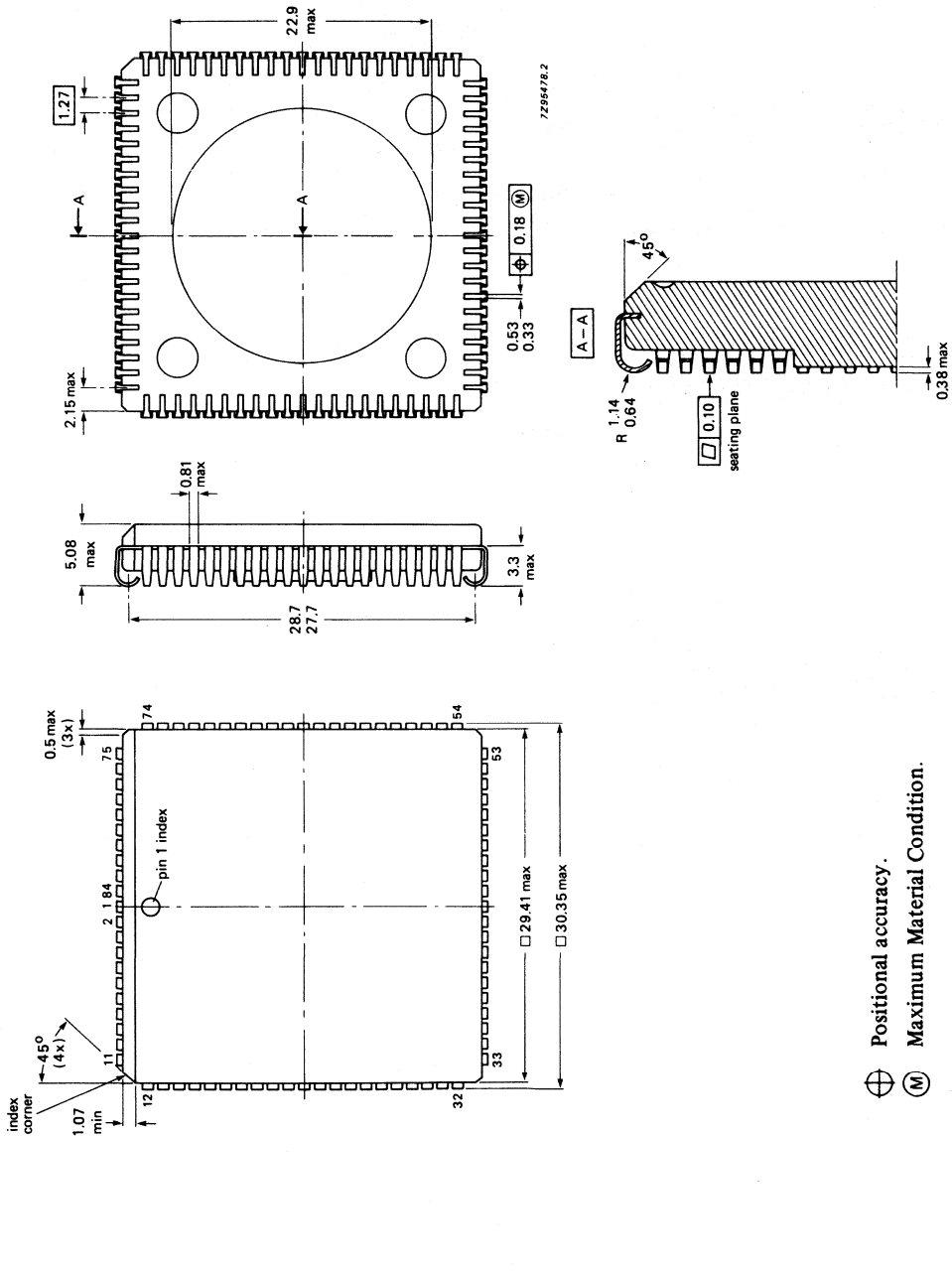


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

84-LEAD PLASTIC LEADED CHIP CARRIER (PLCC); 'PEDESTAL' VERSION (SOT189)

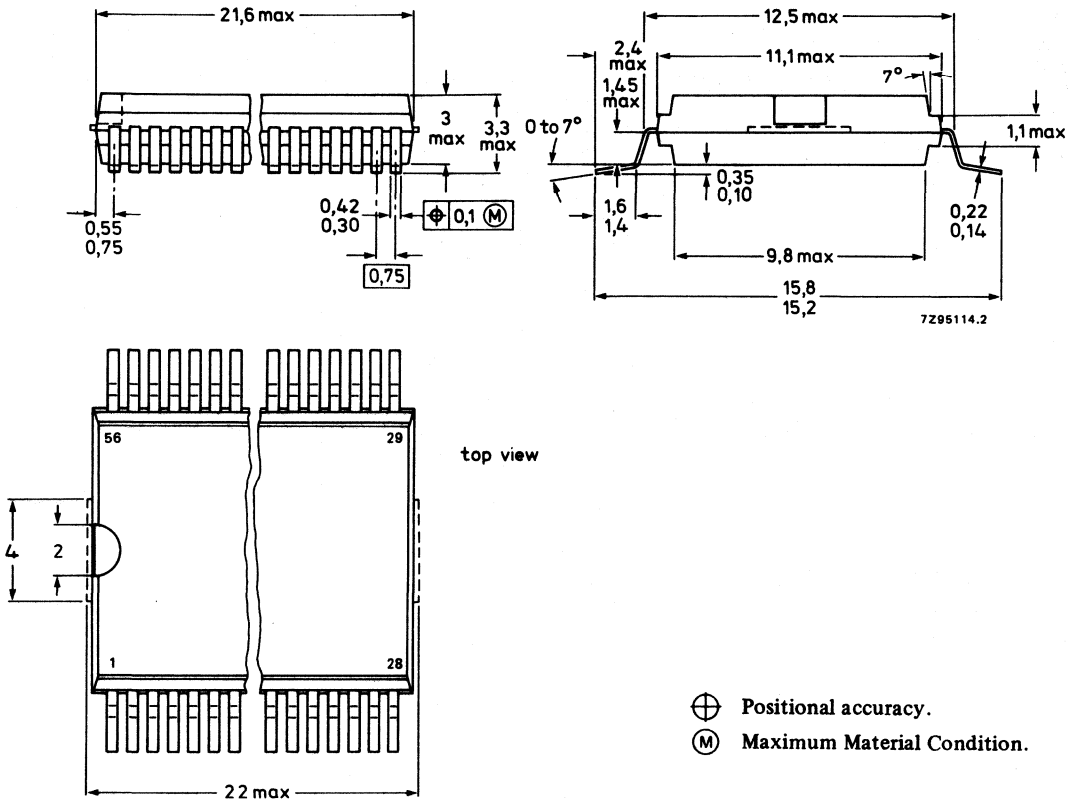


⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

56-LEAD MINI-PACK; PLASTIC (VSO56; SOT190)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

Dimensions in mm

SOLDERING PLASTIC MINI-PACKS

1. By hand-held soldering iron or pulse-heated solder tool

Fix the component by first soldering two, diagonally opposite end leads. Apply the heating tool to the flat part of the lead only. Contact time must be limited to 10 seconds at up to 300 °C. When using proper tools, all other leads can be soldered in one operation within 2 to 5 seconds at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages).

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to substrate by dipping or by an extra thick tin/lead plating before package placement.

2. By wave

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 seconds, if allowed to cool to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

3. By solder paste reflow

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing, for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 seconds according to method. Typical reflow temperatures range from 215 to 250 °C.

Pre-heating is necessary to dry paste and evaporate binding agent.

Pre-heating duration: 45 minutes at 45 °C.

4. Repairing soldered joints

The same precaution and limits apply as in (1) above.

SOLDERING PLASTIC DUAL IN-LINE PACKAGES

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

NOTES

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 70 books with specifications on electronic components, subassemblies and materials. It is made up of six series of handbooks:

PROFESSIONAL COMPONENTS*

DISCRETE SEMICONDUCTORS

INTEGRATED CIRCUITS

PASSIVE COMPONENTS**

MATERIALS**

DISPLAY COMPONENTS

The contents of each series are listed on pages iii to viii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Components is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.
Product specialists are at your service and enquiries will be answered promptly.

* Will replace the Electron tubes (blue) series of handbooks.
** Will replace the Components and materials (green) series of handbooks.

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This series of data handbooks comprises:

T1 **Power tubes for RF heating and communications**

T2a **Transmitting tubes for communications, glass types**

T2b **Transmitting tubes for communications, ceramic types**

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T4 **Magnetrons for microwave heating**

T5 **Cathode-ray tubes**
Instrument tubes, monitor and display tubes, C.R. tubes for special applications

T6 **Geiger-Müller tubes**

T8* **Colour display systems**
Colour TV picture tubes, colour data graphic display tube assemblies, deflection units

T9 **Photo and electron multipliers**

T10 **Plumbicon camera tubes and accessories**

T11 **Microwave semiconductors and components**

T12 **Vidicon and Newvicon camera tubes**

T13 **Image intensifiers and infrared detectors**

T15 **Dry reed switched**

T16** **Monochrome tubes and deflection units**
Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

* Handbook T8 will be issued in a new series of handbooks (Display Components) and will have the new handbook code DC01.

** Handbook T16 will be re-issued in the future in the new series of handbooks (Display Components).

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This series of data handbooks comprises:

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S5 **Small-signal field-effect transistors**

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S14 **Liquid Crystal Displays**

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current code		new handbook code
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C4 C5	Ferroxcube potcores, square cores and cross cores Ferroxcube for power, audio/video and accelerators	MA01**
C7	Variable capacitors	PA04$^{\triangle}$
C8	Variable mains transformers	PC10$^{\triangle\triangle}$
C9	Piezoelectric quartz devices	PA07$^{\triangle}$
C11	Varistors, thermistors and sensors	PA02$^{\triangle}$
C12	Potentiometers, encoders and switches	PA03$^{\triangle}$
C13	Fixed resistors	PA08$^{\triangle}$
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C15	Ceramic capacitors	PA06$^{\triangle}$
C16	Permanent magnet materials	MA02**
C19	Piezoelectric ceramics	MA03**
C20	Wire-wound components for TVs and monitors	DC05*
C22	Film capacitors	PA05$^{\triangle}$

* These handbooks will be re-issued in the future in the new series of handbooks (Display Components).

** These handbooks will be re-issued in the future in the new series of handbooks (Materials).

$^{\triangle}$ These handbooks will be re-issued in the future in the new series of handbooks (Passive Components).

$^{\triangle\triangle}$ These handbooks will be re-issued in the future in the new series of handbooks (Professional Components).

MATERIALS

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MA02* **Permanent magnet materials**

MA03* **Piezoelectric ceramics**

* Not yet issued in the Materials series of handbooks.

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This series of handbooks comprises:

DC01 **Colour display systems**

DC02* **Monochrome tubes and deflection units**

DC03* **Television tuners, coaxial aerial input assemblies**

DC04* **Loudspeakers**

DC05* **Wire-wound components for TVs and monitors**

* Not yet issued in the Display Components series of handbooks.

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